Specifications

Working in groups of two, you will design a differential amplifier, and test it in a feedback configuration driving a speaker. Design your amplifier to meet the following specifications.

- You may use a single supply or dual supplies totaling up to 12 V. \( V_{CC} + |V_{EE}| \leq 12V \).
- The input transistors should be MOS transistors (ALD 1106 or 1107). The remainder of the circuit may use any transistors available from the parts store.
- Coupling: The amplifier inputs, outputs, and any inter-stage connections should be DC-coupled. I.e. you should not use any coupling capacitors or transformers. You may need a compensation capacitor (which will be discussed in class) and you should definitely bypass your supplies with a bypass capacitor.
- Total open-loop voltage gain \( A_V \geq 20\text{dB} \) with a single-ended output driving a 8\( \Omega \) load, including all stages and bias circuits.
- Common-mode rejection ratio \( \text{CMRR} \geq 30\text{dB} \).
- Circuit should include biasing circuitry, but it need not be supply independent. A supply-derived bias such as a resistor and diode-connected transistor between the supplies would be appropriate.
- The amplifier will be tested in a feedback configuration with gain of 6 dB (\( A_V = 2V/V \)).
- Deliver \( \geq 1 \text{ mW} \) to an 8\( \Omega \) speaker. This corresponds to a 126 mV amplitude sine wave output. This will require a follower output stage or the class-AB output stage described in the second option above. With the 8\( \Omega \) load, your amplifier should still provide 20 dB of open-loop gain and 6 dB of closed-loop gain.
- The amplifier should exhibit carrier-spur ratio (CSR) of less than 26 dB when driving 1 mW onto an 8\( \Omega \) load.
- Incorporate a class AB output stage into your op-amp. More efficient output stages (e.g. class C, D, etc.) that can meet the distortion requirement are also acceptable.
- Optimize your design to minimize quiescent power consumption. Since \( P = IV \), you can do this by minimizing current consumption, or by designing your amplifier to operate from a lower supply voltage.

Design Procedure

You need not follow this design procedure to the letter, but the methods described here should give you an idea of how to complete the design. We will work backwards from the load, but read through the whole procedure before you begin, as there will be some iterating between the steps and awareness of the upcoming steps will save you time.
Figure 1: Feedback configuration for gain of 2. The input should be centered around the reference voltage, which can be a supply-derived voltage of $V_{DD}/2$ for a single supply or ground for a dual supply.

- Design your output stage, accounting for the load it must drive. (Because the linearity will be substantially improved by the feedback, it may make sense to complete a first pass design and simulate before performing extensive analysis to ensure sufficient linear range in any of the stages). Determine how much driving resistance it can tolerate (i.e. the output resistance of the second-to-last stage). At this point, you it is probably easiest to use an ideal voltage source to generate the level shift between the “push” and “pull” devices of the AB output stage. You may also need to manually adjust the DC input voltage in order to get the output voltage at the correct DC level. Note that DC current flowing across the load resistor will disrupt the bias point and hurt performance.

- Design your input stage. Determine the small-signal parameters ($g_m$, etc.) needed to meet the specifications and then the DC bias conditions needed. Use the plots in the datasheet to determine what bias currents are needed to achieve the required small-signal parameters. CMOS transistors are required here, as is often the case when a high input impedance is needed. Experiment with different topologies in simulation. The inputs can be PMOS or NMOS and the load can be resistors or a current mirror. You can also choose the bias current. It is possible to design a single stage to achieve adequate gain, but you may opt to design a lower-gain first stage and add a second stage. At this stage you will probably want to provide your bias current from an ideal current source so it is easy to vary. Simulate the input stage alone and verify that it works and provides adequate gain.

- You may find that the gain or CMRR is better with different output or common-mode input levels. Explore this and discuss what you find and reasons for it in the report. If your gain is high, you may also find that you need to apply a small differential offset to the input in order to keep the output in an acceptable range.

- Determine the need for any subsequent stages. Do you need more gain? Improved drive (i.e. some buffering)? Design additional stages as needed to meet the specifications. Include an appropriate load resistor ($10k\Omega$) during simulation. You may want to modify the input stage to make the subsequent stage designs easier (or possible).

- After you connect all of your stages together, simulate the small-signal (open-loop) gain of the completed op-amp. In a closed-loop configuration, the feedback will allow the op-amp to settle to the correct differential DC input voltage, but for open-loop simulations, you may need to perform a DC sweep to find it. Make sure that you are meeting the open-loop specifications.

- The circuit you have can now be represented as an operational amplifier (op-amp). Determine which input is inverting and which is non-inverting. Connect your amplifier in the feedback configuration shown in Figure 1(a). If you observe oscillations at the output, add a capacitor to ground at the output of the input stage. (We will discuss this issue in class.) Is it operating as expected? Are any stages consuming unexpected power? Is there a systematic offset that is reducing gain or hurting performance. At this stage, you may want to refine one or more stage of your design.

- Design your bias circuit.
Test Procedure

Below are listed a few considerations which you may find helpful.

**ESD** MOS transistors are more fragile than BJTs. The gate oxide can easily be destroyed by static discharge. In order to avoid this, discharge yourself by touching a well-grounded metallic object before touching the transistors.

**Load Resistor** You may choose to terminate the load resistor to the mid-rail reference voltage, roughly $V_{DD}/2$ for a single supply or ground for a dual supply. Termination to the negative supply will result in a significant DC current, which could potentially disrupt the bias point.

**Negative Input** It may be useful to be able to adjust the negative (inverting) input voltage independently from the positive input voltage, so that you can adjust both the common-mode input voltage and the DC differential offset. To do that, you may choose to use a potentiometer to build an adjustable voltage divider, as shown in Figure . Be sure to bypass it with a large capacitor so that it provides a solid DC voltage.

Perform the following tests with an 8Ω load resistor connected, unless otherwise indicated. Include oscilloscope captures of all measurements in your report.

1. With one input fixed, sweep the other input and record the output voltages. (You may also use LabView to automate this if you prefer.) This can be a fairly coarse sweep for most of the range, but capture several points in the steep transition region. From this sweep calculate the input-referred offset voltage (the differential input voltage when the output was approximately halfway between the supplies).

2. Measure the differential-mode gain $A_{DM}$. Because of the difficulty in providing a true differential signal, we will actually measure the gain in response to a single-ended signal, which contains components of both $A_{CM}$ and $A_{DM}$. However, under reasonable assumptions ($A_{CM} \ll A_{DM}$), this will give us a good estimate of $A_{DM}$. Apply a small signal (large enough to observe easily, but not much larger) to the input that you swept in the previous step. The DC differential input should be in the high-gain range identified in the previous step. Observe the output amplitude and calculate the gain.

3. Sweep the frequency upward until the drain drops by 3 dB. Record this as the upper cutoff frequency.

4. Return the frequency to 1 kHz and choose an input amplitude that gives an output amplitude of about 130 mV. Using the FFT function, measure the carrier-spur ratio and capture an image of the FFT. In your report, discuss how this measurement compares to its simulated value.

5. Measure the common-mode gain $A_{CM}$. Connect the two inputs together and set their DC level at a voltage that results in a roughly mid-rail output voltage. If you are using dual supplies, this voltage can be ground. Drive a sine wave at 1 kHz into the two inputs and measure the gain.
6. Connect the op-amp in the feedback configuration shown in Figure 1(a). Choose an input amplitude that gives approximately 130 mV output amplitude. Measure the gain and high-frequency cutoff \( f_H \) (where gain decreases by 3 dB). Measure the CSR at 1 kHz and capture an image of the FFT.

7. Measure the total current consumption, with no input signal. The input should have a DC level that results in a roughly mid-rail output voltage, but no sine wave.

8. With the amplifier operating in the feedback configuration and an output amplitude of 130 mV, measure the total power consumption when driving the specified load. Calculate the overall power efficiency.

9. In closed-loop configuration, find the output amplitude at which the gain drops by 1 dB. This is known as \( P_{1dB} \) the 1 dB compression point, and is a common metric of the large-signal linearity of amplifiers.

10. There should be an MP3 player with a headphone-test clip adapter available in the lab. With the amplifier operating in an open-loop configuration, play some music through your amplifier and the speaker with the volume adjusted to a comfortable level. Make a note of the approximate peak-peak voltage at the output. Also note the quality of the sound.

11. Repeat the previous step using a closed-loop configuration. Adjust the volume to provide a similar output amplitude and a similar volume. Compare the quality of the sound to the previous step.

**Report Contents and Format**

Document the design and testing of your amplifier in a report. Templates for both MS Word and L\TeX\ are available on the class web page. Figures should be included in the body of the document, not printed separately and stapled to the back. Your report should thoroughly explain your design process. The items below represent key parts of the design, but do not constitute an exhaustive list of what your report should explain. The report should include the following sections:

**Introduction** Describe the purpose of the project, what you intended to accomplish, and inform the reader about the upcoming sections. Two to three paragraphs should be sufficient.

**Design and Analysis**

- Discuss your choice of transistors. Both MOS and BJT have advantages and disadvantages for this project. Explain why you chose one or the other for various parts of the circuit. Remember that your amplifier need not be all-MOS or all-bipolar (though the inputs must be MOS).
- Discuss how you chose your topology and current level. Describe your design process. Include plots of key simulation results.
- Include here or in an appendix your hand calculations for the current levels in each stage, and (if applicable) in the supply-independent bias circuit.
- Simulation results. Include an AC sweep showing the high cutoff frequency, a transient simulation showing the output at full scale (0.5 V), and a DC sweep showing the variation of supply current with supply voltage (use the same supply range as in testing, above). Include schematics for the complete circuit, including biasing. If necessary to yield a readable schematic, break the schematic into two parts. Please ensure that the schematics and simulation results are readable and have a light-colored background.

**Results** Include the measurements and oscilloscope screen shots that you took during testing. Include a table summarizing the following performance measurements: \( A_V, f_L, f_H, I_{CCQ}, \) CSR (both measurements), as well as the measurements specific to your added features. Email these specifications to the instructor in an email with the subject line “Project 2 Results.” The data should be in a single line formatted as “<Open-loop differential \( A_v \) in dB>, <Open-loop common-mode gain in \( dB \)>, <Closed-loop \( A_v \) in \( dB \)>,” etc. On a separate line, list your team members.

**Discussion** Compare your measurement results with the simulation results. Were they similar? What might account for the difference? Describe any difficulties you encountered in the design or testing phase.
**Conclusion**  Briefly summarize your results. What did you learn? What might you do differently if you were doing the project again? What improvements might you want if you were going to use the amplifier in a real-life application?

Your lab checkoff sheet should also be included at the end of your report.