An FPGA Implementation of a Time Delay Reservoir Using Stochastic Logic

<table>
<thead>
<tr>
<th>Journal:</th>
<th>Journal on Emerging Technologies in Computing Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manuscript ID</td>
<td>JETC-2017-0193</td>
</tr>
<tr>
<td>Manuscript Type:</td>
<td>SI: Neuromorphic Computing</td>
</tr>
<tr>
<td>Date Submitted by the Author:</td>
<td>15-Dec-2017</td>
</tr>
<tr>
<td>Complete List of Authors:</td>
<td>Loomis, Lisa; Air Force Research Laboratory, RITB Merkel, Cory McDonald, Nathan; Air Force Research Laboratory,</td>
</tr>
<tr>
<td>Computing Classification Systems:</td>
<td>Emerging architectures, Neural networks, Reconfigurable logic and FPGAs, Stochastic processes</td>
</tr>
</tbody>
</table>
An FPGA Implementation of a Time Delay Reservoir Using Stochastic Logic

LISA LOOMIS, Air Force Research Laboratory
CORY MERKEL, Air Force Research Laboratory
NATHAN MCDONALD, Air Force Research Laboratory

This paper presents and demonstrates a stochastic logic time delay reservoir design in FPGA hardware. The reservoir network approach is analyzed using a number of metrics, such as kernel quality, generalization rank, performance on simple benchmarks, and is also compared to a deterministic design. A novel re-seeding method is introduced to reduce the adverse effects of stochastic noise, which may also be implemented in other stochastic logic reservoir computing designs, such as echo state networks. Benchmark results indicate that the proposed design performs well on noise-tolerant classification problems, but more work needs to be done to improve the stochastic logic time delay reservoir’s robustness for regression problems.

KEYWORDS
Stochastic computing, reservoir computing, time delay reservoir, Bernstein polynomials

1 INTRODUCTION

Reservoir computing (RC) is proving to be a powerful machine learning technique for regression, classification, and forecasting of time series data. Introduced in the early 2000s by Jaeger [1] and Maass [2], RC is a type of neural network with an untrained recurrent hidden layer called a reservoir. A major computational advantage of RC is that the output of the network can be trained on the reservoir states using simple regression techniques, without the need for backpropagation. In the last decade and a half, RC has been successful in a number of wide-ranging applications domains such as image classification [3], bio-signal processing [4], and optimal control [5]. In some domains, RC has outperformed state-of-the-art techniques and is often easier to implement than methods such as Kalman filtering or long short term memory. Beyond its computational advantages, one of the main attractions of RC is that it can be implemented efficiently in hardware with low area and power overheads.

Today, there are three major categories of RC. The first is echo state networks (ESNs) [1], where reservoirs are implemented using a recurrent network of continuous (e.g. logistic sigmoid) neurons. The second category, referred to as liquid state machines (LSMs) [2] utilizes recurrent connections of spiking (e.g. leaky integrate and fire) neurons. A challenge in both of these categories is routing. A reservoir with \( H \) neurons will have up to \( H^2 \) connections, potentially creating a large area and power overhead. A third category of RC called time delay reservoirs (TDR) [6] avoids this overhead by time multiplexing resources. TDRs utilize a single neuron and a

This material is based upon work supported by the Air Force Office of Scientific Research (AFOSR) under award number FA9550-15-RIFICR122. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author and do not necessarily reflect the views of AFRL. The material and results presented in this paper have been cleared for public release, unlimited distribution (Case Number 88ABW-2017-6271). Author’s addresses: Air Force Research Laboratory/ Information Directorate Rome, NY, USA.

Contains previously published material from C. Merkel, "Design of a time delay reservoir using stochastic logic: A feasibility study," 2017 International Joint Conference on Neural Networks (IJCNN), Anchorage, AK, 2017, pp. 2186-2192.

Permission to make digital or hard copies of part or all of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. Copyrights for components of this work owned by others than ACM must be honored. To copy otherwise, distribute, republish, or post, requires prior specific permission and/or a fee. Request permissions from permissions@acm.org.

© 201X ACM.
delayed feedback to create reservoirs with either a chain topology or even full connectivity (see Supplemental Material of [6]).

Besides a reduction in routing overhead, TDRs have two key advantages over ESNs and LSMs. First, adding additional neurons to the reservoir is trivial and amounts to increasing the delay in the feedback loop. Second, TDRs can use any dynamical system to implement their activation function and can easily be modeled via delay differential equations. This second point is particularly useful since it means that TDRs can be implemented using a variety of technologies. For example, in [6], Appeltant et al. used a Mackey-Glass oscillator, which models a number of physiological processes (e.g. blood circulation), as the non-linear node in a TDR. In [7], a TDR is demonstrated using a coherently driven passive optical cavity. A TDR has also been implemented using a single XOR gate with delayed feedback [8]. A common thread among all of these implementations is that they are analog and some, such as the photonic implementation, are still large prototypes that have yet to be integrated into a chip. Aside from the higher cost and design effort for analog implementations, they are much more susceptible to noise, especially in RC, where the system operates on the edge of chaos.

Digital RC designs, and digital circuits in general, have much better noise immunity compared to analog implementations. There have been a number of digital designs proposed for ESNs and LSMs, such as [9], but digital TDR designs are presently scarce. One example is given in [10], where the authors have implemented a Mackey-Glass-type TDR on an FPGA. One of the challenges with digital implementations is that the area cost can be high due to the requirement of multipliers for input weighting and implementation of the activation function. This is especially true if high precision is required. However, not all applications require high precision. An alternative design approach to conventional digital logic is stochastic logic, where values are represented as stochastic bit streams and characterized by probabilities. Stochastic logic has previously been used to implement ESNs [11, 12]. In this work, we explore the feasibility of implementing TDRs with stochastic logic. To the best of the author’s knowledge, this is the first paper to demonstrate a stochastic logic TDR in hardware.

The rest of the paper is organized as follows. Section 2 discusses in detail time delay reservoir computing and stochastic logic. Section 3 presents a digital circuit implementation of a TDR based on stochastic logic. Section 4 presents our experimental results, both in simulation and FPGA hardware, followed by discussion of these results. Final conclusions are in Section 5.

2 Background

2.1 Time Delay Reservoirs (TDR)

RC makes use of a random recurrent neural network in order to regress, forecast, or classify time series data. The basic structure of an RC is shown in Figure 1. This is different from a traditional recurrent neural network (RNN) in that the hidden layer weights are randomly set and not trained, avoiding calculation-intensive techniques such as backpropagation. Time series inputs \( u \) in the input layer are multiplied by a random weight matrix \( W^{(s)} = W_{in}u^{(s)} \), and then used as inputs to the reservoir layer. Here, the index \( p \) is used to denote a discrete timestep. Within the reservoir layer, there are a number of neurons that are connected with each other through a random weight matrix \( x^{(p+1)} = f(W_{res}x^{(p)} + s^{(p)}) \), where \( f \) is an activation function. The state of the reservoir \( x^{(p)} \) is then connected to an output layer via a third weight matrix \( y^{(p)} = c(W_{out}x^{(p)}) \), where \( c \) is the output function. In this work, \( c \) is an identity function, such that the output is given directly by the product of the output weight matrix and the reservoir state. The output layer is trained such that the reservoir performs a particular function (e.g. regression, classification) of the inputs as

\[
W_{out} = \arg \min_{W_{in}} \frac{1}{2} \sum_{p=1}^{m_{\text{train}}} (y^{(p)} - \hat{y}(p))^2
\]

(1)

where \( y^{(p)} \) is the expected output at timestep \( p \) and \( m_{\text{train}} \) is the size of the training set. In this work, this optimization problem is solved via regularized least squares:

\[
W_{out} = (X^TX + \lambda I)^{-1}X^TY
\]

(2)
where $\lambda$ is the regularization parameter, $I$ is the identity matrix, $X$ and $Y$ are the matrices composed of the reservoir states and the expected outputs corresponding the training set $u$, respectively. Note that the only parameters that are modified during training are the output weights $W_{\text{out}}$. The random input and reservoir layers serve to randomly project the input into a high-dimensional space which increases the linear separability of inputs. In addition, the recurrent connections of the reservoir provide a short-term memory that allows inputs to be integrated over time. This is critical to analyzing data based on its behavior over multiple timesteps.

$$s = W_{in} u$$

$$\hat{y} = c(W_{out} x)$$

Fig. 1. Basic structure of an RC design, showing the three layers: input, reservoir, and output.

A TDR (Figure 2) is a special type of RC that shares resource time to reduce routing overhead. A single non-linear node (shown as an opaque black circle) provides the activation function, analogous to the sigmoid and spiking functions in the ESN and LSM, respectively. The activation function can be any polynomial or transcendental function and is sometimes governed by a delay differential equation (DDE). At each timestep $p$, the reservoir’s input is sampled and held for a duration of $H$ smaller timesteps of duration $\Omega$. For each of the $H$ timesteps, the held input is multiplied by an input weight $W_{in}$ and then added to a bias term $\theta_i$. The weighted and biased input is added to the delayed state of the reservoir node, $x^{(p-1)}$, where $\tau \geq H$ is the delay of the feedback. In this work, $\tau = H + 1$. The sum is then fed back into the activation function. In this way, $H$ components make up the reservoir’s state corresponding to each sampled and held input. This approach is attractive because the hardware implementation usually consists of a simple circuit and a delay line without the routing overhead associated with ESNs and LSMs. However, TDRs are more restricted in terms of their connectivity patterns and may require numerical simulation of DDEs when implemented in software. For an instantaneous activation function (e.g. $f$ settles within $\Omega$) and $\tau = H + 1$, a TDR has a unidirectional ring topology. The next section will present an efficient hardware implementation of a TDR using stochastic computing techniques.
2.2 Stochastic Logic

Stochastic logic was pioneered by von Neumann [13] half a century ago and was later adopted by the machine learning community to reduce hardware complexity, power, and unreliability [14, 15]. At the heart of stochastic computing is the stochastic representation of binary numbers. In a single-line bipolar [15] stochastic representation, a q-bit 2’s complement number $z \in \{-2q-1, \ldots, -1, 0, 1, \ldots, 2q-1, 1\}$ is mapped to a Bernoulli process $Z$ of length $L$ [16, 17]:

$$\bar{z} \equiv \Pr(Z_r = 1) = \frac{z + 2^q}{2^q - 1} = \frac{\bar{z} + 1}{2}$$

(3)

where the terms $\bar{z} \in [0, 1]$ and $\bar{z} \in [-1, 1]$ are defined for convenience and $r = 1, 2, \ldots, L$ is an index into the stochastic bit stream. Converting from the binary to the stochastic representation can be achieved using a random number generator such as a linear feedback shift register (LFSR) and a comparator. If the random number is less than or equal to the value held in the register, then a logic 1 value is produced on the output. Otherwise, the comparator output is logic 0 [16]. As $L$ becomes large, $\Pr(Z_r = 1)$ approaches the value in (3). Converting from a stochastic representation back to a digital number can be achieved by counting the number of 1’s and 0’s in the stream. By initializing the counter to zero, adding ‘1’ every time a ‘1’ is encountered in the stream and subtracting ‘1’ every time a ‘0’ is encountered, the final counter value will be the 2’s complement binary representation of the bit stream.

One advantage of a stochastic representation is that several mathematical operations become trivial to implement in hardware. For example, consider the logic function $Y_i = g(I_1, I_2, \ldots, I_n)$, where each input $I_j$ to the function is mapped to a stochastic bit stream $Z_j$ and, therefore, the output is also a stochastic bit stream. The probability that the function evaluates to ‘1’ is given by

$$\Pr(Y_i = 1) = \sum_{I_1, I_2, \ldots} f(I_1, I_2, \ldots) \prod_{k=1}^{n} \Pr(Z_{k} = I_k)$$

(4)

which is a multivariate polynomial in $z_1, z_2, \ldots, z_n$ with integer coefficients and powers no greater than 1. Implementations for a number of stochastic logic operations are shown in Figure 3. Note that, in general, the implementation of stochastic logic operations will be different for unipolar representations. For example, in the case of a bipolar representation, multiplication is implemented using an XNOR gate (Figure 3). (Alternatively, for a unipolar representation, the same operation uses an AND gate.) Other basic operations, such as negation and weighted averaging, are achieved using inverters and multiplexers, respectively.

![Fig. 3. Basic logic gates implementing mathematical operations on single-line bipolar stochastic bit streams.](image)

In addition to the simple mathematical operations shown in Figure 3, it will also be necessary for the stochastic logic RC to implement a non-linear activation function. If the activation function is a polynomial, it can readily be implemented as the sum of product logic, e.g. AND, OR logic, per Eq. (4). However, if the activation function is not a transcendental function, then one way to implement it is to approximate it with a polynomial. Bernstein polynomials are a good choice, since they can approximate any function on the unit interval (or any other interval) with arbitrary precision, which was shown by Bernstein as part of a proof of the Weierstrass approximation theorem [18, 19]. The Bernstein basis polynomials of degree $n$ are defined as [19]
An FPGA Implementation of a Time Delay Reservoir Using Stochastic Logic

\[ b_{k,n}(\bar{z}) \equiv \binom{n}{k} \bar{z}^k (1 - \bar{z})^{n-k}, k = 0, 1, ..., n \]  

(5)

A Bernstein polynomial of degree \( n \) is defined as a linear combination of the \( n \)-degree Bernstein basis polynomials:

\[ B_n(\bar{z}) \equiv \sum_{k=0}^{n} \beta_k b_{k,n}(\bar{z}) \]  

(6)

The coefficients \( \beta_k \) are called the Bernstein coefficients. Furthermore, the \( n \)-degree Bernstein polynomial for a function \( f(\bar{z}) \) is defined as

\[ B_n(f; \bar{z}) = \sum_{k=0}^{n} f\left( \frac{k}{n} \right) b_{k,n}(\bar{z}). \]  

(7)

Bernstein showed that \( B_n(f; \bar{z}) \) approaches \( f(\bar{z}) \) uniformly on \([0, 1]\) as \( n \) approaches infinity.

It can also be shown that the set of Bernstein basis polynomials \( \{b_{k,n}\} \) of degree \( n \) forms a basis for the space of power-form polynomials with real coefficients and degree no more than \( n \). In other words, the power-form polynomial

\[ p(\bar{z}) = \sum_{i=0}^{n} a_i \bar{z}^i \]  

(8)

can be written in the form of (6). In [20], it is shown that the Bernstein coefficients can be obtained from the power-form coefficients as

\[ \beta_k = \frac{1}{n} \sum_{j=0}^{n-k} \binom{n}{j} \binom{j}{k} a_i. \]  

(9)

It is important to note that if \( f \) in (6) maps the unit interval to the unit interval, then \( f(k/n) \) is also in the unit interval. Similarly, Qian et al. have proven that if \( p \) in (8) maps the unit interval to the unit interval, then the Bernstein coefficients in (9) will also be in the unit interval. Coefficients in the unit interval are important because they can be represented stochastically.

In summary, any non-polynomial (polynomial) function that maps the unit interval to the unit interval can be approximated by (written in the form of) a Bernstein polynomial with coefficients that are also in the unit interval. To find the coefficients for non-polynomial functions, one may form the constrained optimization problem [17]:

\[ \text{minimize} \ \{\beta_0, ..., \beta_n\} \int_{0}^{1} \left( f(\bar{z}) - \sum_{k=0}^{n} \beta_k b_{k,n}(\bar{z}) \right)^2 d\bar{z} \]  

(10)

subject to \( b_k \in [0, 1] \forall k = 0, 1, ..., n \)

which can be solved using numerical techniques.

Bernstein polynomials can be implemented in stochastic logic using only an adder and a MUX [17]. Consider an adder with \( n \) inputs, each one a stochastic bit stream \( Z_1, \ldots, Z_n \). Furthermore, let each bit stream be independent and identically distributed, such that \( \bar{z} \equiv \bar{z}_i = \bar{z}_j \forall i, j \). Then, at a particular time \( t \), the adder will be adding \( n \) bits, each one being ‘1’ with probability \( \bar{z} \). Therefore, for their sum \( V \) to be a particular value \( k \) requires that \( k \) bits are ‘1’ and \( n-k \) bits are ‘0’. The probability of this occurring is \( \binom{n}{k} \bar{z}^k (1 - \bar{z})^{n-k} \). Connecting the adder’s output to the select line of a MUX whose inputs are equal to the Bernstein coefficients results in the Bernstein polynomial in (6).

3 Stochastic Logic TDR Circuit Design

The stochastic logic TDR implemented in this work is shown in Figure 4. The design is composed of three parts to provide input weight, compute the non-linear activation function, and hold the reservoir state. The input weighting stage takes in an analog signal, converts it to a digital signal using an analog-to-digital (A2D) converter, and converts that to a stochastic bit stream using a binary-to-stochastic (B2S) converter. In this design, the number

ACM J. Emerging Technologies in Computing.
of bits in the linear feedback shift registers (LFSR) in each B2S is equal to the number of bits in the binary representation of the input \( q \). Each timestep the B2S compares \( q \) to the LFSR’s current value and produces one bit of the stochastic representation of \( q \). The stochastic representation of the input is then multiplied by the input weight using an XNOR gate, as discussed in the Section 2.2. Then, the signal is mixed with the delayed reservoir state and added to the input bias using MUXes. The non-linear node estimates the non-linear activation function \( f(s) \) using Bernstein polynomials. Shift registers are used to delay the non-linear node’s input in order to create multiple statistically independent copies of the same stochastic bit stream. In this design, the activation function implemented is

\[
f(\bar{s}) = \sin(\gamma \bar{s}),
\]

where \( \gamma \) is a frequency term. However, recall that Bernstein polynomials map the unit interval to the unit interval. By definition, \( \bar{s} \) ranges from \([-1, +1]\), and the \( \sin \) function also ranges from \([-1, +1]\). In general, any function to be implemented by a Bernstein polynomial has to be shifted and scaled so that the portion of it that is used lies entirely in the unit square. In the case of \( \sin(\gamma \bar{s}) \), this is achieved by transforming the function as

\[
f(\bar{s}) = \frac{f(\Delta s \bar{s} - 0.5) - f_{min}}{f_{max} - f_{min}},
\]

where \( \Delta s \) is the domain of interest, \( f_{max} \) is the maximum of the function on \([-\Delta s/2, \Delta s/2]\), and \( f_{min} \) is the minimum of the function on \([-\Delta s/2, \Delta s/2]\). For the function \( f(\bar{s}) \), this results in the dotted curve in Figure 5. Also shown is the stochastic logic approximation using Bernstein polynomials with \( L = 1000 \) and \( n = 5 \). Notice that the features of the curve around \( s = 0 \) and \( s = 1 \) are not reproduced well by this approximation but could be by increasing \( n \). However, it was found that the approximation, which is similar to a logistic sigmoid function, works well for the benchmarks explored in this work.

After the activation function is computed, the reservoir node \( x_i \) is converted back to a binary number using a stochastic-to-binary (S2B) converter and then placed in a shift register which holds the entire reservoir state \( x \). Although the states could be stored in their stochastic representation, storing them as binary values is more area-efficient since \( L >> q \). Note that a control block is also included in Figure 4 to emphasize that the sample-and-hold circuit (inside the A2D), the B2S, and the S2B require a state machine when implemented in hardware. The shift register serves as the delay line shown in Figure 2. Note that training was not the focus of this work and performed using a non-stochastic implementation of Eq. (2).

Next is the task of choosing the design parameters \( a \) and \( \gamma \). One way is to look at application-dependent metrics such as accuracy, specificity, sensitivity, mean squared error, etc., and see how they vary over the parameter space via, e.g. a grid search. Another way is to use metrics that capture features such as the reservoir’s short-term memory capacity, ability to linearly separate input data, capability of mapping similar inputs to similar reservoir states (generalization) and different inputs to distant reservoir states (separation). These types of application-independent metrics provide more insight into the effects of different parameter choices on the TDR’s computing power than metrics like accuracy. This work makes use of such metrics: kernel quality (KQ) and generalization rank (GR) [21]. KQ is calculated by driving the reservoir with \( H \) random input streams of length \( m \). At the end of each sequence, the reservoir’s final state vector is inserted as a column into an \( H \times H \) state matrix \( X \). Then, KQ is equal to the rank of \( X \). It is desired to have \( X \) be full rank, meaning that different inputs map to different reservoir states. However, note that the number of training patterns is usually much larger than \( H \), so if \( \text{rank}(X) = H \), it doesn’t mean that any training dataset can be fit exactly. In fact, exact fitting, or overfitting, is generally bad, since it means that the TDR (or any machine learning algorithm) will not generalize well to novel inputs. Therefore, another metric, GR, is used to measure the TDR’s generalization capability. GR is calculated in a similar way, except that all of the input vectors are identical except for some random noise. GR is an estimate of the Vapnik-Chervonenkis dimension [21], which is a measure of learning capacity. A low GR is desirable. Therefore, to achieve good performance, the difference KQ-GR should be maximized.
Figure 6 shows the KQ and GR metrics for the stochastic logic TDR with $L = n = \infty$. The values are normalized to $H$ and are averaged over 10 runs. In each subplot, the size of the reservoir is $H = 50$ and $m = 50$. KQ (Figure 6(a)) is close to 0 for $\alpha = 0$. When $\alpha = 0$, the TDR does not accept any new inputs, so if the initial TDR state is all zeros, then the final state matrix will be a zero matrix, which has a rank of zero. For larger $\alpha$ values, KQ becomes non-zero. When $\gamma$ is small, the activation function is approximately linear, which leads to a smaller KQ. In fact, it
is likely that the TDR operates in the deterministic phase for $\gamma < 1$. As $\gamma$ becomes larger, KQ becomes equal to $H$. This is because the non-linearity of the activation function increases with $\gamma$ and results in the TDR operating within the chaotic regime. The GR metric (Figure 6(b)) has similar behavior, though recall that a low GR value is desirable. When the difference KQ-GR is taken (Figure 6(c)), a small region of optimal $\alpha$ and $\gamma$ is observed. If $\alpha$ is too large, then the TDR will have no memory; and if $\alpha$ is too small, then it will ignore inputs. Furthermore, if $\gamma$ is too large, then the TDR will overfit the training data; and if $\gamma$ is too small then the TDR will not have enough dynamic behavior. In practice, the optimal parameter values will have some application dependence. For our simulation work, parameter values of $\alpha = 0.2$ and $\gamma = 2$ were determined empirically to be the best for the studied benchmarks. However, from Figure 6(c), this parameter choice was expected to be suboptimal. Therefore, while one can generally consider such metrics such as GR and KQ, one ought to optimize the behavior of the RC for a chosen set of applications.

![Fig. 6. Computational capability of TDR for $L = \infty$, $H = 50$. (a) KQ vs. $\alpha$ and $\gamma$. (b) GR vs. $\alpha$ and $\gamma$. (c) KQ-GR vs. $\alpha$ and $\gamma$.](image)

Next we studied the effect of the stochastic length $L$ on the TDR metrics. Intuitively, one would expect that a small value of $L$ would lead to both a large KQ and GR, since the variance introduced from the stochastic computation is $\propto 1/L$. This was indeed observed in the KQ and GR metrics for two cases (Figure 7). In the first case, each LFSR was only seeded at the beginning of the simulation. This resulted in KQ-GR equal to zero over all $L$ values, except $L = 1$, where the noise was not large enough to modify the stochastic representation. From the previous discussion, we see that KQ-GR will eventually become non-zero as $L \to \infty$. However, that would mean that the TDR may have to wait an impractical number of clock cycles for each calculation. Instead, the approach used in this work was to re-seed each PRNG for every reservoir node with a unique seed for that node. Although this does not eliminate stochastic noise, it does keep the effect of the noise approximately constant for each node. With re-seeding, KQ-GR is non-zero for reasonable $L$ values such as 100 and 1000.

4 RESULTS AND DISCUSSION

4.1 Simulation

The stochastic logic TDR proposed in this work was tested in simulation on two simple benchmarks: NARMA10 (regression) and sine vs. square wave discrimination (classification). NARMA10 is a standard benchmark used in RC research. Given a random vector $u \in [0, 0.5]^n$, the goal is to train the RC to compute

$$y^{(p+1)} = 0.3 y^{(p)} + 0.05 y^{(p)} \left[ \sum_{k=0}^{9} y^{(p-k)} \right] + 1.5 u^{(p)} u^{(p-9)} + 0.1$$

(13)
Fig. 7. KQ and GR vs. $L$ in the stochastic logic TDR. Results are shown for the cases where the PRNG is not (no seed) and is (with seed) re-seeded for each reservoir node.

In this work, the TDR was trained on a set of 1000 points and tested on the subsequent 1000 points of the function. Figure 8 shows the normalized mean square error (NMSE) of the TDR for the test data. The NMSE is calculated as

$$NMSE = \frac{\sum_{p}(y^{(p)} - \hat{y}^{(p)})^2}{\sum_{p}(y^{(p)} - \langle y \rangle)^2}$$

(14)

where $\langle \cdot \rangle$ is the arithmetic mean. The plot shows an average over 10 runs with error bars indicating the standard deviation. It is observed that the NMSE is much larger than the “ideal” case ($L = \infty$) until $L$ becomes very large $>1 \times 10^4$. Such a large value of $L$ would give the TDR a prohibitively large latency and may only be feasible if the time constant of the input signal is very large, that is the input changes slowly. It is possible to improve the NMSE by adding more reservoir nodes, which can be observed as $H$ changes from 50 to 100. However, in a digital implementation, each new node requires additional hardware to store the additional component of the reservoir state. This could become costly if $H$ is very large.

Fig. 8. NARMA10 benchmark NMSE vs. $L$ using stochastic logic TDR for reservoir sizes of $H = 10$ and 100. Lines marked $L = \infty$ correspond to ideal implementations with no stochastic noise.
To test its performance on a time-series binary classification task, the stochastic logic TDR was trained to discriminate between sine and square wave signals. 20 signals of random wave sequences of 1000 points were used for training and another 20 signals were used for testing, as was the case for the NARMA10 benchmark. The results are shown in Figure 9(a). As expected, at very small values of \( L \), the TDR gives classification accuracies that are close to random chance. However, when \( L = 100 \), which is fairly small, the TDR performs approximately as well as the deterministic TDR. In fact, for \( H = 50 \), the accuracy of the stochastic TDR surpasses that of the deterministic design. At first, this seems counterintuitive, since smaller values of \( L \) result in more noise. However, the noise is actually acting as a regularizer in this case, reducing the stochastic TDR's ability to overfit.

To illustrate the effect of re-seeding the PRNG, Figure 9(b) depicts the same task for \( H = 50 \) under the two seeding conditions. As can be seen, the TDR without a re-seeded PRNG achieves an accuracy 30-40 percentage points lower than the TDR that does employ this trick.

![Figure 9(a) Sine vs. square wave discrimination accuracy vs. \( L \) using stochastic logic TDR for reservoir sizes of \( H = 50 \) and 100. Lines marked \( L = \infty \) correspond to ideal implementations with no stochastic noise. (b) Classification accuracy of \( H = 50 \) stochastic reservoir with and without a re-seeded PRNG.](image)

**4.2 FPGA Implementation**

Hardware experimentation in this work was performed on a Xilinx Spartan-6 XC6SLX75T board. Because of the poor performance of the simulated stochastic logic TDR on the NARMA10 task, we tested our FPGA implementation on the sine vs. square wave task. For these experiments, the feedback variable \( \alpha = 0.5 \), bias \( \theta = 0.1 \), and frequency term \( \gamma = 2 \). The TDR was trained on 1000 points and tested on an additional 1000 in each of 20 trials for with \( N = 50 \) and \( L = 32 \) (Figure 10). To increase the number of training and testing pairs evaluated, for each signal \( i \), a \( W_{\text{out}} \) vector was computed (Eq. (2)). This \( W_{\text{out}} \) was then used to test against all the other \((i-1)\) trials, \( \hat{y}^{(\ell)} = W_{\text{out}} \hat{x}^{(\ell)} \), affording 400 unique training/testing pairs. The average testing accuracy was 90.0% and the maximum was 97.9%.
Figure 10 shows the classification accuracy for several values of $H$ and $L$. Each point represents 400 train/test pairs. For $H = 40$ and $H = 50$, the circuit with larger values of $L$ could not fit on the Xilinx board, because of the way the reservoir output is stored before being transmitted. These larger reservoirs appear to perform better, so future work will attempt to fix this limitation.

The output weights $W_{out}$ are calculated for each trial based on each training signal separately. These are shown in Figure 12 for the trials of $H = 50$ and $L = 32$. Since the output weights are trained to generalize a given task, it is expected that the individual weight values will be similar across training instances. When the $W_{out}$ matrices
were averaged to create a new output weight matrix, the new testing accuracy was 93.4%, an increase from using a single training signal’s trained weights. Table 1 shows the average test accuracy for several values of $N$ and $L$, without and with the trained $W_{out}$ averaging. In all cases, the accuracy was increased by around 2 percentage points. Alternatively, we concatenated all the training signals as a single training signal. The resulting network accuracy was comparable to the averaged $W_{out}$ approach.

Table 1. Comparison of average test accuracy without and with $W_{out}$ averaging.

<table>
<thead>
<tr>
<th>N</th>
<th>L</th>
<th>Average accuracy</th>
<th>Accuracy with $W_{out}$ averaging</th>
<th>Accuracy with concatenated training sets</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>16</td>
<td>0.8119 ± 0.0237</td>
<td>0.8199 ± 0.0148</td>
<td>0.8294 ± 0.0152</td>
</tr>
<tr>
<td></td>
<td>32</td>
<td>0.8643 ± 0.0308</td>
<td>0.8919 ± 0.0291</td>
<td>0.8938 ± 0.0287</td>
</tr>
<tr>
<td></td>
<td>64</td>
<td>0.8501 ± 0.0271</td>
<td>0.8598 ± 0.0235</td>
<td>0.8629 ± 0.0232</td>
</tr>
<tr>
<td></td>
<td>128</td>
<td>0.8156 ± 0.0218</td>
<td>0.8337 ± 0.0193</td>
<td>0.8280 ± 0.0209</td>
</tr>
<tr>
<td>30</td>
<td>16</td>
<td>0.8281 ± 0.0292</td>
<td>0.8491 ± 0.0169</td>
<td>0.8453 ± 0.0178</td>
</tr>
<tr>
<td></td>
<td>32</td>
<td>0.8990 ± 0.0220</td>
<td>0.9135 ± 0.0190</td>
<td>0.9159 ± 0.0170</td>
</tr>
<tr>
<td></td>
<td>64</td>
<td>0.8707 ± 0.0261</td>
<td>0.8810 ± 0.0241</td>
<td>0.8746 ± 0.0211</td>
</tr>
<tr>
<td></td>
<td>128</td>
<td>0.8636 ± 0.0250</td>
<td>0.8759 ± 0.0193</td>
<td>0.8722 ± 0.0162</td>
</tr>
<tr>
<td>40</td>
<td>16</td>
<td>0.8738 ± 0.0334</td>
<td>0.8905 ± 0.0116</td>
<td>0.8984 ± 0.0111</td>
</tr>
<tr>
<td></td>
<td>32</td>
<td>0.9018 ± 0.0274</td>
<td>0.9366 ± 0.0154</td>
<td>0.9366 ± 0.0150</td>
</tr>
<tr>
<td></td>
<td>64</td>
<td>0.9136 ± 0.0209</td>
<td>0.9236 ± 0.0181</td>
<td>0.9221 ± 0.0175</td>
</tr>
<tr>
<td>50</td>
<td>16</td>
<td>0.8861 ± 0.0447</td>
<td>0.9264 ± 0.0105</td>
<td>0.9264 ± 0.0093</td>
</tr>
<tr>
<td></td>
<td>32</td>
<td>0.9000 ± 0.0423</td>
<td>0.9335 ± 0.0167</td>
<td>0.9420 ± 0.0143</td>
</tr>
</tbody>
</table>

A major attraction of stochastic logic is the reduction in logic gates required for performing calculations. Tables 2 and 3 show the number of configurable logic blocks, called slices, that were utilized according to the Xilinx ISE Place-and-Route report, excluding TX/RX and output storage. An occupied slice contains four registers or LUTs.
Higher $N$ values require a longer delay register, leading to both longer calculation times and more occupied slices (Table 2). The stochastic length $L$ affects the time taken for calculations. It also affects the circuitry in this implementation (Table 3). Increasing $L$ from 16 to 128 adds about 20 slice registers to the design because larger counters are needed. This portion is expected to increase at the rate $\log_2(L)$. The explored configurations took 1-2% of the available slices, when not accounting for the UART module and registers used to store the reservoir output values. The storage of output values takes up most of the slices on the FPGA board, limiting the size of the reservoir in this implementation.

**Table 2. Slice usage of Stochastic TDR with $L$ as circuit input**

<table>
<thead>
<tr>
<th>$N$</th>
<th>Slice Registers</th>
<th>Slice LUTs</th>
<th>Occupied Slices</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>439</td>
<td>540</td>
<td>195</td>
</tr>
<tr>
<td>30</td>
<td>469</td>
<td>552</td>
<td>214</td>
</tr>
<tr>
<td>40</td>
<td>488</td>
<td>575</td>
<td>210</td>
</tr>
<tr>
<td>50</td>
<td>544</td>
<td>635</td>
<td>249</td>
</tr>
</tbody>
</table>

Available slices: 93296 46648 11662

**Table 3. Slice usage of Stochastic TDR with $L$ hardcoded**

<table>
<thead>
<tr>
<th>$N$</th>
<th>$L$</th>
<th>Slice Registers</th>
<th>Slice LUTs</th>
<th>Occupied Slices</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>16</td>
<td>367</td>
<td>321</td>
<td>109</td>
</tr>
<tr>
<td>32</td>
<td>373</td>
<td>332</td>
<td>115</td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>379</td>
<td>336</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td>128</td>
<td>385</td>
<td>351</td>
<td>118</td>
<td></td>
</tr>
</tbody>
</table>

| 30  | 16  | 397             | 331        | 114             |
| 32  | 403 | 346             | 121        |
| 64  | 409 | 348             | 117        |
| 128 | 415 | 367             | 121        |

| 40  | 16  | 416             | 352        | 113             |
| 32  | 422 | 363             | 120        |
| 64  | 428 | 372             | 119        |
| 128 | 434 | 387             | 124        |

| 50  | 16  | 446             | 363        | 117             |
| 32  | 452 | 377             | 122        |
| 64  | 458 | 378             | 127        |
| 128 | 464 | 401             | 149        |

### 4.3 Discussion and Future Direction

We have shown that an FPGA implementation of a stochastic logic TDR is a viable method for sine vs. square wave classification. Without fully optimizing the TDR parameters, we achieved average classification accuracy of 90.0% for a reservoir with $N = 50$ and $L = 32$.

By using a Bernstein polynomial as the non-linear node of the reservoir, any activation function can be approximated. This gives flexibility to the design without adding circuitry and calculation time for floating point calculations. For example, a $\sin^2$ function instead of $\sin$ function may give better results for a particular application. Only the Bernstein coefficients $\beta_k$ need to be changed.

We have introduced and explored the effects of reseeding the PRNGs for the stochastic logic TDR. Without the re-seed, the $(KQ - GR) = 0$ over all $L$; whereas, applying this technique, the $(KQ - GR)$ metric becomes non-
zero at small $L$ by reducing the noise in the reservoir algorithm. This can lead to a significant increase in accuracy at lower $L$ values as shown in Figure 9(b).

A further area to explore is the effect of the LFSRs. Currently a separate LFSR is used for each binary-to-stochastic converter, each starting at its own seed value. Sharing LFSRs between S2B converters would decrease the board area required, but may introduce too much dependence between stochastic streams.

To fit the stochastic logic TDR design on the Xilinx Spartan-6 board, some circuit additions were made. This included the addition of a universal asynchronous receiver transmitter (UART) module. Because of the way inputs and outputs are loaded and stored on the board, the values of $N$ and $L$ available are limited. Most of the board area was used in storing the reservoir states before output. Future work would implement a different communication format, opening up more area of the board. All of the training in this work was performed batch-wise in Matlab. Further work would involve developing an onboard, online training method. This would bring the process from sensor to decision onto the FPGA.

Averaging the $W_{\text{out}}$ vectors from multiple training sets led to higher classification accuracy. This showed the possibility of using an average of trained sets of weights to increase accuracy. The average of twenty trained weight vectors gave similar performance to using the concatenation of training sets to train a single weight vector. This indicates multiple training approaches may achieve comparable test results.

Target applications of this design are size, weight, and power (SWaP) constrained platforms as found in embedded systems or edge/fog computing processors and applications, such as airborne or remote sensing applications. While specific power requirements were not measured at this stage, this proof of concept illustrates an approach to artificial neural network (ANN) implementation, in our particular case a TDR, which dramatically reduces the circuitry required for floating point matrix multiplication, which is ubiquitous in ANNs. Precision of the calculations can be adjusted by varying the stochastic length $L$. Increasing $L$ increases the time requirement per calculation but will ideally not change the hardware requirements. This now allows for design of systems that can dynamically optimize the trade-off between calculation speed and precision for different applications.

5 CONCLUSIONS

This paper presents and demonstrates a stochastic logic time delay reservoir design implemented in FPGA hardware. The reservoir network approach is analyzed using a number of metrics, such as kernel quality, generalization rank, and performance on simple benchmarks. The use of a Bernstein polynomial as the non-linear node allows any activation function to be approximated, adding flexibility to the design. A novel re-seeding method is introduced to reduce the adverse effects of stochastic noise. This method may also be implemented in other stochastic logic reservoir computing designs, such as echo state networks. Benchmark results indicate that the proposed design performs well on noise-tolerant classification problems, but more work needs to be done to improve the stochastic logic time delay reservoir’s robustness for regression problems. Further research will be done to increase the resource efficiency of our FPGA hardware implementation and apply the TDR to more computationally complex tasks.

ACKNOWLEDGMENTS

This material is based upon work supported by the Air Force Office of Scientific Research (AFOSR) under award number FA9550-15RICOR122. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author and do not necessarily reflect the views of AFRL. The material and results presented in this paper have been cleared for public release, unlimited distribution (Case Number 88ABW-2017-6271).

REFERENCES
An FPGA Implementation of a Time Delay Reservoir Using Stochastic Logic


To whom it may concern:


This paper adds an FPGA implementation of the time delay reservoir algorithm (see Section 4.2). Several experiments were performed on a Xilinx Spartan FPGA (Figures 10, 11, 12 and Tables 1, 2, 3). In addition, simulations have been run exploring the testing accuracy with the re-seeded PRNG (Figure 9.b). The Discussion (Section 4.3) and Conclusions (Section 5) have also been updated.

We feel that this adds significant value to the research and enough new material to be considered for publication in the JETC Special Issue.

Lisa Loomis
Dr. Cory Merkel
Nathan McDonald
Design of a Time Delay Reservoir Using Stochastic Logic: A Feasibility Study

Cory Merkel
Information Directorate
Air Force Research Laboratory
Rome, NY 13441
Email: cory.merkel.1@us.af.mil

Abstract—This paper presents a stochastic logic time delay reservoir design. The reservoir is analyzed using a number of metrics, such as kernel quality, generalization rank, performance on simple benchmarks, and is also compared to a deterministic design. A novel re-seeding method is introduced to reduce the adverse effects of stochastic noise, which may also be implemented in other stochastic logic reservoir computing designs, such as echo state networks. Benchmark results indicate that the proposed design performs well on noise-tolerant classification problems, but more work needs to be done to improve the stochastic logic time delay reservoir’s robustness for regression problems.

Keywords—Reservoir computing, time delay reservoir, stochastic logic, artificial neural networks.

I. INTRODUCTION

Reservoir computing (RC) is proving to be a powerful machine learning technique for regression, classification, and forecasting of time series data. Introduced in the early 2000s by Jaeger [1] and Maass [2], RC is a type of neural network with an untrained recurrent hidden layer called a reservoir. A major computational advantage of RC is that the output of the network can be trained on the reservoir states using simple regression techniques, without the need for backpropagation. In the last decade and a half, RC has been successful in a number of wide-ranging applications domains such as image classification [3], biosignal processing [4], and optimal control [5]. In some domains, RC has outperformed state-of-the-art techniques and is often easier to implement than methods such as Kalman filtering or long short term memory. Beyond its computational advantages, one of the main attractions of RC has previously been used to implement ESNs [11, 12]. In this work, we explore the feasibility of implementing TDRs with delayed feedback [8]. A common thread among all of these implementations is that they are analog and some, such as the photonic implementation, are still large prototypes that have yet to be integrated into a chip. Aside from the higher cost and design effort for analog implementations, they are much more susceptible to noise, especially in RC, where the system operates on the edge of chaos.

Besides a reduction in routing overhead, TDRs have two key advantages over ESNs and LSMs. First, adding additional neurons to the reservoir is trivial and amounts to increasing the delay in the feedback loop. Second, TDRs can use any dynamical system to implement their activation function and can easily be modeled via delay differential equations. This second point is particularly useful since it means that TDRs can be implemented using a variety of technologies. For example, in [6], Appeltant et al. used a Mackey-Glass oscillator, which models a number of physiological processes (e.g. blood circulation), as the non-linear node in a TDR. In [7], a TDR is demonstrated using coherently driven passive optical cavity. A TDR has also been implemented using a single XOR gate with delayed feedback [8]. A common thread among all of these implementations is that they are analog and some, such as the photonic implementation, are still large prototypes that have yet to be integrated into a chip. Aside from the higher cost and design effort for analog implementations, they are much more susceptible to noise, especially in RC, where the system operates on the edge of chaos.

Digital RC designs, and digital circuits in general, have much better noise immunity compared to analog implementations. There have been a number of digital designs proposed for ESNs and LSMs, such as [9], but digital TDR designs are presently scarce. One example is given in [10], where the authors have implemented a Mackey-Glass-type TDR on an FPGA. One of the challenges with digital implementations is that the area cost can be high due to the requirement of multipliers for input weighting and implementation of the activation function. This is especially true if high precision is required. However, not all applications require high precision. An alternative design approach to conventional digital logic is stochastic logic, where values are represented as stochastic bit streams and characterized by probabilities. Stochastic logic has previously been used to implement ESNs [11, 12]. In this work, we explore the feasibility of implementing TDRs with stochastic logic. To the best of the author’s knowledge, this is the first paper discussing TDR implementation with stochastic logic, and hopefully it will serve as a foundation for future research in this area.

The rest of this paper proceeds as follows: Section II provides background information on TDRs and stochastic logic. Section III presents the stochastic logic TDR designed in this work and discusses tuning of design parameters. Section IV discusses the performance of the proposed TDR design on two benchmark tasks: NARMA10 (regression) and sine/square...
wave discrimination (classification). Section V concludes this work.

II. BACKGROUND

A. Time Delay Reservoirs

RC makes use of a random recurrent neural network in order to regress, forecast, or classify time series data. The basic structure of an RC is shown in Figure 1. Time series inputs in the input layer are multiplied by a random weight matrix $s^{(p)} = W^{in} u^{(p)}$, and then used as inputs to the reservoir layer. Here, the index $p$ is used to denote a discrete timestep. Within the reservoir layer, there are a number of neurons (circles) that are connected with each other through a random weight matrix $x^{(p+1)} = f(W^{res} x^{(p)} + s^{(p)})$, where $f$ is an activation function. The state of the reservoir $x^{(p)}$ is then connected to an output layer via a third weight matrix $\hat{y}^{(p)} = c(W^{out} x^{(p)})$, where $c$ is the output function. In this work, $c$ is an identity function, such that the output is given directly by the product of the output weight matrix and the reservoir state. The output layer is trained such that the reservoir performs a particular function (e.g. regression, classification) of the inputs as

$$W^{out} = \arg \min W_{out} \frac{1}{2} \sum_{p=1}^{m_{\text{train}}} (y^{(p)} - \hat{y}^{(p)})^2$$

where $y^{(p)}$ is the expected output at timestep $p$ and $m_{\text{train}}$ is the size of the training set. In this work, this optimization problem is solved via regularized least squares:

$$W^{out} = (X^T X + \lambda I)^{-1} X^T Y,$$

where $\lambda$ is the regularization parameter, $I$ is the identity matrix, $X$, and $Y$ are the matrices composed of the reservoir states and the expected outputs corresponding the training set $U_{\text{train}}$, respectively. Note that the only parameters that are modified during training are the output weights $W^{out}$. The random input and reservoir layers serve to randomly project the input into a high-dimensional space which increases the linear separability of inputs. In addition, the recurrent connections of the reservoir provide a short-term memory that allows inputs to be integrated over time. This is critical to analyzing data based on its behavior over multiple timesteps.

A TDR (Figure 2) is a special type of RC that shares resources in time to reduce routing overhead. A single nonlinear node (shown as an opaque black circle) provides the activation function, analogous to the sigmoid and spiking functions in the ESN and LSM, respectively. The activation function can be any polynomial or transcendental function and is sometimes governed by a delay differential equation. At each timestep $p$, the reservoir’s input is sampled and held for a duration of $H$ smaller timesteps of duration $\Omega$. For each of the $H$ timesteps, the held input is multiplied by an input weight $w^{in}$ and then added to a bias term $\theta_i$. The weighted and biased input is added to the delayed state of the reservoir node, $x^{(p)}$, where $\tau \geq H$ is the delay of the feedback. In this work, $\tau = H + 1$. The sum is then fed back into the activation function. In this way, $H$ components make up the reservoir’s state corresponding to each sampled and held input. This approach is attractive because the hardware implementation usually consists of a simple circuit and a delay line without the routing overhead associated with ESs and LSMs. However, TDRs are more restricted in terms of their connectivity patterns and may require numerical simulation of DDEs when implemented in software. For an instantaneous activation function (e.g. $f$ settles within $\Omega$) and $\tau = H + 1$, a TDR has a unidirectional ring topology.

B. Stochastic Logic

The next section will present an efficient hardware implementation of a TDR using stochastic computing techniques. Stochastic logic was pioneered by von Neumann [13] half a century ago and was later adopted by the machine learning community to reduce hardware complexity, power, and unreliability [14, 15]. At the heart of stochastic computing is the stochastic representation of binary numbers. In a single-line bipolar [15] stochastic representation, a $q$-bit 2’s complement number $z \in \{-2^{q-1}, \ldots, -1, 0, 1, \ldots, 2^{q-1} - 1\}$ is mapped to a Bernoulli process $Z$ of length $L$ [16, 17]:

$$\bar{z} \equiv \Pr(Z_r = 1) = \frac{z + 2^{q-1}}{2^q - 1} = \frac{\bar{z} + 1}{2},$$

where the terms $\bar{z} \in [0, 1]$ and $\bar{\bar{z}} \in [-1, 1]$ are defined for convenience and $r = 1, 2, \ldots, L$ is an index into the stochastic bit stream. Converting from the binary to the stochastic representation can be achieved using a random number generator such as a linear feedback shift register (LFSR) and a comparator. If the random number is less than or equal to the value held in the register, then a logic 1 value is produced on the output. Otherwise, the comparator output is logic 0 [16]. As $L$ becomes large, $\Pr(Z_r = 1)$ approaches the value in (3). Converting from a stochastic representation back to a digital
number can be achieved by counting the number of 1’s and 0’s in the stream. By initializing the counter to zero, adding ‘1’ every time a ‘1’ is encountered in the stream and subtracting ‘1’ every time a ‘0’ is encountered, the final counter value will be the 2’s complement binary representation of the bit stream.

One advantage of a stochastic representation is that several mathematical operations become trivial to implement in hardware. For example, consider the logic function $Y_1 = g(I_1, I_2, \ldots, I_n)$, where each input $I_j$ to the function is mapped to a stochastic bit stream $Z^j$ and, therefore, the output is also a stochastic bit stream. The probability that the function evaluates to ‘1’ is given by

$$\Pr(Y_1 = 1) = \sum_{I_1, I_2} f(I_1, I_2, \ldots) \prod_{k=1}^n \Pr(Z^k = I_k),$$

which is a multivariate polynomial in $\pi_1, \pi_2, \ldots, \pi_n$ with integer coefficients and powers no greater than 1. Implementations for a number of stochastic logic operations are shown in Figure 3. Note that, in general, the implementation of stochastic logic operations will be different for unipolar representations. For example, in the case of a bipolar representation, multiplication is implemented using an XNOR gate (see Figure 3). However, for a unipolar representation, the same operation uses an AND gate. Other basic operations such as negation and weighted averaging are achieved using inverters and multiplexers, respectively.

In addition to the simple mathematical operations shown in Figure 3, it will also be necessary for the stochastic logic RC to implement a non-linear activation function. As indicated by (4), this is trivial if the activation function is a polynomial. However, if the activation function is not a transcendental function, then one way to implement it is to approximate it with a polynomial. Bernstein polynomials are a good choice, since they can approximate any function on the unit interval (or any other interval) with arbitrary precision, which was shown by Bernstein as part of a proof the Weierstrass approximation theorem [18, 19]. The Bernstein basis polynomials of degree $n$ are defined as [19]

$$b_{k,n}(\pi) \equiv \binom{n}{k} \pi^k (1-\pi)^{n-k}, \quad k = 0, 1, \ldots, n.$$  

A Bernstein polynomial of degree $n$ is defined as a linear combination of the $n^{th}$-degree Bernstein basis polynomials:

$$B_n(\pi) \equiv \sum_{k=0}^n \beta_k b_{k,n}(\pi)$$

The coefficients $\beta_k$ are called the Bernstein coefficients. Furthermore, the $n^{th}$-degree Bernstein polynomial for a function $f(\pi)$ is defined as

$$B_n(f; \pi) = \sum_{k=0}^n \binom{n}{k} \frac{f(k)}{n} b_{k,n}(\pi).$$

Bernstein showed that $B_n(f; \pi)$ approaches $f(\pi)$ uniformly on $[0, 1]$ as $n$ approaches infinity.

It can also be shown that the set of Bernstein basis polynomials $\{b_{k,n}\}$ of degree $n$ forms a basis for the space of power-form polynomials with real coefficients and degree no more than $n$. In other words, the power-form polynomial

$$p(\pi) = \sum_{i=0}^n a_i \pi^i$$

can be written in the form of (6). In [20], it is shown that the Bernstein coefficients can be obtained from the power-form coefficients as

$$\beta_k = \sum_{i=0}^k \binom{k}{i} \binom{n}{j}^{-1} a_i.$$  

It is important to note that if $f$ in (6) maps the unit interval to the unit interval, then $f(k/n)$ is also in the unit interval. Similarly, Qian et al. have proven that if $p$ in (8) maps the unit interval to the unit interval, then the Bernstein coefficients in (9) will also be in the unit interval. Coefficients in the unit interval are important because they can be represented stochastically.

In summary, any non-polynomial (polynomial) function that maps the unit interval to the unit interval can be approximated by (written in the form of) a Bernstein polynomial with coefficients that are also in the unit interval. To find the coefficients for non-polynomial functions, one may form the constrained optimization problem [17]:

$$\min_{\beta_k} \frac{1}{2} \int_0^1 (f(\pi) - \sum_{k=0}^n \beta_k b_{k,n}(\pi))^2 d\pi$$

subject to $\beta_k \in [0, 1] \forall k = 0, 1, \ldots, n$

which can be solved using numerical techniques.

Bernstein polynomials can be implemented in stochastic logic using only an adder and a MUX [17]. Consider an adder with $n$ inputs, each one a stochastic bit stream $Z_1, \ldots, Z_n$. Furthermore, let each bit stream be independent and identically distributed, such that $\pi = \pi_j \forall j$. Then, at a particular time $t$, the adder will be adding $n$ bits, each one being ‘1’ with probability $\pi$. Therefore, for their sum $V$ to be a particular value $k$ requires that $k$ bits are ‘1’ and $n-k$ bits are ‘0’. The probability of this occurring is $\binom{n}{k} \pi^k (1-\pi)^{n-k}$. Now, connecting the adder’s output to the select line of a MUX, with inputs equal to the Bernstein coefficients, results in the Bernstein polynomial in (6).

III. Stochastic Logic TDR Design

The stochastic logic TDR designed in this work is shown in Figure 4. The design is composed of three parts to provide input weight, compute the non-linear activation function, and hold the reservoir state. The input weighting stage takes in an
analog signal, converts it to a digital signal using an analog-to-digital (A2D) converter, and converts that to a stochastic bit stream using a binary-to-stochastic (B2S) converter. In this design, the number of bits in the LFSRs in each B2S is equal to the number of bits in the binary representation of the input, \(q\). The stochastic representation of the input is then multiplied by the input weight using an XNOR gate, as discussed in the last section. Then, the signal is mixed with the delayed reservoir state and added to the input bias using MUXes. The non-linear node estimates the non-linear activation function in the dotted curve in Figure 5. Also shown is the stochastic approximation using Bernstein polynomials with \(n = 5\) and \(L = 1000\). Notice that the features of the curve around \(\pi = 0\) and \(\pi = 1\) are not reproduced well by this approximation but could be by increasing \(n\). However, it was found that the approximation, which is similar to a logistic sigmoid function, works well for the benchmarks explored in this work.

After the activation function is computed, the reservoir node \(x_i\) is converted back to a binary number using a stochastic-to-binary (S2B) converter and then placed in a shift register which holds the entire reservoir state \(x\). Although the states could be stored in their stochastic representation, storing them as binary values is more area-efficient since \(L \gg q\). Note that a control block is also included in Figure 4 to emphasize the sample-and-hold circuit (inside the A2D), the B2S, and the S2B require a state machine when implemented in
hardware. However, all of the simulations in this work are behavioral and implemented in MATLAB, so this block wasn’t explicitly required. The shift register serves as the delay line shown in Figure 2. Note that training was not the focus of this work and performed using a non-stochastic implementation of (2).

Next is the task of choosing the design parameters $\alpha$ and $\gamma$. One way is to look at application-dependent metrics such as accuracy, specificity, sensitivity, mean squared error, etc., and see how they vary over the parameter space via, e.g., a grid search. Another way is to use metrics that capture features such as the reservoir’s short-term memory capacity, ability to linearly separate input data, capability of mapping similar inputs to similar reservoir states (generalization), and different inputs to distant reservoir states (separation). These types of application-independent metrics provide more insight into the effects of different parameter choices on the TDR’s computing power than metrics like accuracy. This work makes use of such metrics: Kernel quality (KQ) and generalization rank (GR) [21]. KQ is calculated by driving the reservoir with $H$ random input streams of length $m$. At the end of each sequence, the reservoir’s final state vector is inserted as a column into an $H \times H$ state matrix $X$. Then, KQ is equal to the rank of $X$. It is desired to have $X$ be full rank, meaning that different inputs map to different reservoir states. However, note that the number of training patterns is usually much larger than $H$, so if rank($X$) = $H$, it doesn’t mean that any training dataset can be fit exactly. In fact, exact fitting, or overfitting, is generally bad, since it means that the TDR (or any machine learning algorithm) won’t generalize well to novel inputs. Therefore, another metric, GR, is used to measure the TDR’s generalization capability. GR is calculated in a similar way, except that all of the input vectors are identical except for some random noise. GR is an estimate of the Vapnik-Chervonenkis dimension [21], which is a measure of learning capacity. A low GR is desirable. Therefore, to achieve good performance, the difference KQ-GR should be maximized.

Figure 6 shows the KQ and GR metrics for the stochastic logic TDR with $L = n = \infty$. The values are normalized to $H$ and are averaged over 10 runs. In each subplot, the size of the reservoir is $H = 50$, and $m = 50$. KQ is close to 0 for $\alpha = 0$. When $\alpha = 0$, the TDR does not accept any new inputs, so if the initial TDR state is all zeros, then the final state matrix will be a zero matrix, which has a rank of zero. For larger $\alpha$ values, KQ becomes non-zero. When $\gamma$ is small, the activation function is approximately linear, which leads to a smaller KQ. In fact, it is likely that the TDR operates in the deterministic phase for $\gamma < 1$. As $\gamma$ becomes larger, KQ becomes equal to $H$. This is because the non-linearity of the activation function increases with $\gamma$, and results in the TDR operating within the chaotic regime. The GR metric (Figure 6(b)) has similar behavior. When the difference KQ-GR is taken (Figure 6(c)), a small region of optimal $\alpha$ and $\gamma$ is observed. Values of $\alpha$ should be somewhere between 0 and 1. If $\alpha$ is too large, then the TDR will have no memory; and if $\alpha$ is too small, then it will ignore inputs. Furthermore, if $\gamma$ is too large, then the TDR will overfit the training data, and if $\gamma$ is too small then the TDR won’t have enough dynamic behavior. Also note that the optimal parameter values will have some application dependence. In this work, parameter values of $\alpha = 0.2$ and $\gamma = 2$ were determined empirically to be the best for the studied benchmarks. However, from Figure 6(c), it appears that this choice is suboptimal. Therefore, one should be cautious when using metrics such as GR and KQ and always consider the behavior of the RC for a chosen set of applications.

Studied next was the effect of the stochastic bit stream...
length $L$ on the TDR metrics. Intuitively, one would expect that a small value of $L$ would lead to both a large KQ and GR, since the variance introduced from the stochastic computation is $\propto 1/L$. Indeed, this is true. Figure 7 shows the KQ and GR metrics for two cases. In the first case (no seed), each LFSR was only seeded at the beginning of the simulation. This resulted in KQ-GR equal to zero over all $L$ values, except $L = 1$, where the noise wasn’t large enough to modify the stochastic representation. From the previous discussion, we see that KQ-GR will eventually become non-zero as $L \to \infty$. However, that would mean that the TDR may have to wait an impractical number of clock cycles for each calculation. Instead, the approach used in this work is to re-seed each PRNG for every reservoir node, with a unique seed for that node. Although this doesn’t eliminate stochastic noise, it does keep the effect of the noise approximately constant for each node. With re-seeding (Figure 7), KQ-GR is non-zero for reasonable $L$ values such as 100 and 1000.

IV. BENCHMARK RESULTS AND ANALYSIS

The stochastic logic TDR proposed in this work was tested on two simple benchmarks: NARMA10 (regression) and sine/square wave discrimination (classification). NARMA10 is a standard benchmark used in RC research. Given a random vector $u \in [0, 0.5]^m$, the goal is to train the RC to compute

$$y^{(p+1)} = 0.3y_i^{(p)} + 0.05y^{(p)} \sum_{k=0}^9 y^{(p-k)} + 1.5u^{(p)}u^{(p-9)} + 0.1.$$  (13)

In this work, the TDR was trained on a set of 1000 datapoints and tested on an additional 1000. Figure 8 shows the normalized mean square error (NMSE) of the TDR on the test data. The NMSE is calculated as

$$\text{NMSE} = \frac{\sum_p \left( y^{(p)} - \hat{y}^{(p)} \right)^2}{\sum_p \left( y^{(p)} - \langle y^{(p)} \rangle_{\text{train}} \right)^2},$$  (14)

where $\langle \cdot \rangle$ is the arithmetic mean, and $y_{\text{train}}$ is the vector of the entire training sequence. The plot shows an average over 10 runs, with error bars indicating the standard deviation. It is observed that the NMSE is much larger than the “ideal” case ($L = \infty$) until $L$ becomes very large (e.g. $1 \times 10^4$). Such a large value of $L$ would give the TDR a prohibitively large latency and may only be feasible if the time constant of the input signal is very large (i.e. the input changes slowly). It is possible to improve the NMSE by adding more reservoir nodes, which can be observed as $H$ changes from 50 to 100. However, in a digital implementation, each new node requires additional hardware to store the additional component of the reservoir state. This could become costly if $H$ is very large.

To test its performance on classification tasks, the stochastic logic TDR was trained to discriminated between sine and square wave signals. 1000 training and test cases were used, as was the case for the NARMA 10 benchmark. The training and test sequences were created by randomly interposing segments of sine waves into a square wave such that there was a 50% chance that any point in the sequence was part of a sine (or square) wave. The results are shown in Figure 9. As expected, at very small values of $L$, the TDR gives classification accuracies that are close to random chance. However, when $L$ is equal to 100, which is fairly small, the TDR performs approximately as well as the deterministic TDR. In-fact, for $H = 50$, the accuracy of the stochastic TDR surpasses that of the deterministic design. At first, this seems counterintuitive, since smaller values of $L$ result in more noise. However, the noise is actually acting as a regularizer in this case, reducing the stochastic TDR’s ability to overfit.

V. CONCLUSIONS AND FUTURE WORK

This work studied a novel TDR design that uses stochastic logic to perform weighting, biasing, and activation function operations. The design is more flexible than previous approaches as it allows any activation function to be implemented after it is properly shifted and scaled. Optimal design parameters are chosen based on kernel quality and generalization rank, and a method for reducing stochastic noise using re-seeding was proposed. The design was tested using the NARMA10 and sine/square wave discrimination benchmarks. Results indicate that high-precision benchmarks, such as NARMA10, do not perform well on a stochastic TDR due to random noise. However, for classification benchmarks, the stochastic TDR is more area efficient than previous design approaches. This paper provides a foundation for future research directions related to stochastic logic TDRs. Some potentially fruitful avenues include investigation of other activation functions (e.g.
Mackey-Glass), methods for reducing the complexity of B2S converters (i.e. removing expensive comparators and LFSRs), exploring methods for reducing stochastic noise, and investigation of emerging memory technologies for more efficient storage of reservoir states.

ACKNOWLEDGMENTS

The author is grateful to Nathan McDonald, Clare Thiem, Lisa Loomis, and Ashley Prater for proofreading the manuscript and providing helpful discussions.

The material and results presented in this paper have been CLEARED (Distribution A) for public release, unlimited distribution by AFRL, case number 88ABW-2016-6393. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author and do not necessarily reflect the views of AFRL or its contractors.

REFERENCES