CS 530, Fall 2013, Exam 1 Study Guide

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September 20, 2013

1 Chapter 1 and Appendix A Concepts and Problems

Know limiting factors in computer architectures:

- Power
- Energy
- Leakage
- Complexity
- Speed of light
- Amdahl's law

Make sure you know the reasons for these and their consequences.

Familiarize yourself with the concepts from the lectures and know how they fit together in various design combinations.

2 Chapter 2 and Appendix B Concepts and Problems

Know the memory hierarchy concepts (the lectures slides are a good reference): cache block, associativity, address mapping, ...

Make sure you know how to apply access time equation and Amdahl's law for computing memory performance and usefulness of various design decisions.

B.1 page B-60 (Appendix B)

B.1 part a

Using the equation on page 75:
Average access time = (1 miss rate) × hit time + miss rate × miss time = .95 × 1 + 0.05 × 105 = 6.2 cycles.

B.1 part b

Because of the randomness of the accesses, we first computed the probability of a hit. An access will be a hit, if it accesses data that is in cache. Because of the randomness, the probability is equal to the size of the cache divided by the size of the array.

$$\text{Hit rate} = \frac{64\text{ Kbytes}}{256\text{ Mbytes}} = \frac{1}{4000} = 0.00025.$$

Make sure you get the units right: 1 KB = 1000 B and 1 KiB = 1024 B. Similarly, there is a difference between MB and MiB.

We use the equation on page 75:
average access time = 0.00025 × 1 cycle + (1 0.00025) × 105 cycles = 104.974 cycles.

B.1 part c

Locality is crucial to cache operation. If the cache is switched off, the access time becomes 100 cycles. This is more than the average access time (part b above) 104.974 cycles with cache and no locality.

B.1 part d

Symbol list:

- L — loss due to use of cache
- G — gain due to use of cache
- t_{off} — access time if cache is switched off
- t_{on} — access time if cache is switched on
- m — miss rate

Access times under miss and hit scenarios:

- m fraction of accesses are misses and their access time is $t_{\text{off}} + L$
- $1 - m$ fraction of accesses are hits and their access time is $t_{\text{off}} - G$

So when we turn the cache on, we get average access time:

$$t_{\text{on}} = (1 - m) \times (t_{\text{off}} - G) + m \times (t_{\text{off}} + L)$$

The question to answer is for which m the cache is detrimental with $t_{\text{on}} \geq t_{\text{off}}$. After plugining into the above equation, we get

$$m \geq \frac{G}{G + L}$$

If $G = 99$ and $L = 5$, $m \geq \frac{99}{99+5} \approx 0.95$