D. EXERCISES

D Exercises

Exercise II.1 Show that Eq. II.3 (p. 41) can be rearranged to Eq. II.4 (p. 41).

Exercise II.2 Show that the Fredkin gate is reversible.

Exercise II.3 Show that the Fredkin gate implements $(a, 0, 1) \mapsto (a, a, \bar{a})$ (the "spy circuit").

Exercise II.4 Show how to use a single Fredkin gate to implement each of the NOT, OR, and FAN-OUT gates. (FAN-OUT copies its input value to two output wires.) Note! You cannot use FAN-IN or FAN-OUT in your implementations, only Fredkin gates.

Exercise II.5 Use the Fredkin gate to implement XOR. Minimize the number of Fredkin gates you use.

Exercise II.6 Give a truth table for a reversible gate that is not conservative (does not preserve the total number of 1s and 0s). It should have the same number of outputs as inputs.

Exercise II.7 Give a truth table for a 2-input / 2-output gate that is conservative but not reversible.

Exercise II.8 Show for the eight possible inputs that Fig. II.14 is a correct implementation of a 1-line to 4-line demultiplexer. That is, show in each of the four cases $A_1A_0 = 00, 01, 10, 11$ the bit X = 0 or 1 gets routed to Y_0, Y_1, Y_2, Y_3 , respectively. You can use a Boolean algebra proof, if you prefer.

Exercise II.9 Show that implementation of a J- \overline{K} flip-flop with Fredkin gates in Fig. II.24 is correct. A J- \overline{K} flip-flop has the following behavior:

 $\begin{array}{c|ccc} J & \bar{K} & behavior \\ \hline 0 & 0 & reset, Q \rightarrow 0 \\ 0 & 1 & hold, Q doesn't change \\ 1 & 0 & toggle, Q \rightarrow \bar{Q} \\ 1 & 1 & set, Q \rightarrow 1 \end{array}$



Figure II.24: Implementation of J- \bar{K} flip-flop. [adapted from Fredkin & Toffoli (1982)]

Exercise II.10 Show that the inverse of the interaction gate (Fig. II.20) works correctly. Hint: It only needs to work correctly for outputs that actually occur. Therefore, to invert a pq output, balls must be shot into outputs A and D simultaneously.

Exercise II.11 Use interaction gates (and constant inputs and garbage outputs, as necessary) to implement NOT, OR (inclusive or), and XOR (exclusive or).

Exercise II.12 Show that the realization of the Fredkin gate in terms of interaction gates (Fig. II.23) is correct, by labeling the inputs and outputs of the interaction gates with Boolean expressions of a, b, and c.