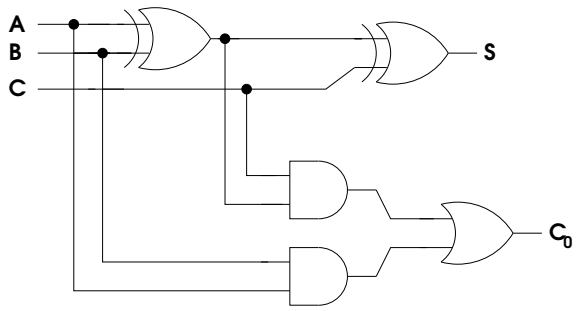
May 11, 2010 sylF10.tex

ECE 255 Introduction to Logic Design, Fall 2010



The figure is a logic diagram for a binary *Full Adder* implemented with two XOR (exclusive-OR) gates, two AND gates, and one OR gate. We'll define these gates early in the course. The shape of a gate in a schematic tells what kind it is: the two XORs are at the top; the two ANDs and the single OR are at the bottom. Each gate computes a binary-valued function of its two binary inputs. The Full Adder computes the sum of the three input bits A,B,C in binary arithmetic and outputs the answer as sum bit S and carry bit C_0 according to this *Truth Table*:

A	B	C	C_0	S	Equivalent decimal number
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	1	0	2
1	0	0	0	1	1
1	0	1	1	0	2
1	1	0	1	0	2
1	1	1	1	1	3

Instructor: Michael Thomason
Class: 9:05-9:55 MWF, Room C206 in the Claxton outpost.
Office Hours: 10:05-11:15 MWF, Room C316 (Often around at other times, but not guaranteed available.)
e-mail: *thomason@eecs.utk.edu* or *thomason@cs.utk.edu*

If you send e-mail, recognize its limitations. The volume of e-mail, including SPAM, is very large, so you have to expect delays. Also, e-mail isn't viable for detailed technical questions and answers: use the office hours or make an appointment on a timely basis. Grades on homework or exams will not be sent by email.

Labs: Open lab in Ferris Hall with weekly hours TBA. Each lab is described in detail (including the due-date) in a handout given in class, and your results are demonstrated to

GTA during lab hours. Labs use a printed circuit board that you can check out at the appropriate time in Ferris Hall and return later.

Note 1: CAD software for Xilinx Spartan 3e FPGA: details soon.

Note 2: Digilent Adept software: details soon.

Note 3: The labs are not optional. You must complete every lab to pass the course regardless of how well you do on the other work. The labs are individual assignments, not team projects.

Course Description

Catalog Description: Standard codes, number systems, base conversions, and computer arithmetic. Boolean algrbra, minimization and synthesis techniques for combinational and sequential logic. Use of VHDL for logic synthesis. Implementation of circuits using SSI, MSI, and LSI components. Includes Level 1 design projects which require lab work.

Required Text: Bound lecture notes for ECE 255 from Graphics Creations.

Topics (expect some real-time tuning and adjustments):

Intro. to logic design: What's it about? What're the goals? What tools are used in this course?

Boolean Algebra: operations and properties; manipulation of expressions

Truth Tables; canonical expressions

Intro. to CAD tools and VHDL as a language for logic design

Minimization; Karnaugh maps; "don't cares"; implicants (prime, essential)

Number systems; binary arithmetic

Combinational logic modules (adders, multiplexers, encoders and decoders); PLAs

Sequential logic; cross-coupled gates to make flip-flops; RS, T, D, and JK flip-flops

Flip-flop arrays (registers, counters)

Clocked (synchronous) sequential circuits; state diagrams of Mealy and Moore machines

Asynchronous sequential circuits; timing considerations and hazards [as time permits]

For your lab work, we must cover aspects of the Xilinx ISE design software, the Digilent Adept software, the Digilent BASYS board with its Xilinx Spartan3e FPGA, and some VHDL programming. You are responsible for all assignments: in class, in the lecture notes, in handouts, and in labs.

Prereq and Grading: ECE 255 is an introduction to logic design, not a course intended for people who already have a background in the topic. It is a 4-credit course with a lab.

Your course grade will be based on 500 points as follows.

- There will be three in-class exams (50 minute, closed book, no calculators or other electronics) for 100 points each. Exams will be spaced about evenly through the semester.
- There will be graded homework spread over several assignments and averaged to 100 points. Homework to turn in for grading will be handed out in class with a specific due-date and must get grade 0 if late.
- The lab assignments, verified by the GTAs by specific due-dates, will be averaged for the last 100 points.

The course letter grade will be based on the percentage (rounded to uint8) of points earned out of the 500 points possible: 90 to 100% A- to A, 80 to 89% B- to B+, 70 to 79% C- to C+, 60 to 69% D, $<$ 60% F. There *may* be a curve downward (like 79% for B-) depending on the class distribution, but this is not likely. The breakpoints for + and - will depend on the class distribution.

Students who have a disability that requires accomodation should make an appointment with the Office of Disability Services to discuss specific needs.