**Resistance**

\[ R = \frac{\rho}{t} \left( \frac{1}{w} \right) \text{ ohms} \]

where

\( \rho = \text{resistivity}, \ t = \text{thickness}, \ l = \text{conductor length}, \ w = \text{conductor width} \)

Also can use

\[ R = R_s \left( \frac{1}{w} \right) \]

where

\( R_s = \text{sheet resistance (}\Omega/\text{sq.}) \)

Independence from \( \frac{1}{w} \) is obtained by measuring sheet resistance by the "square":

1 rectangular block
\[ R = R_s(l/w) \ [\Omega] \]

4 rectangular blocks
\[ R = R_s(2l/2w) = R_s(l/w) \ [\Omega] \]
Typical sheet resistances for conductors:

<table>
<thead>
<tr>
<th>Material</th>
<th>SHEET RESISTANCE [Ω/SQUARE]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min.</td>
</tr>
<tr>
<td>Intermetal (metal1-metal2)</td>
<td>0.05</td>
</tr>
<tr>
<td>Top-metal</td>
<td>0.03</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>15</td>
</tr>
<tr>
<td>Silicide</td>
<td>2</td>
</tr>
<tr>
<td>Diffusion ($n^+,p^+$)</td>
<td>10</td>
</tr>
<tr>
<td>Silicided diffusion</td>
<td>2</td>
</tr>
<tr>
<td>$n$-well</td>
<td>1k</td>
</tr>
</tbody>
</table>
Delay

Long wire ⇒ distributed RC line

First-order approximation:

\[ \text{delay} = \frac{r \times c \times l^2}{2} \]

where

- \( r \) = resistance per unit length
- \( c \) = capacitance per unit length
- \( l \) = length of the wire

**Important fact** ⇒ interconnect delay does not scale with \( \lambda \), it is constant. When \( \lambda \) decreases, \( R \) increases and \( C \) decreases, resulting in delay constant.

Inserting a buffer in a long resistance line can be advantageous.

For a poly run = 2mm length,

- \( r = 20 \ \Omega/\mu\text{m} \)
- \( c = 4 \times 10^{-4} \ \text{pF}/\mu\text{m} \)

\[ 2\text{mm delay} = \frac{20 \times 4 \times 10^{-4} \times 2^2}{2} = 16 \ \text{ns} \]

If broken into two 1mm sections, then delay of each section = 4ns. Add a buffer with delay = 1ns and total delay becomes \( 4 + 1 + 4 = 9\text{ns} \).
Typically, resistive effects of interconnect much more important than capacitive effects since capacitance tends to be dominated by the gate capacitances.

MOSFET load capacitance $>>$ wire capacitance [unless DSM (deep submicron ($\leq 0.25\mu m$) CMOS technology)]

So, if we decrease interconnect resistance, then we reduce overall propagation delay between driver and load.

Reduce interconnect resistance by using metal, increasing the width of the interconnect.

Usually just want delay ($RC$), where $R$ is the resistance of the interconnect and $C$ is the total of all the capacitive loads.
Stage Ratio - Delay Optimization

To drive a large load, do not just want to make one large driver

large transistors represent a large load back to internal circuitry

Want to drive the load with a series of progressively larger drivers

Each driver (inverter) larger than preceding driver by stage ratio "a".

Let $C_g$ be gate load of first driver which is minimum size.

Then, $C_{gN}$ will be $C_g \times a^N$ and want

$$C_g a^n \leq C_L, \quad \text{[Note: } n = N + 1\]$$
to guarantee that none of capacitances internal to the chain of inverters exceed $C_{\text{load}}$. For example, if $C_{gN} \geq C_{\text{load}}$, why we would need the n-th inverter at all!

So when the condition $C_g a^n \leq C_L$ is set equal we have

$$a^n = \frac{C_L}{C_g}.$$ 

Question: What value of "a" will lead to minimum delay? What value of "n"? If we find one, we can compute the other.

Delay through each stage is approximately $a \times t_d$ where $t_d$ is the delay through a minimum-sized inverter driving another minimum-sized inverter.

Total Delay $= n \times a \times t_d$

We know

$$a^n = \left(\frac{C_L}{C_g}\right),$$

so

$$a = \left(\frac{C_L}{C_g}\right)^{1/n}$$

Substituting,

$$\text{Total Delay} = n \left(\frac{C_L}{C_g}\right)^{1/n} t_d$$

To find optimum value for n, differentiate and set equal to zero.

If we do, then we find
\[ n_{\text{opt}} = \ln\left(\frac{C_L}{C_g}\right) \]

Once we know \( n_{\text{opt}} \), find \( a_{\text{opt}} \)

\[
a^n = \left(\frac{C_L}{C_g}\right)
\]

\[
a^{\ln\left(\frac{C_L}{C_g}\right)} = \frac{C_L}{C_g}
\]

Take the natural log (i.e., \( \ln \)) of both sides:

\[
\ln\left(\frac{C_L}{C_g}\right) \times \ln(a) = \ln\left(\frac{C_L}{C_g}\right)
\]

\[
\ln(a) = 1
\]

\[
\Rightarrow a = e^{1} \approx 2.7
\]

A more detailed analysis shows that the intrinsic output capacitance of the inverter will affect this ratio.

\[
a_{\text{opt}} = \exp\left(\frac{k + a_{\text{opt}}}{a_{\text{opt}}}\right)
\]

where

\[
k = \frac{C_{\text{drain}}}{C_{\text{gate}}}
\]
External Conditions which can affect delay

a) Operating Temperature
b) Supply Voltage
c) Process Variation

Drain current is proportional to $T^{(-1.5)} \Rightarrow$ As temperature is increased, drain current is reduced for a given set of operating conditions, delay increases ↑

The temperature of the die is what counts, this is expressed as

$$T_j = T_a + \theta_{ja} \times P_d$$

where

$T_a \equiv$ ambient Temperature (°C)
$\theta_{ja} \equiv$ package thermal impedance (°C/watt)
$P_d \equiv$ power dissipation

Typical values for $\theta_{ja}$ range from 35 to 45 (°C/watt), depending on chip package

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Pin Count</th>
<th>$\theta_{ja}$ still air</th>
<th>$\theta_{ja}$ 300 ft/min.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plastic J-Leaded Chip Carrier</td>
<td>44</td>
<td>45</td>
<td>35</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>68</td>
<td>38</td>
<td>29</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>84</td>
<td>37</td>
<td>28</td>
<td>°C/W</td>
</tr>
<tr>
<td>Plastic Quad Flatpack</td>
<td>100</td>
<td>48</td>
<td>40</td>
<td>°C/W</td>
</tr>
<tr>
<td>Very Thin (1.0mm) Quad Flatpack</td>
<td>80</td>
<td>43</td>
<td>35</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ceramic Pin Grid Array</td>
<td>84</td>
<td>33</td>
<td>20</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ceramic Quad Flatpack</td>
<td>84</td>
<td>40</td>
<td>30</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
**Parts** usually characterized for different temperature ranges:

- Commercial: 0° to 70° C
- Industrial: −40° to 85° C
- Military: −55° to 125° C

Voltage also affects device speed:
- voltage increases ↑, drain current increases, delay decreases ↓

Typically characterize device around a power supply tolerance

<table>
<thead>
<tr>
<th>Power Supply Voltage Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
</tr>
<tr>
<td>Industrial</td>
</tr>
<tr>
<td>Military</td>
</tr>
</tbody>
</table>

**Process Variations** also affect delay — wafer fabrication is a long series of chemical operations, variations in diffusion depth, dopant densities, oxide/diffusion geometry variations can cause transistor switching speeds to vary from wafer batch to wafer batch, wafer to wafer and even on the same wafer.
Transistors typically characterized as "fast", "nominal", and "slow". Need SPICE transistor models for these cases.

However, variations between \( n \)-MOS-speeds and \( p \)-MOS-speeds can be independent so one can obtain "four corners" model

\[
\begin{array}{c|c}
\text{slow } n\text{MOS} & \text{fast } n\text{MOS} \\
\text{fast } p\text{MOS} & \text{fast } p\text{MOS} \\
\hline
\text{slow } n\text{MOS} & \text{fast } n\text{MOS} \\
\text{slow } p\text{MOS} & \text{slow } p\text{MOS} \\
\end{array}
\]

When characterizing for high speed, also want to use lowest temperature, highest voltage.

When characterizing for "slow" case, want highest temperature, lowest voltage.

<table>
<thead>
<tr>
<th>CMOS Digital Systems Checks (Commercial)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PROCESS</td>
</tr>
<tr>
<td>Fast-( n )/ fast-( p )</td>
</tr>
<tr>
<td>Slow-( n )/ slow-( p )</td>
</tr>
<tr>
<td>Slow-( n )/ fast-( p )</td>
</tr>
<tr>
<td>Fast-( n )/ slow-( p )</td>
</tr>
</tbody>
</table>
Power Dissipation

Power Dissipation has three components:

1. Static
2. Dynamic
3. Short Circuit

For traditional CMOS design, static dissipation is limited to the leakage currents in the reversed-biased diodes formed between the substrate (or well) and source/drain regions. But in some DSM CMOS technology subthreshold leakage tends to also contribute significant static dissipation. Subthreshold leakage increases exponentially as threshold voltage decreases; i.e., lower $V_T$ ($V_{Th}$ and $|V_{Tp}|$) CMOS technology has more static power dissipation (due to subthreshold leakage) than higher $V_T$ technology.

Static power dissipation can be extremely small:

1 inverter @ 5V ⇒ 1 to 2 nanowatts static power

Dynamic Power is governed by

$$P_d = f_p C_L V_{DD}^2$$

This is the amount of power dissipated by charging/discharging internal capacitance and load capacitance.

Note the relations:

Higher the switching speed ⇒ $P_d$ ↑
Lower the voltage ⇒ $P_d$ ↓↓ !
the Bigger the gates ⇒ $P_d$ ↑
To estimate $P_d$, need to know the switching frequencies of the internal signals

Typically break this into two parts:

$$P_d = (P_d)_{\text{clock network}} + (P_d)_{\text{all the rest}}$$

The power dissipation in the clock network tends to dominate in most designs. Usually assume the switching frequency of logic signals as some fraction of the clock frequency, can estimate by running some sample simulations and keeping switching statistics on internal nodes to build a probabilistic model of switching activity.

Logic synthesis techniques can be used to do the following:

a. minimize # of gates

or

b. maximize speed

and/or

c. minimize switching activity

Also, have "short-circuit" power dissipation – proportional to the amount of time when both $p$- and $n$-trees are conducting.

Slow rise/fall times on nodes can make this significant. Usually ignored in most calculations.
Sizing Routing Calculation

The sizing of signal lines to achieve a particular RC delay was previously discussed.

For power conductors, need to worry about

1. **Metal migration** - too much current in too small a conductor will "blow" the conductor
2. **Ground Bounce** - large current spikes in V\textsubscript{DD}/GND leads can occur when simultaneous outputs switch

Two components to ground bounce.

a. \textit{IR} \quad \leftarrow \text{for on-chip conductors, } R \text{ is resistance of on-chip conductor}

b. \( L \left( \frac{di}{dt} \right) \quad \leftarrow \text{L is the on-chip inductance and package inductance in V\textsubscript{DD}/GND pins. Package inductance dominates. Note that } \frac{di}{dt} \text{ is affected by slew rates on input/output pins.} \)
Example

What would be the conductor width of power and ground wires to a 50MHz clock buffer that drives 100pF of on-chip load to satisfy the metal-migration consideration \( J_{AL} = 0.5\text{mA/μm} \)? What is the ground bounce with chosen conductor size? The module is 500μm from both the power and ground pads and the supply voltage is 5 volts.

1. \( P = fCV_{DD}^2 \)
   \[ = 100 \times 10^{-12} \times 25 \times 50 \times 10^6 \]
   \[ = 125\text{mW} \]
   \( I = P/V = 25\text{mA} \)
   Thus the width of the clock wires should be at least 50μm. A good choice would be 100μm.

2. \( R = 500/100 \times 0.05 \)
   \[ = 5 \text{ squares} \times 0.05 \text{ Ω/sq.} \]
   \[ = 0.25\text{Ω} \]
   \( IR = 0.25 \times 25 \times 10^{-3} = 6.25\text{mV} \)

Typically, \( IR \) term of ground bounce very small compared to \( L \left( \frac{di}{dt} \right) \) term.