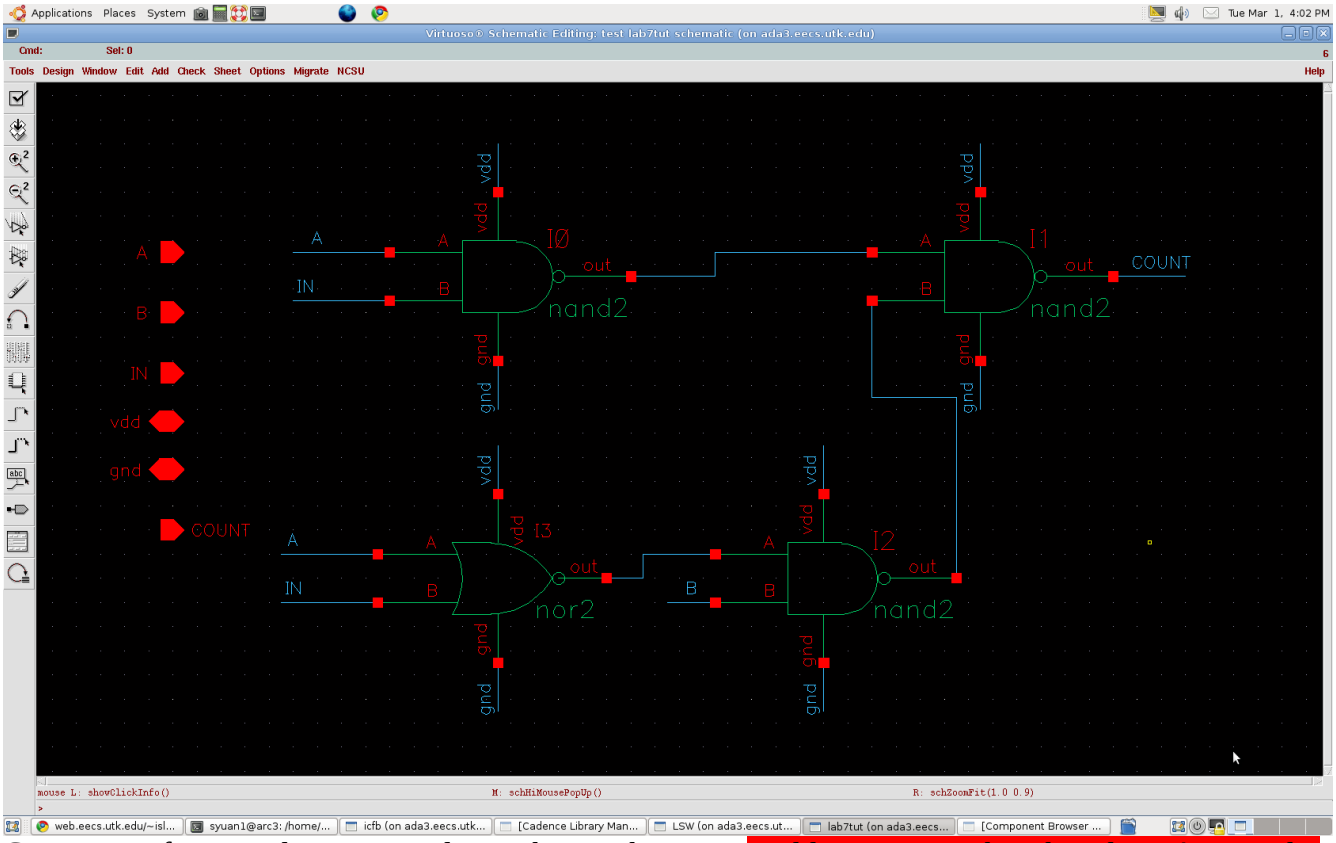
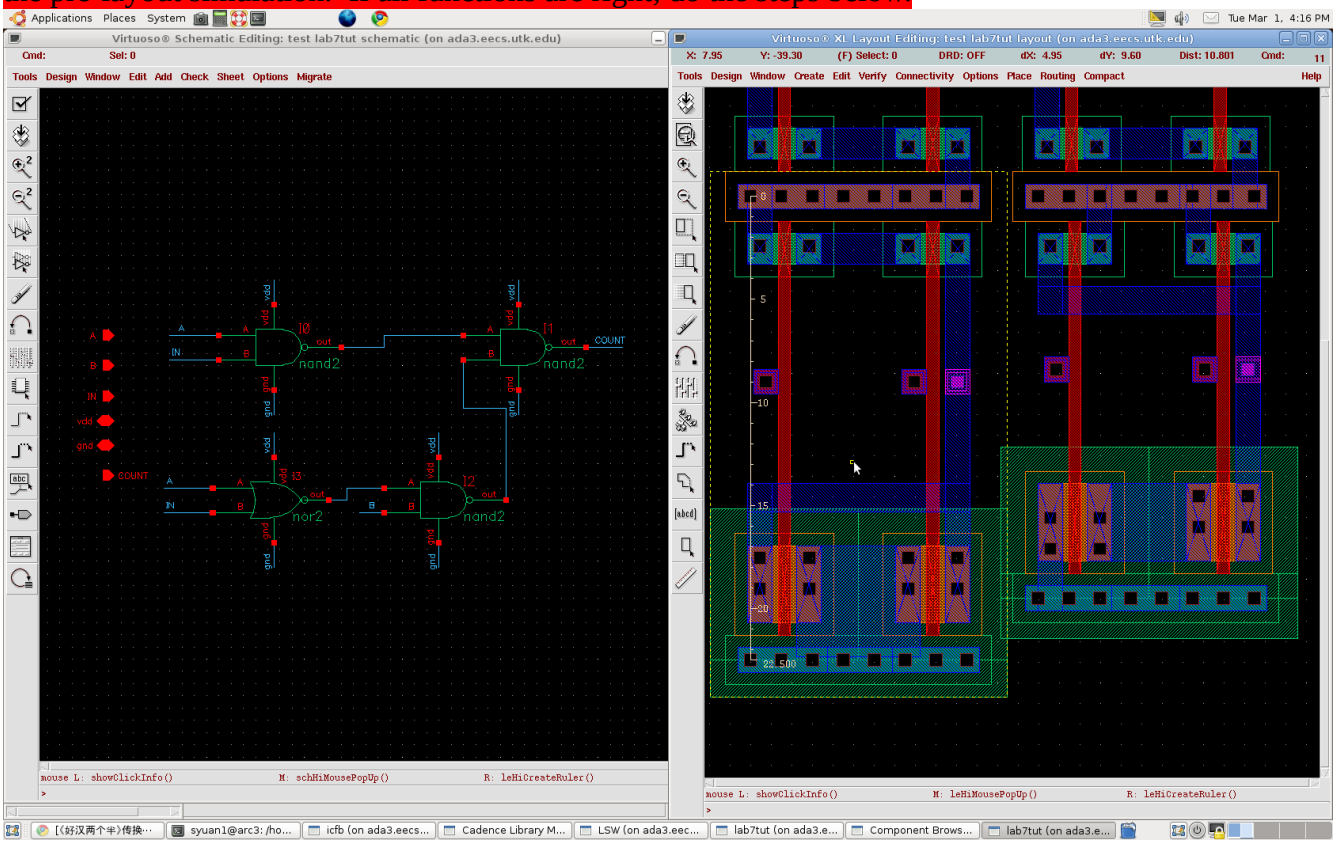
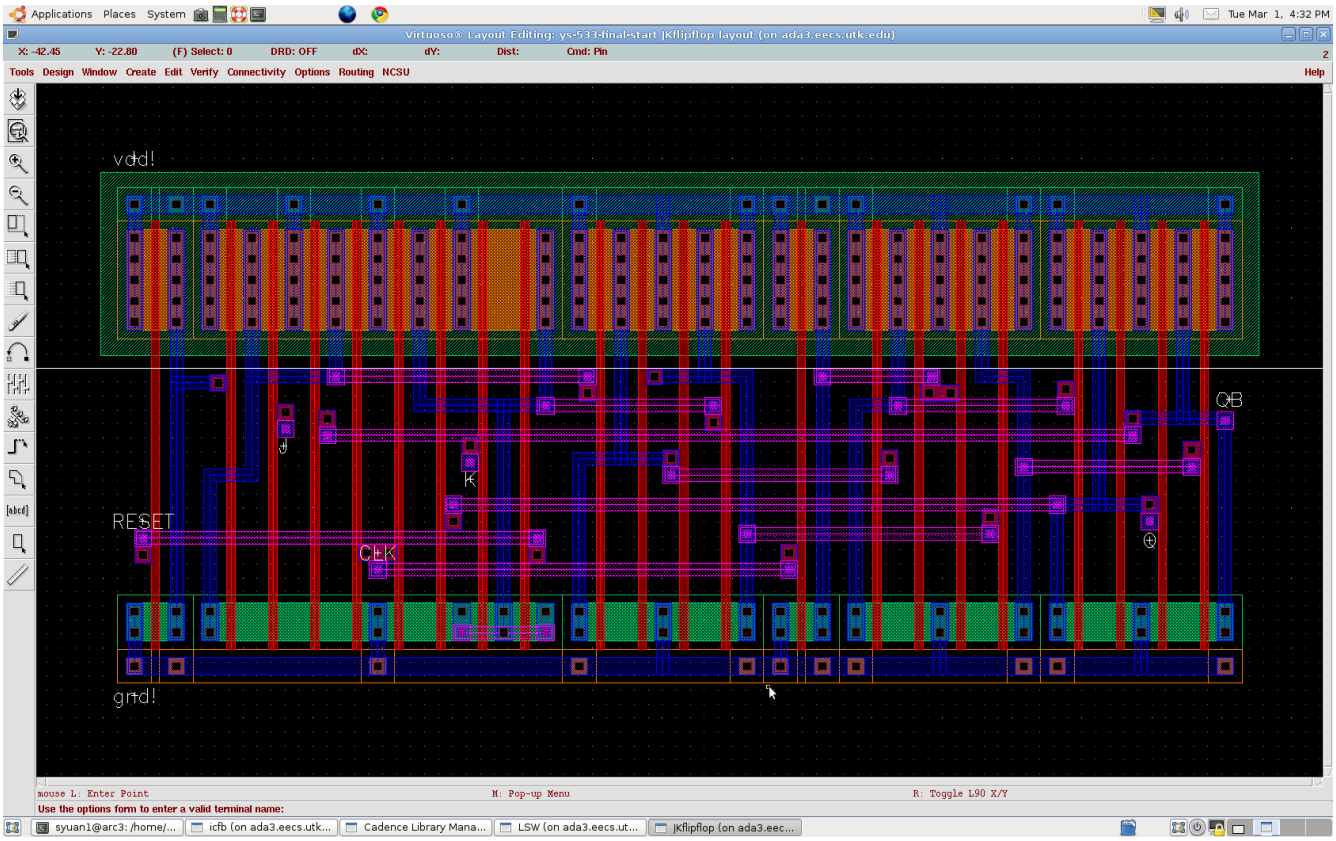


Create your functional circuit similar to above schematic. Build up your test bench and use ADE to do the pre-layout simulation. If all functions are right, do the steps below.

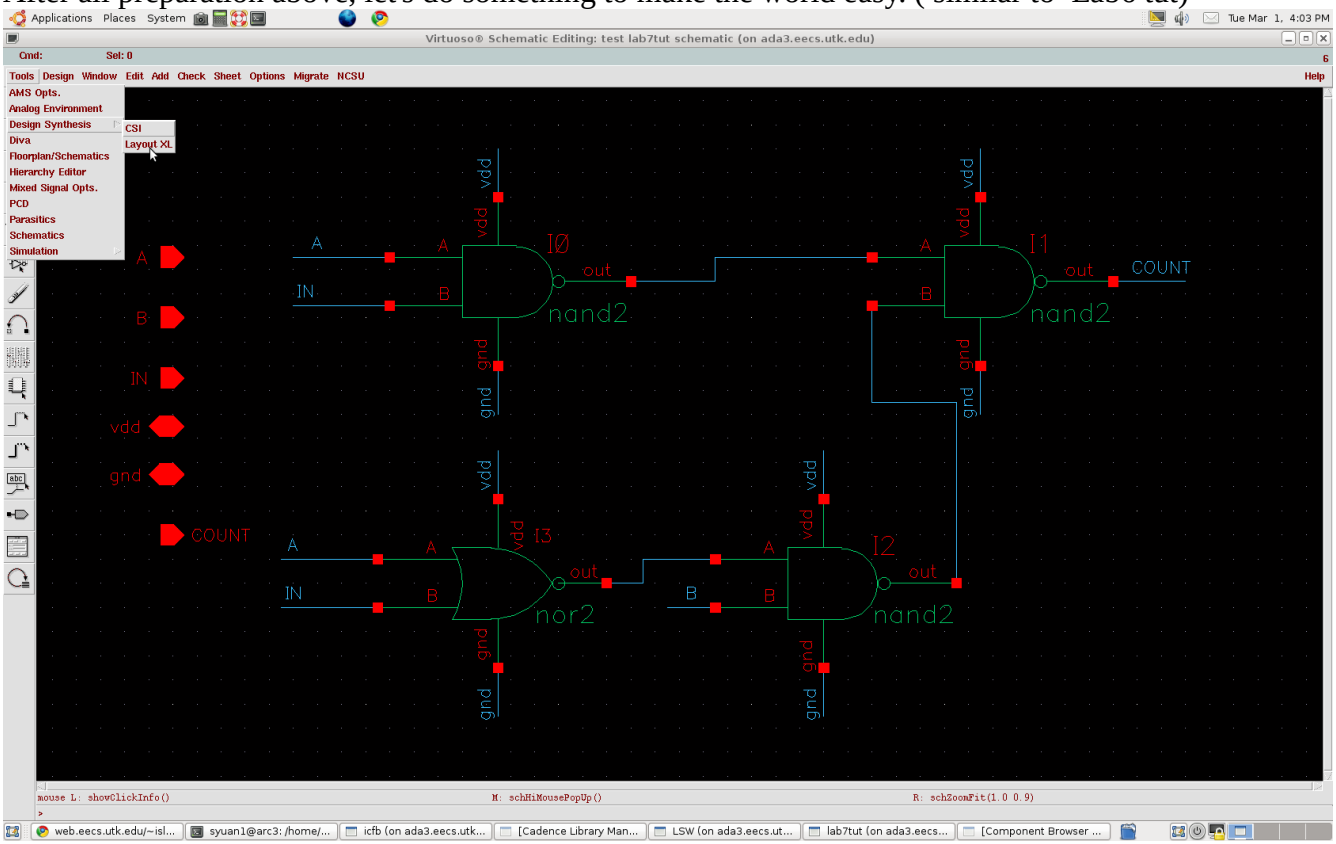


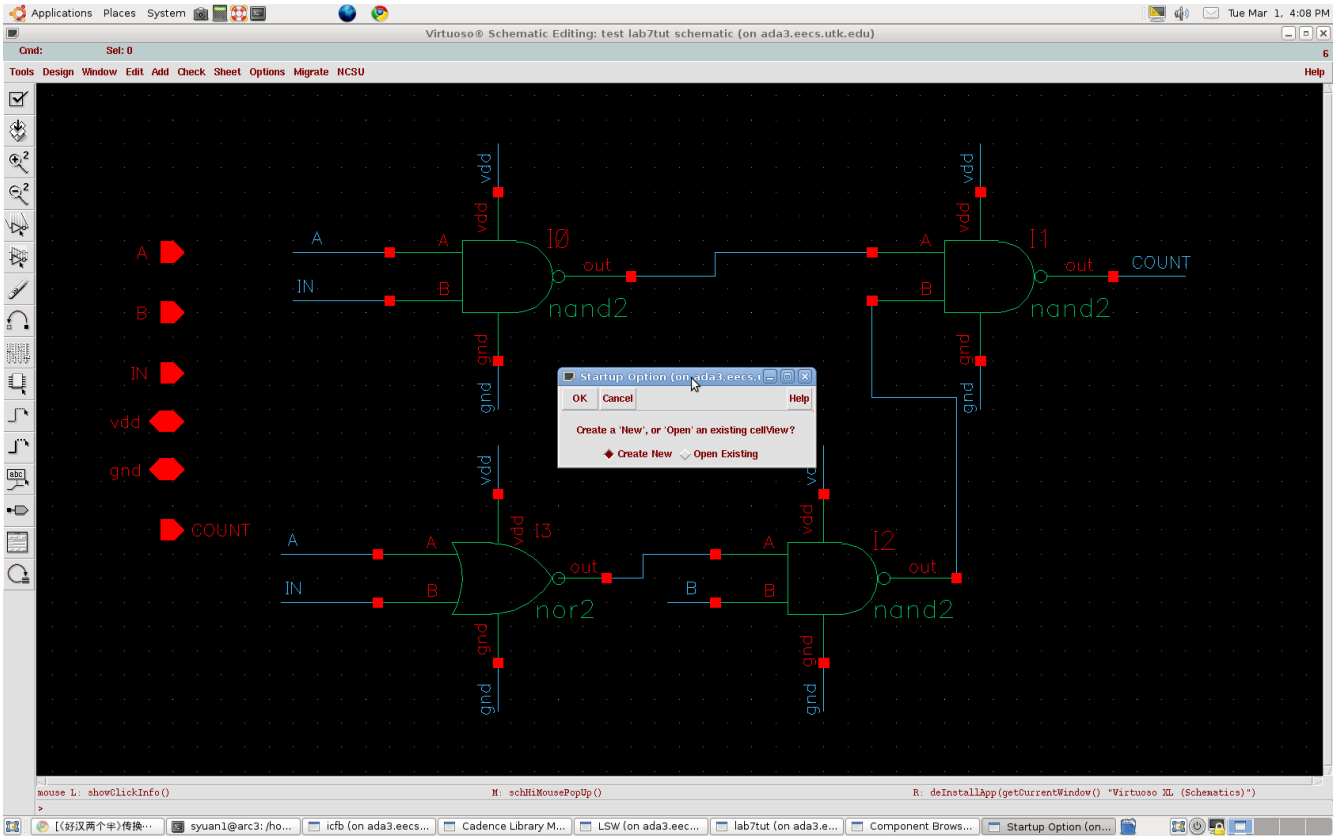
Before we do the layout, please make sure all your standard cell(INV, NAND, NOR, XOR, etc.) layouts have the same height (the height is indicate by the ruler on above picture). As you see, the NAND and NOR gate have different height, and it will cause a lot of troubles for our further layout steps. You can choose different height value. The main principle for that is leaving enough space for the

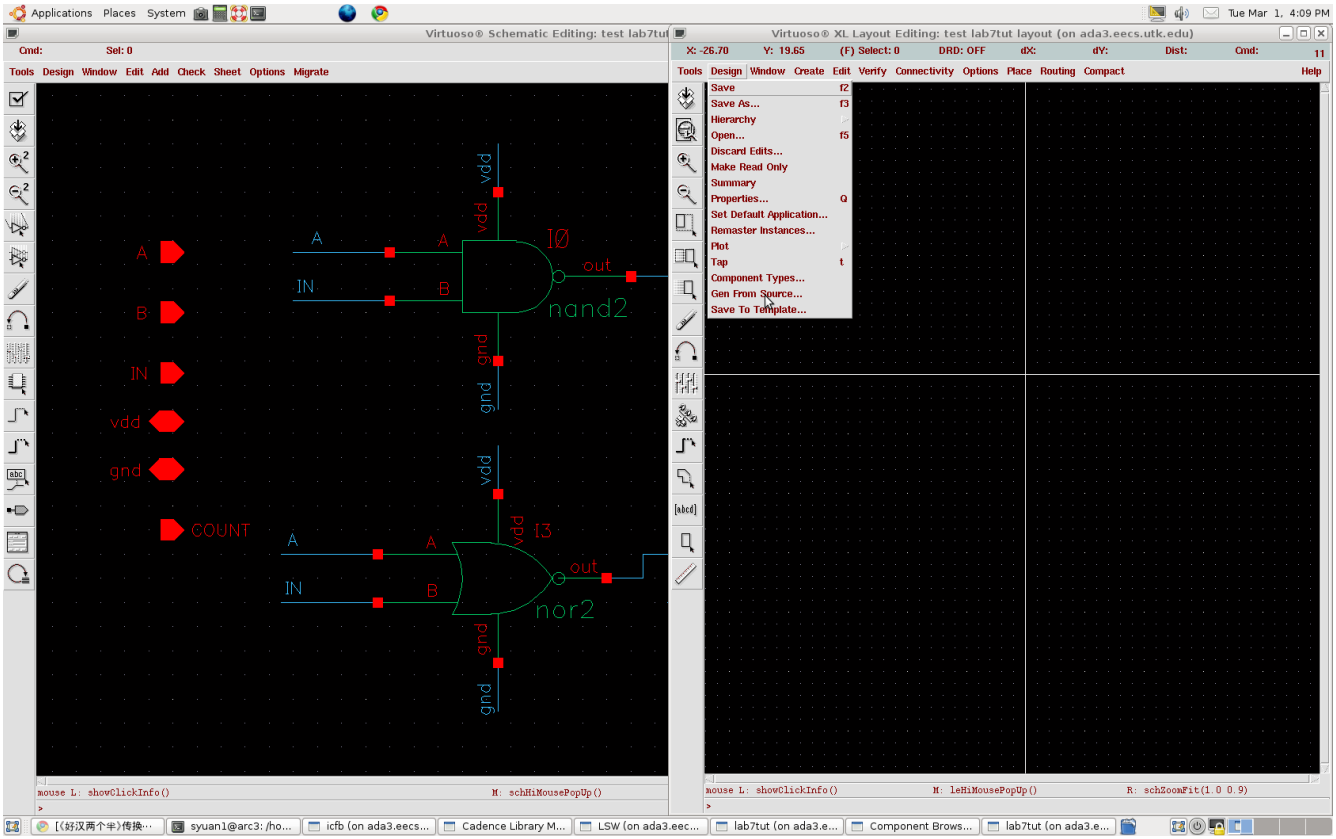
interconnection paths between the standard cells. To make you understand well about what I say, I put a JK FF below.

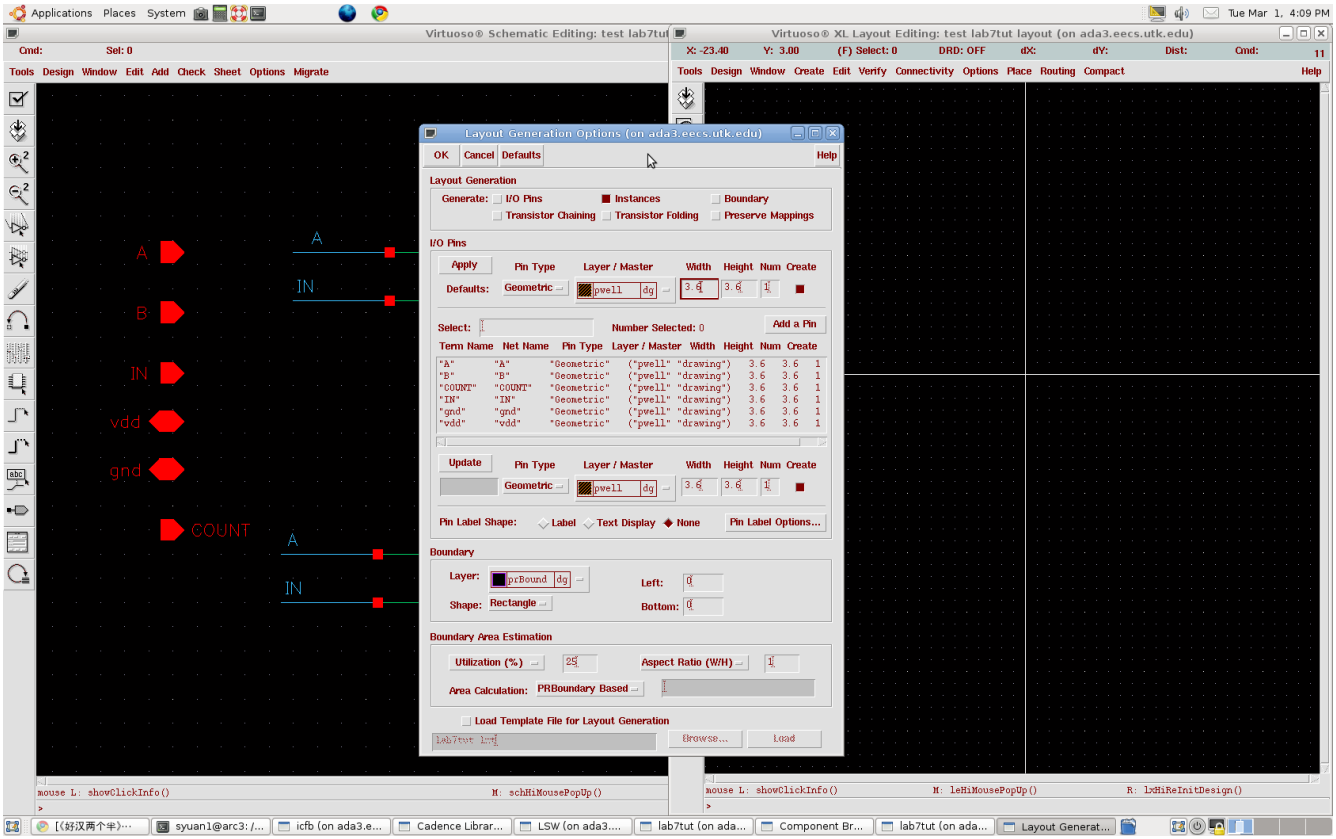


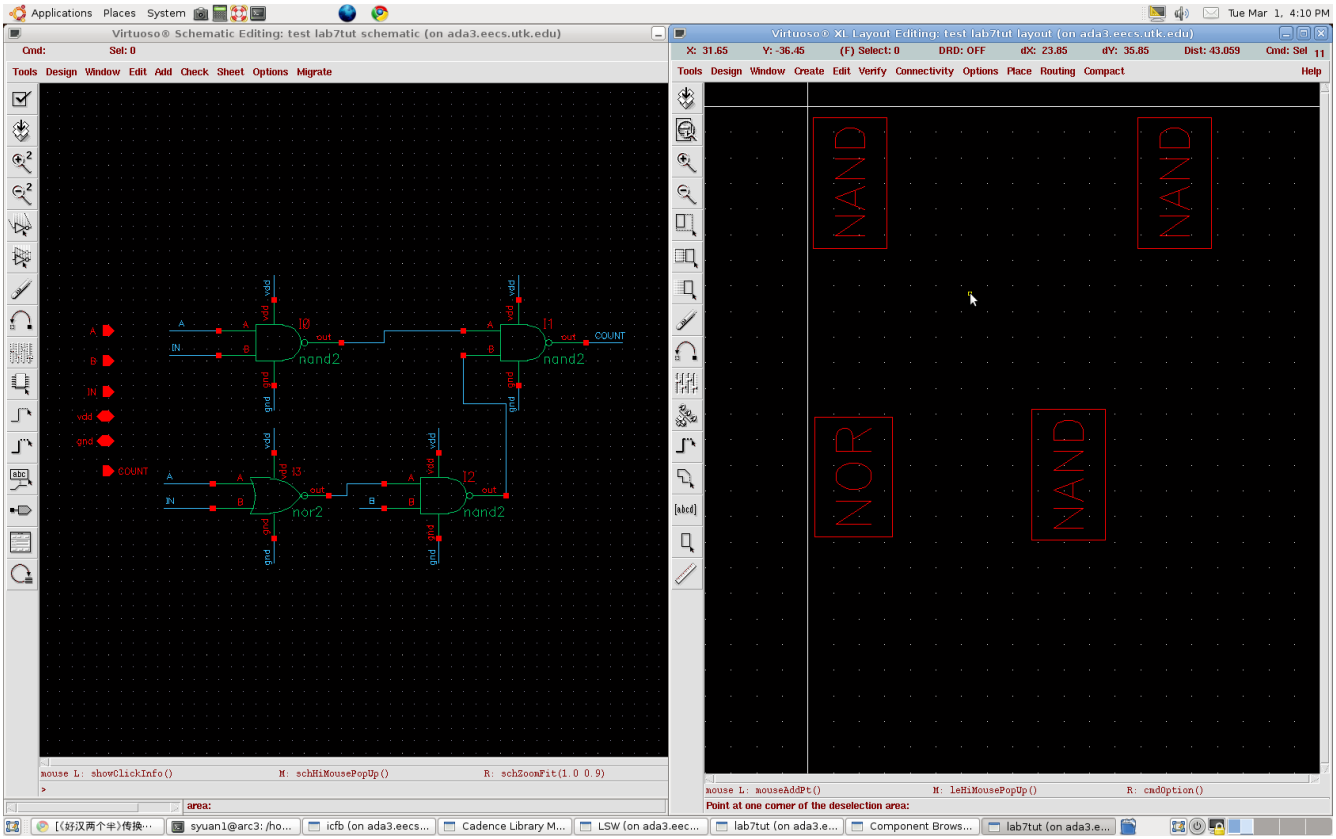
After all preparation above, let's do something to make the world easy. (similar to Lab6 tut)



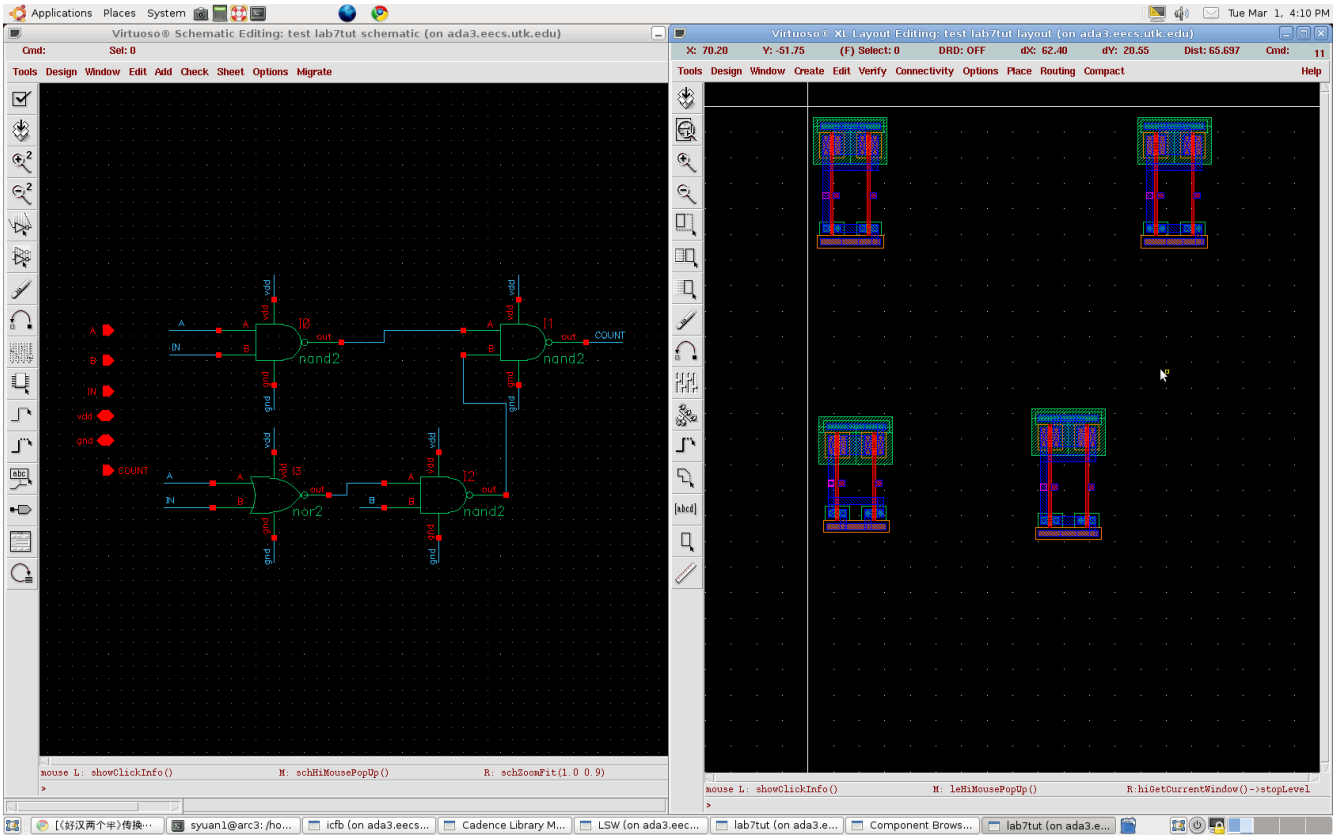

Applications Places System
Tue Mar 1, 4:08 PM
Virtuoso® Schematic Editing: test lab7tut schematic (on ada3.eecs.utk.edu)
Cmd: Sel: 0
Tools Design Window Edit Add Check Sheet Options Migrate NCSU
Help
A
B
IN
vdd
gnd
COUNT
I0
nand2
I1
nand2
I3
nor2
I2
nand2
out
Startup Option (on ada3.eecs.u
OK Cancel Help
Create a 'New', or 'Open' an existing cellView?
Create New Open Existing
mouse L: showClickInfo()
M: schHiMousePopUp()
R: deInstallApp(getCurrentWindow() "Virtuoso XL (Schematics)")

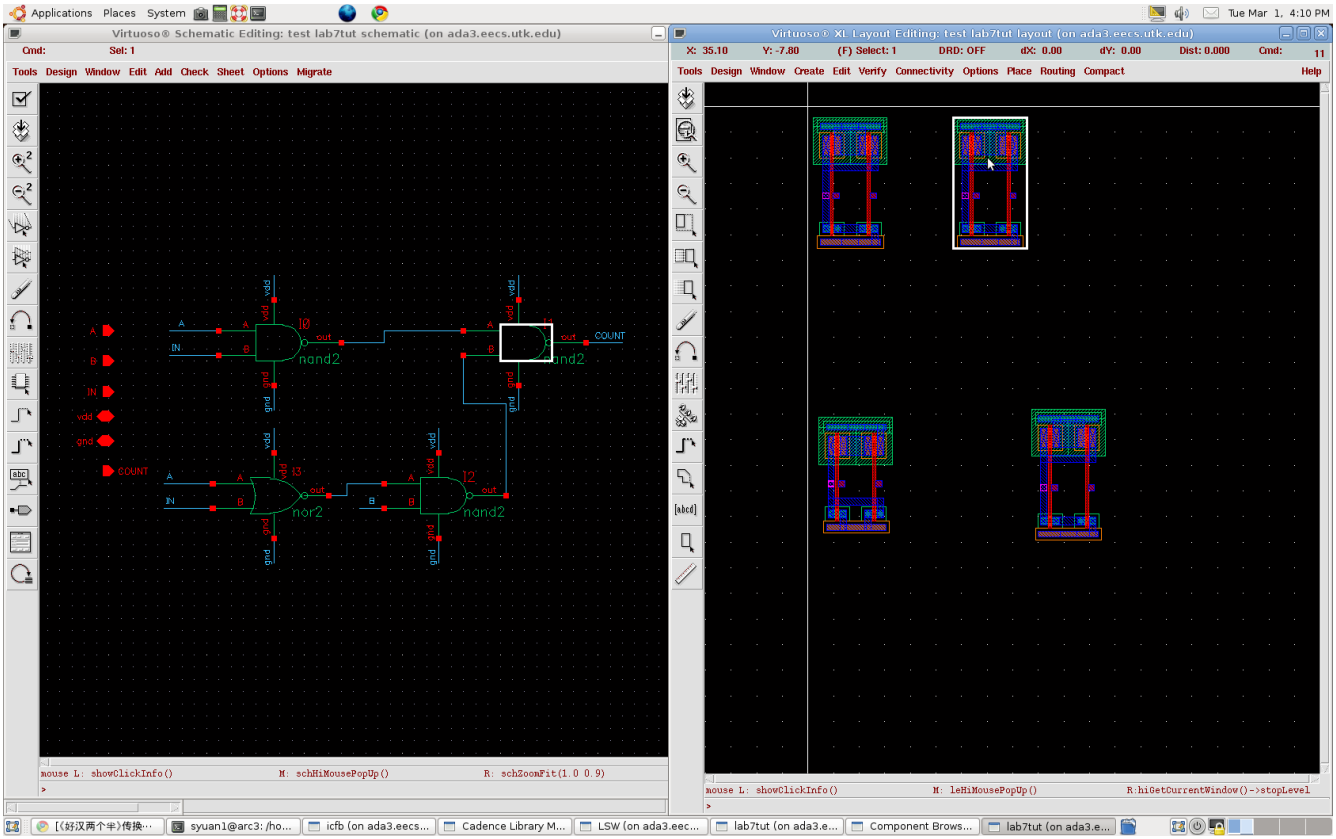

Applications Places System
Tue Mar 1, 4:09 PM
Virtuoso® Schematic Editing: test lab7tut
Virtuoso® XL Layout Editing: test lab7tut layout (on ada3.eecs.utk.edu)
X: -26.70 Y: 19.65 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd:
Tools Design Window Edit Add Check Sheet Options Migrate
Tools Design Window Create Edit Verify Connectivity Options Place Routing Compact
Help
Save f2
Save As... f3
Hierarchy
Open... f5
Discard Edits...
Make Read Only
Summary
Properties... Q
Set Default Application...
Remaster Instances...
Plot
Tap t
Component Types...
Gen From Source...
Save To Template...
mouse L: showClickInfo()
M: schHiMousePopUp()
M: leHiMousePopUp()
R: schZoomFit(1.0 0.9)



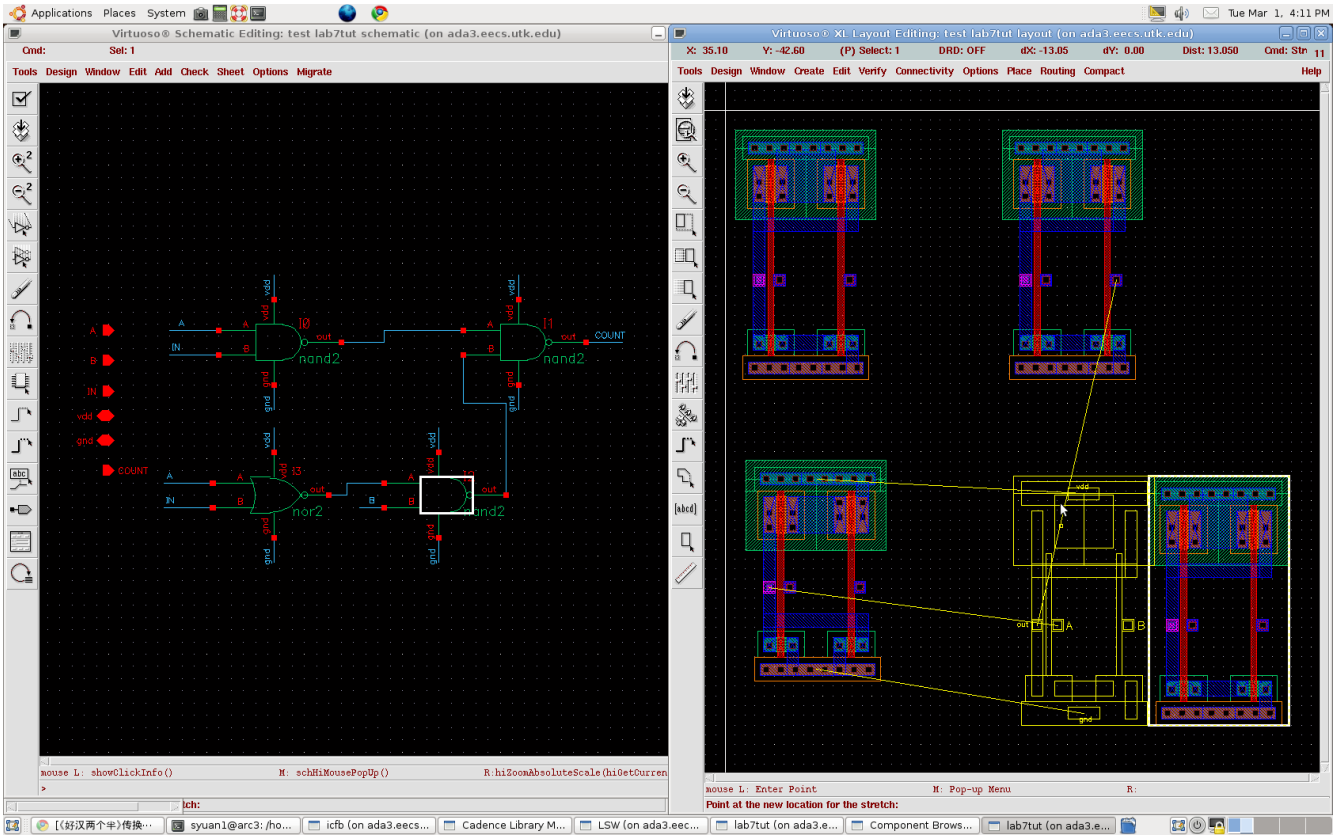


Yes! Life is good! Using Shift+f to see you standard cells and Ctrl+f to change back.

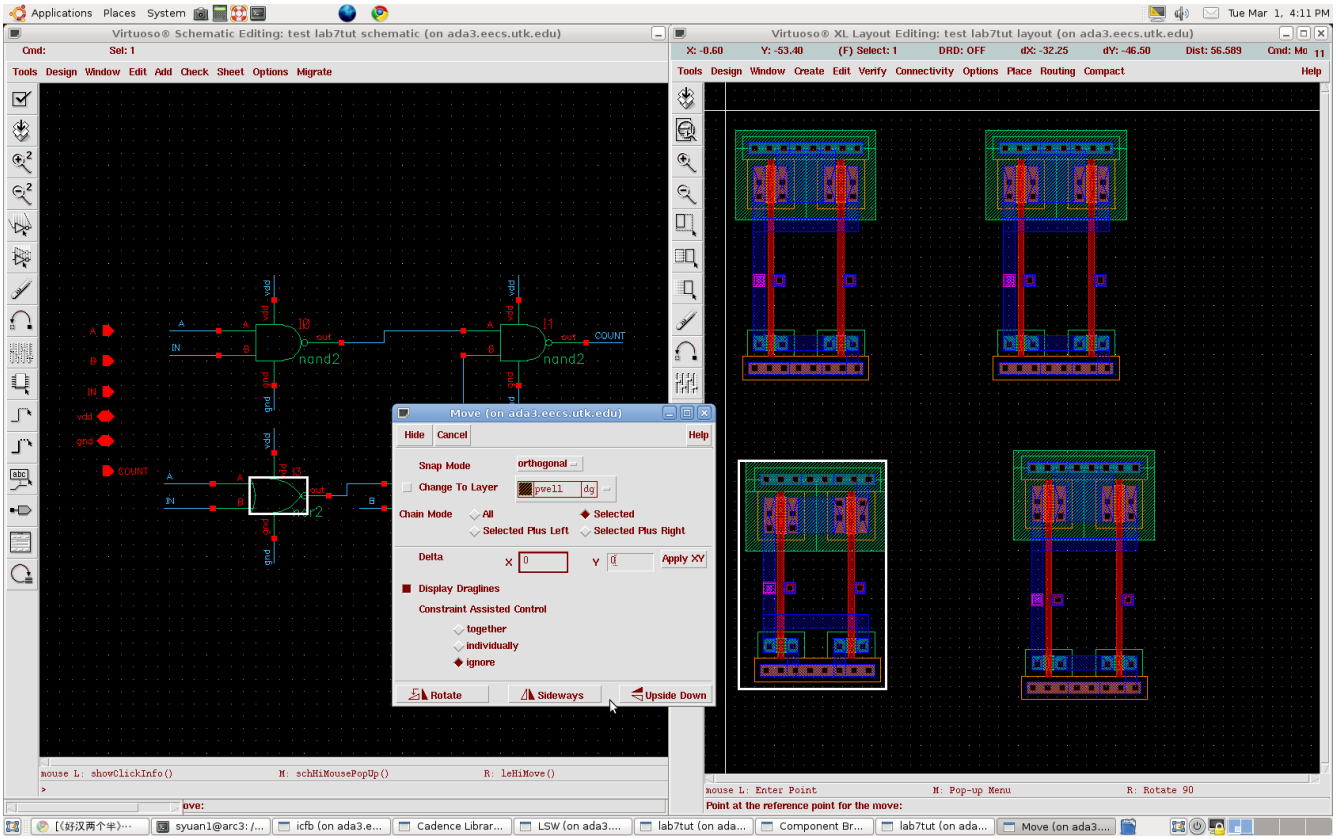




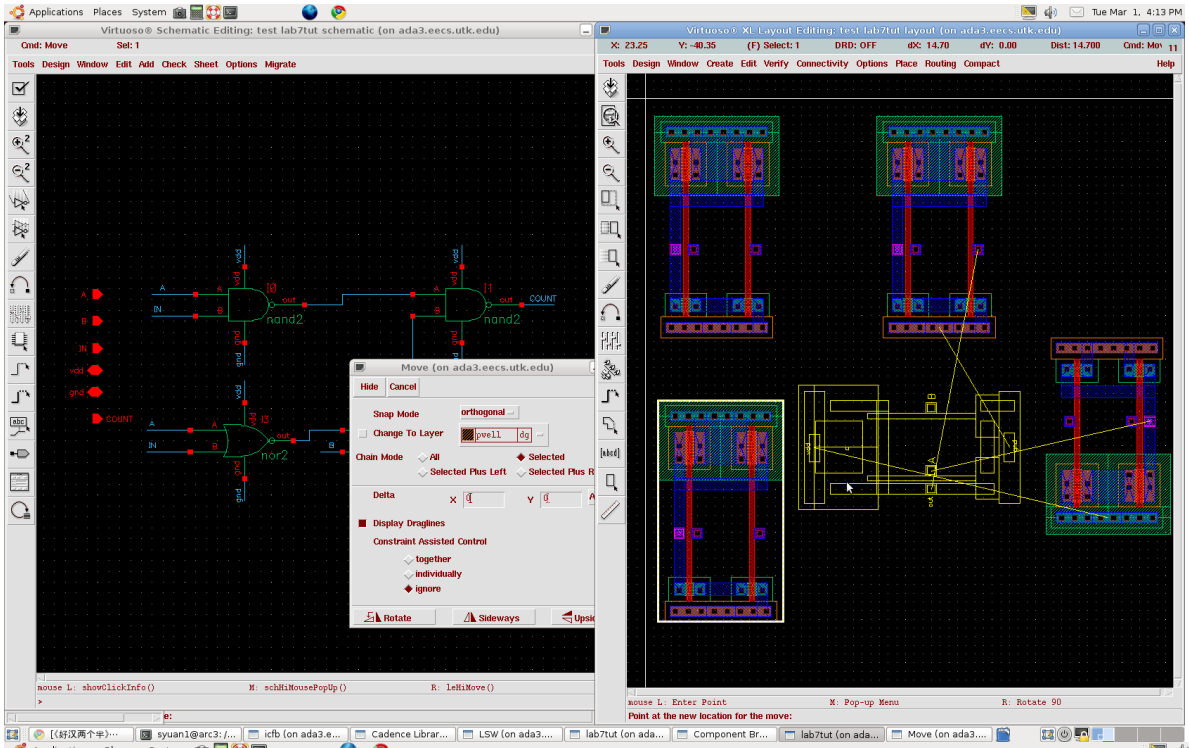
Similar to Lab6 tut, clicking on any cell in Layout XL, it will highlight the respect symbol in your schematic.

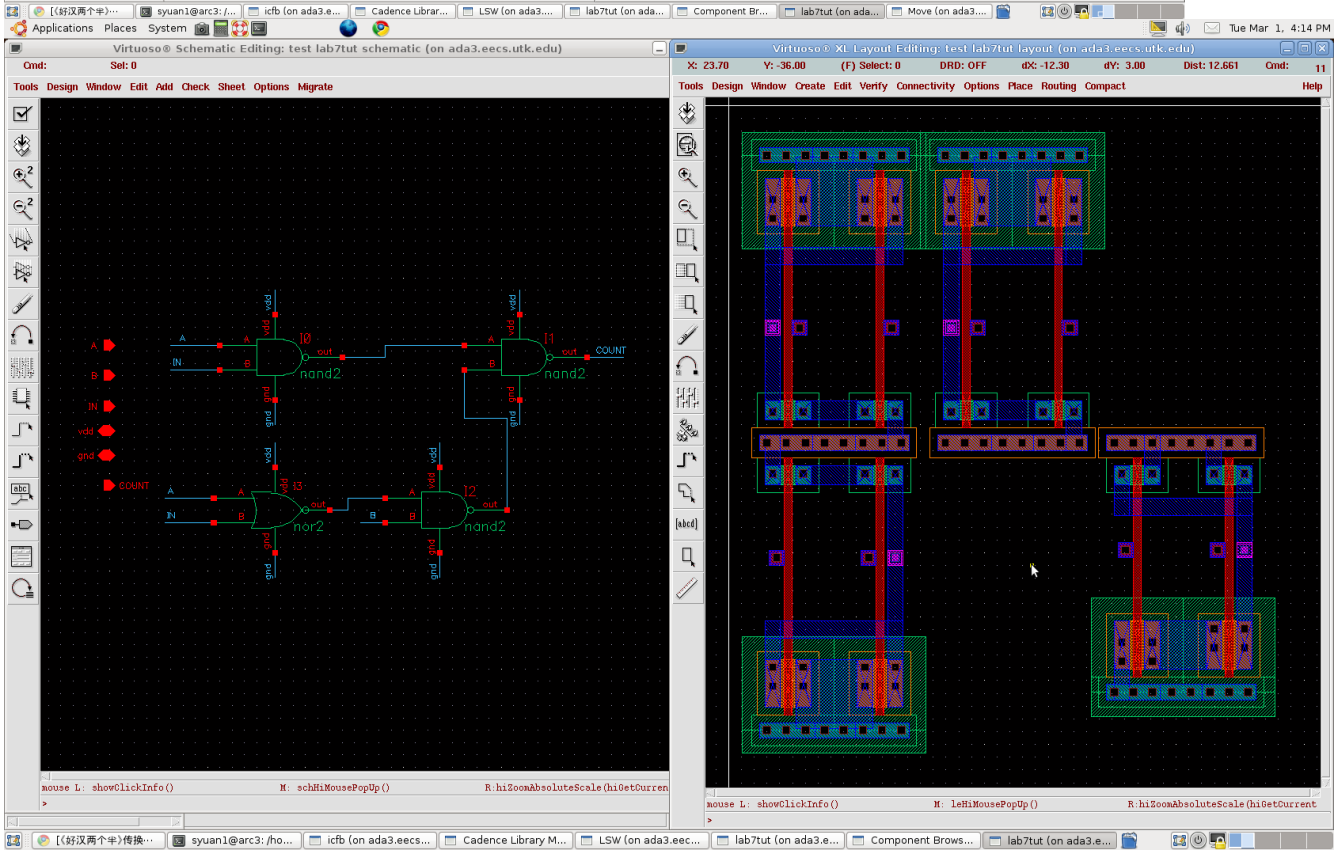


If you move any cell, it will show you the connection to the other cells.



Using shortcut 'm', the dialog block will shows up. Click on the cell you want to operate. You can rotate, sideways and upside down your cell by hit the respect button on the bottom of the dialog block.





In your future work, you may use following two- line place method.

vdd==========

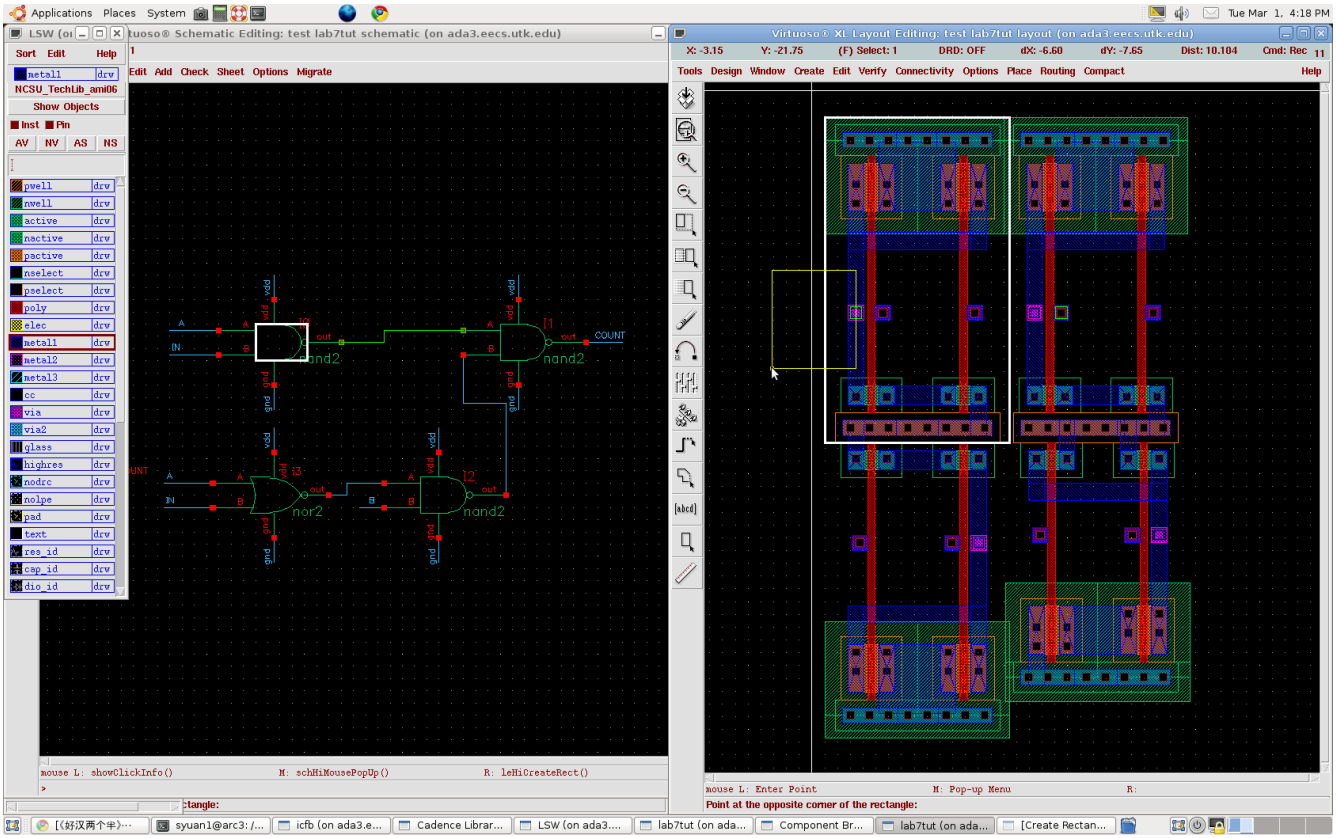
stdcell-1 stdcell-2 stdcell-3

gnd==========

stdcell-4 stdcell-5 stdcell-6

vdd==========

In this picture, using two line place method, I use two exactly same gnd contacts for both NAND gate. So I overlap the gnd contacts to let them share same gnd rail.



If you use shortcut 'r' (create a rectangle) or shortcut 'p' (create a path) to draw the interconnection, it will show you in green highlight for the output and input pin you want to connect in Layout XL and the respect input, output and connect wire in schematic.

Then finish your layout and do the LVS and Extract. Use the ADE to do the post-layout simulation! Enjoy your life :)

Acknowledgement :

Thank Cory Fandrich sharing his stand-cells for the tutorial.