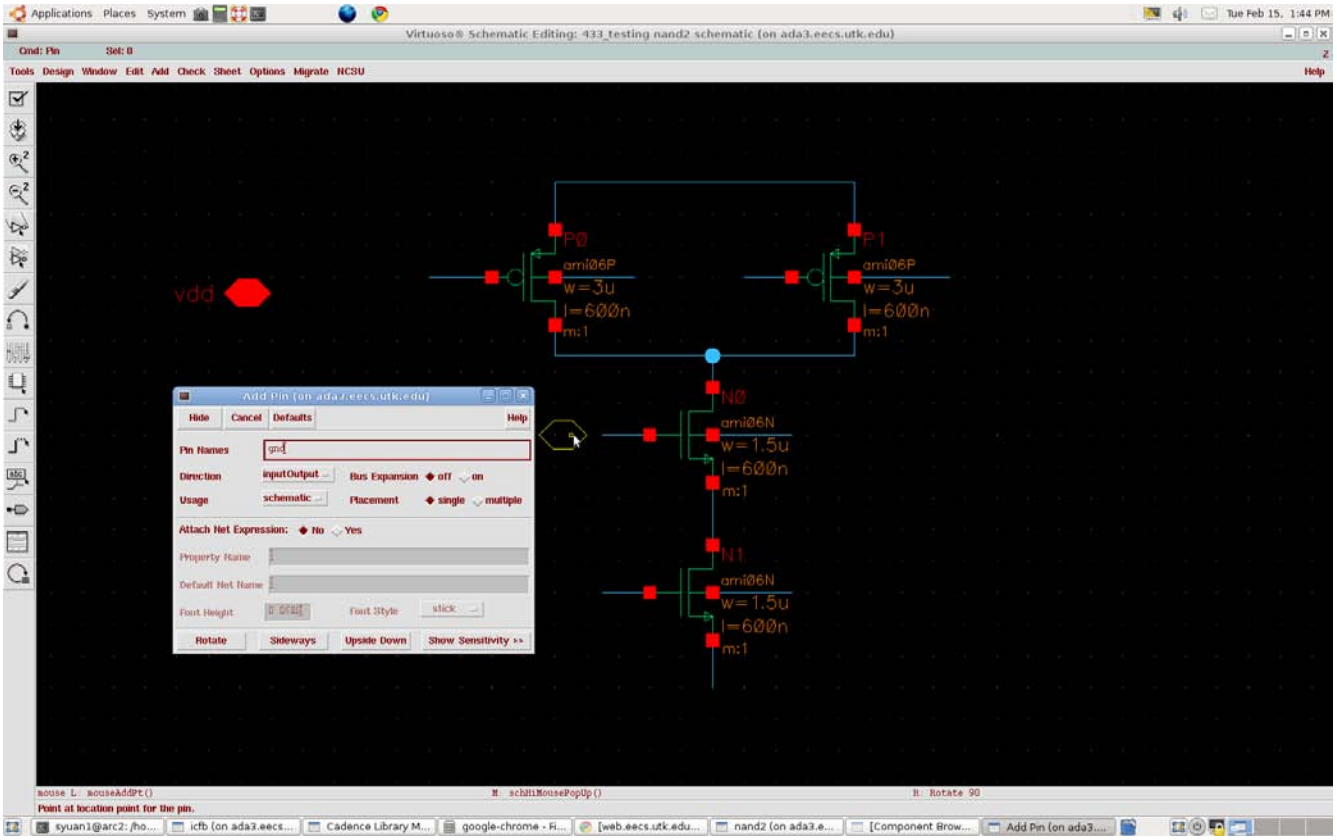
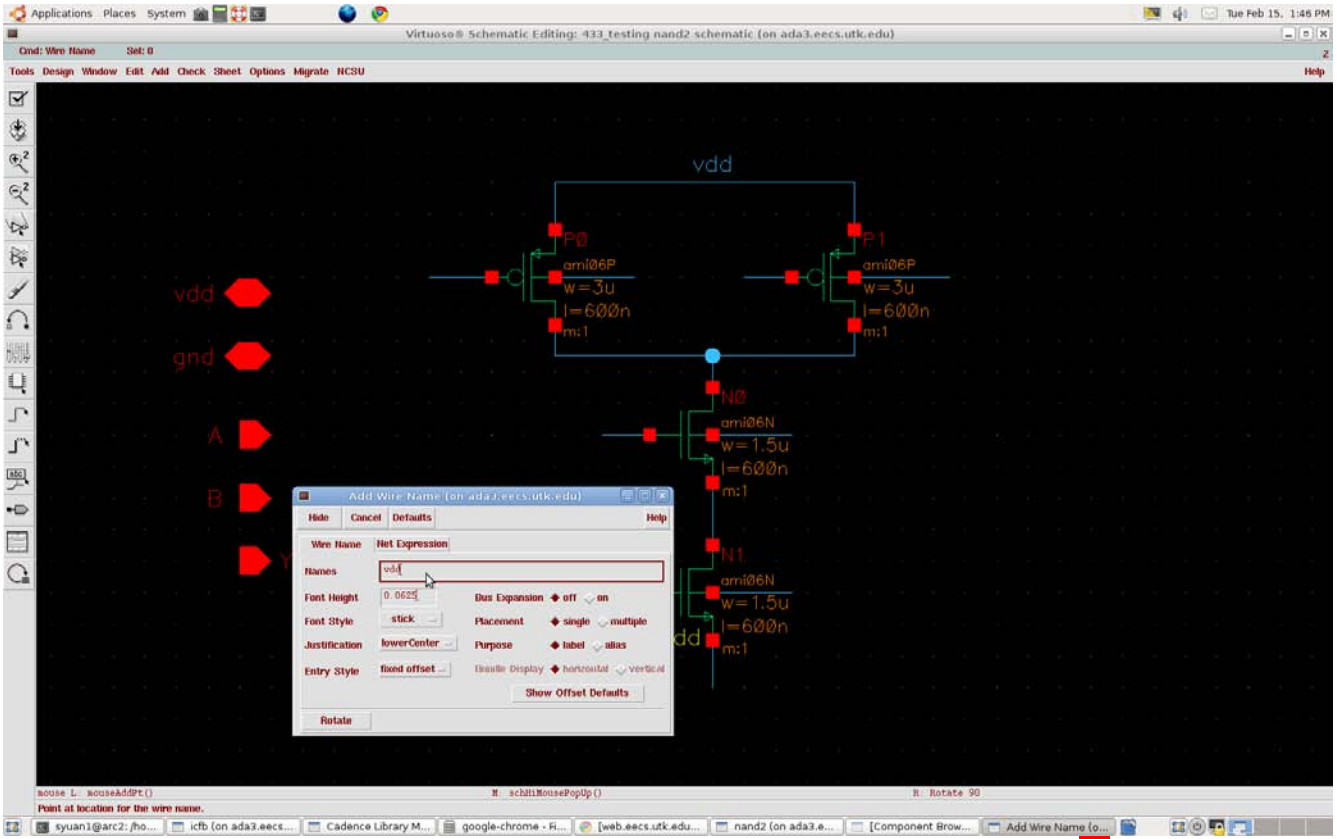
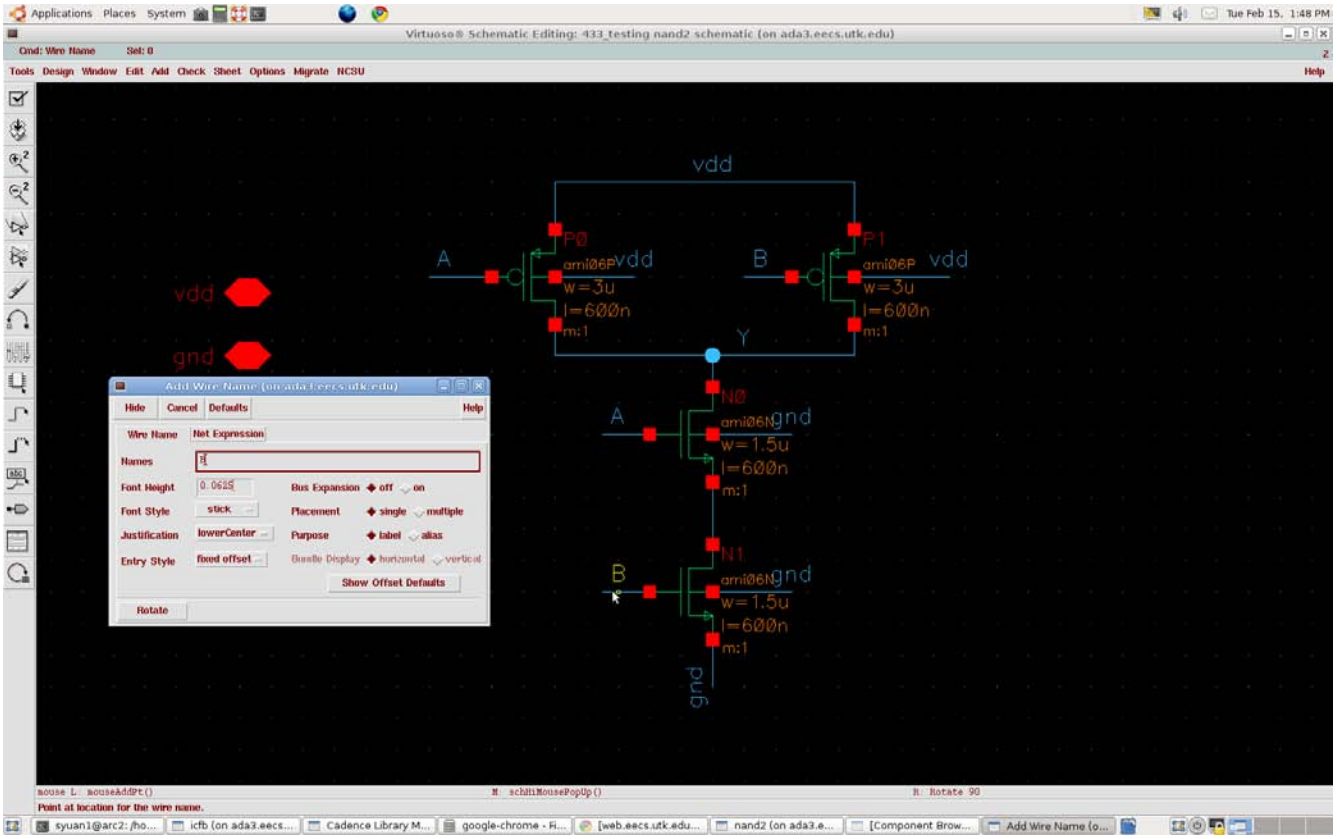
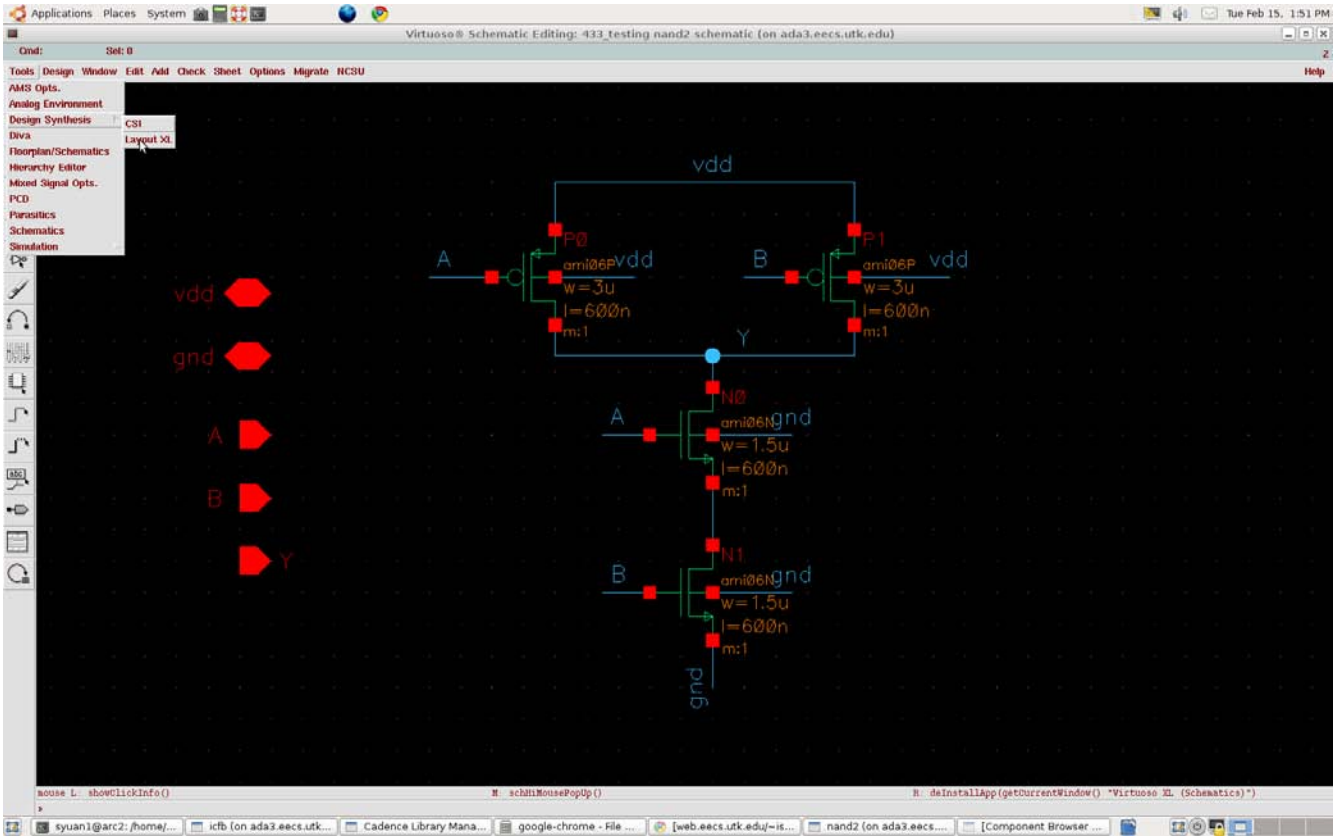


Let us take nand gate as an example. Create nand gate schematic like this. Use shortcut 'Ctrl + p' to add pins. Leave all pins you will use in your nand gate on the left without connecting any wires.

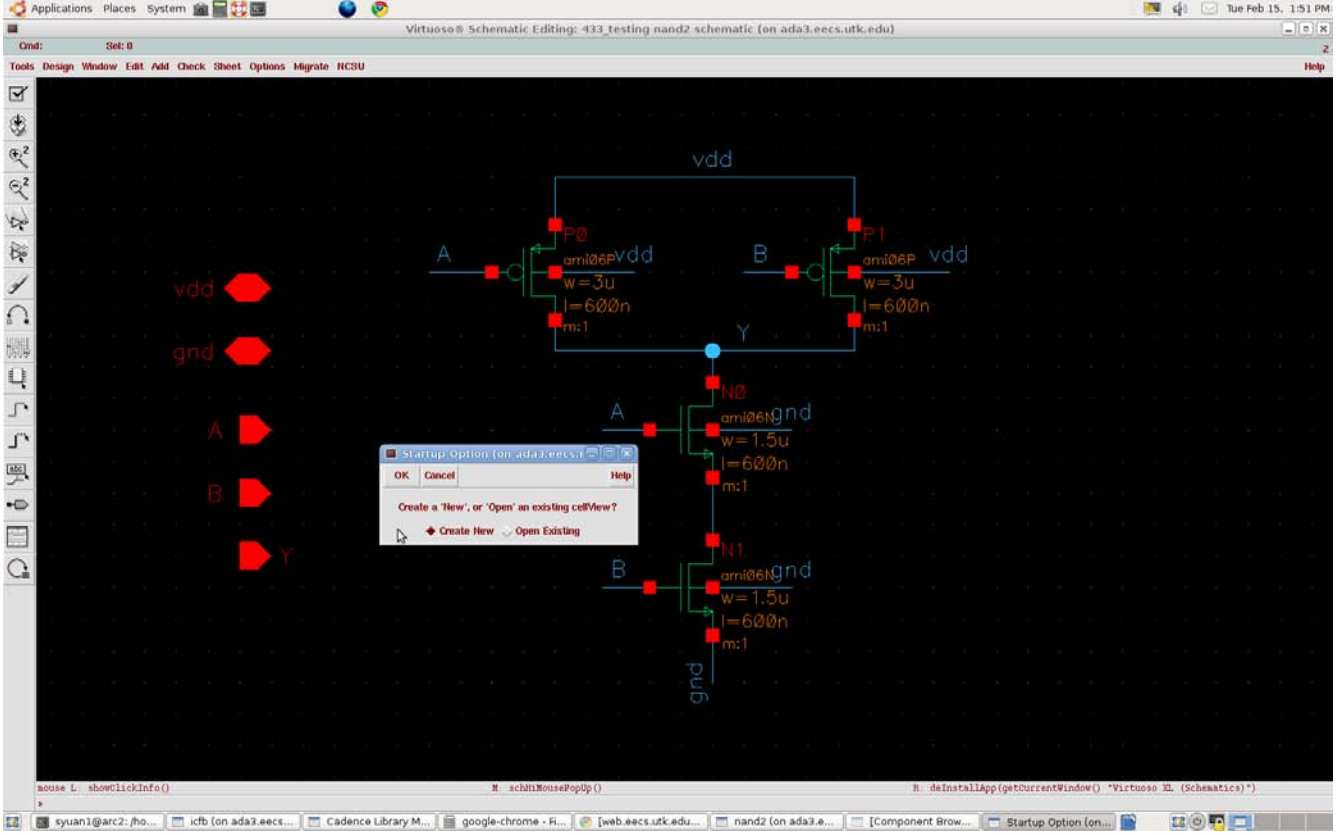


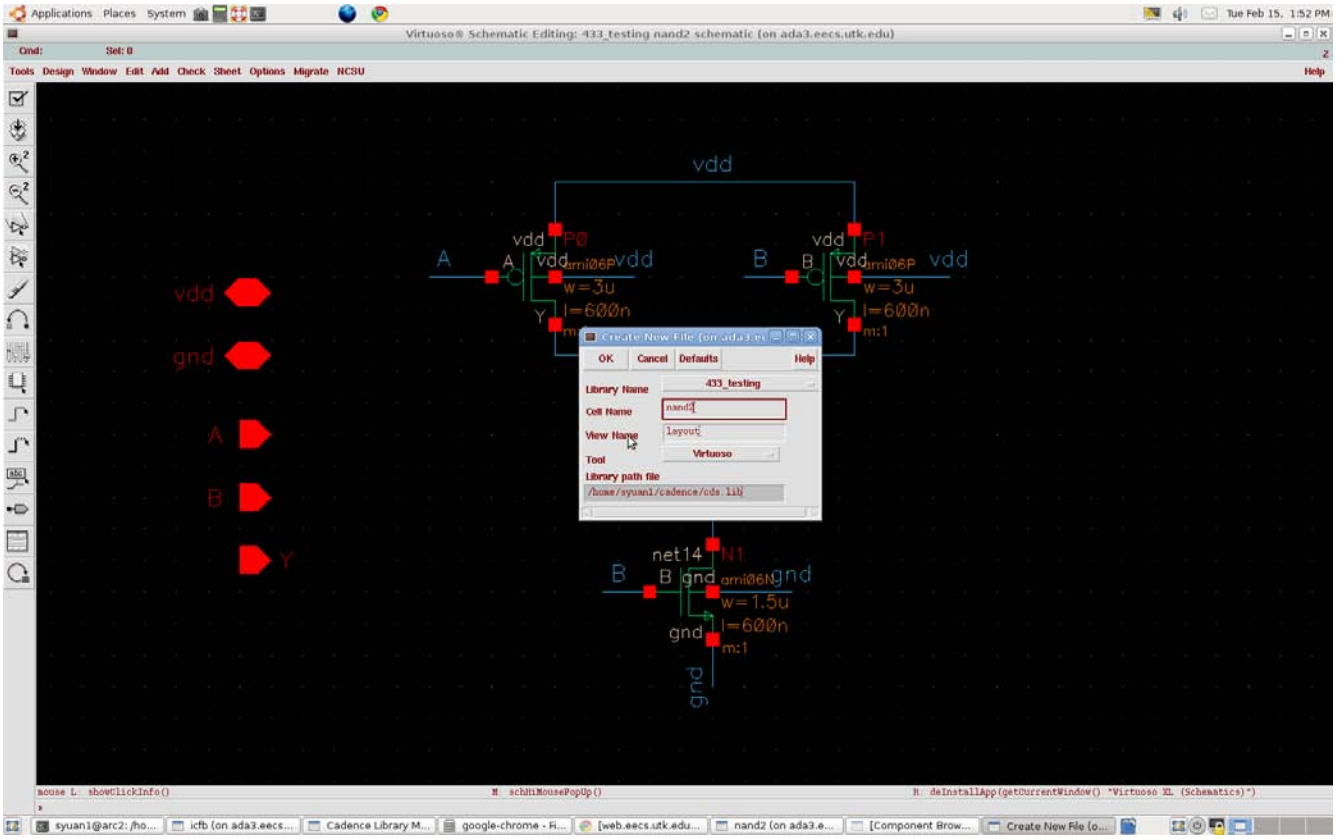
Use shortcut ' l (not one)' to add wire name. Input the wire name, say 'vdd', and then use your mouse to click on all wires you want to name as 'vdd'. Every pin should be matched with a wire name.(Also see the next picture.)



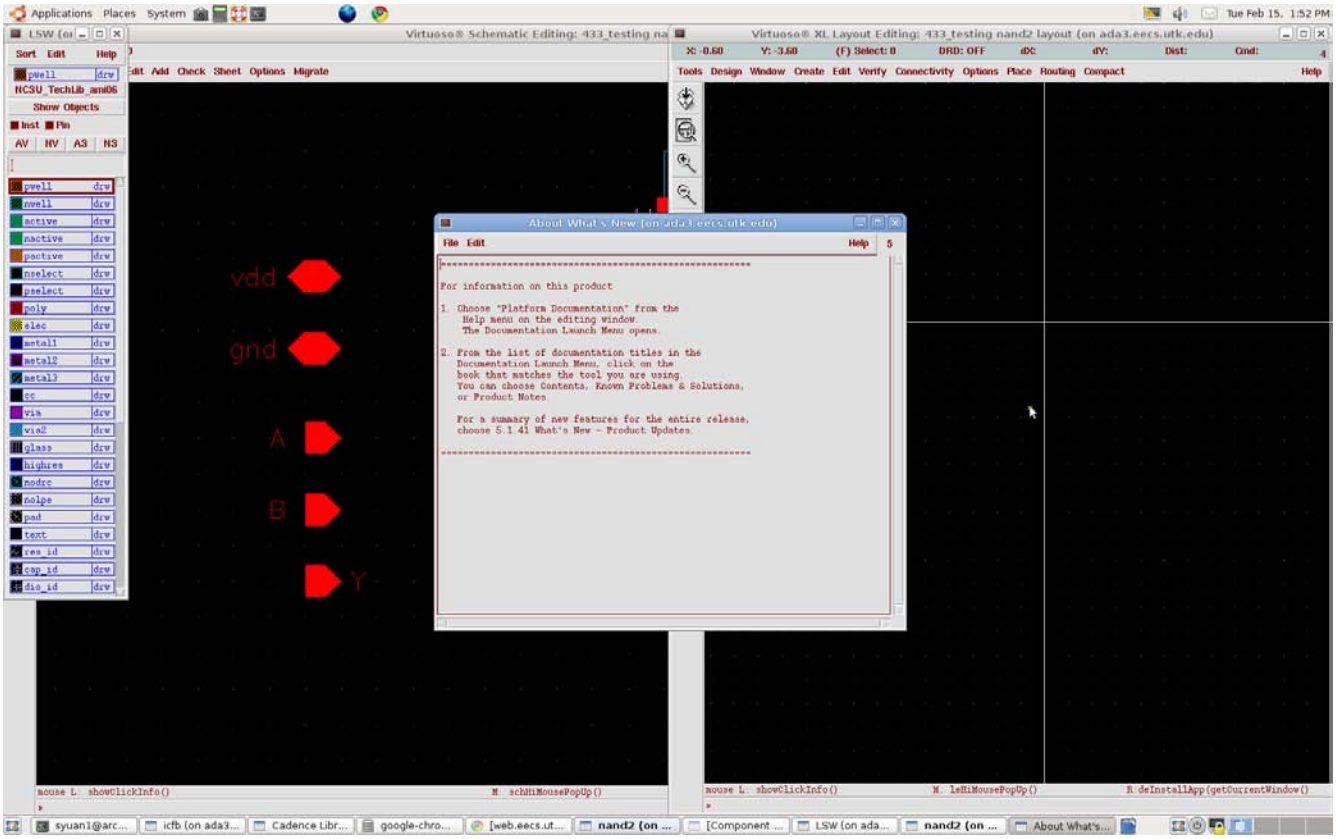


After naming all wires with matched pin names, click 'Tools' ==> 'Design Synthesis' ==>'Layout XL'
The dialog block will come out. Select 'Create New', and then click OK.

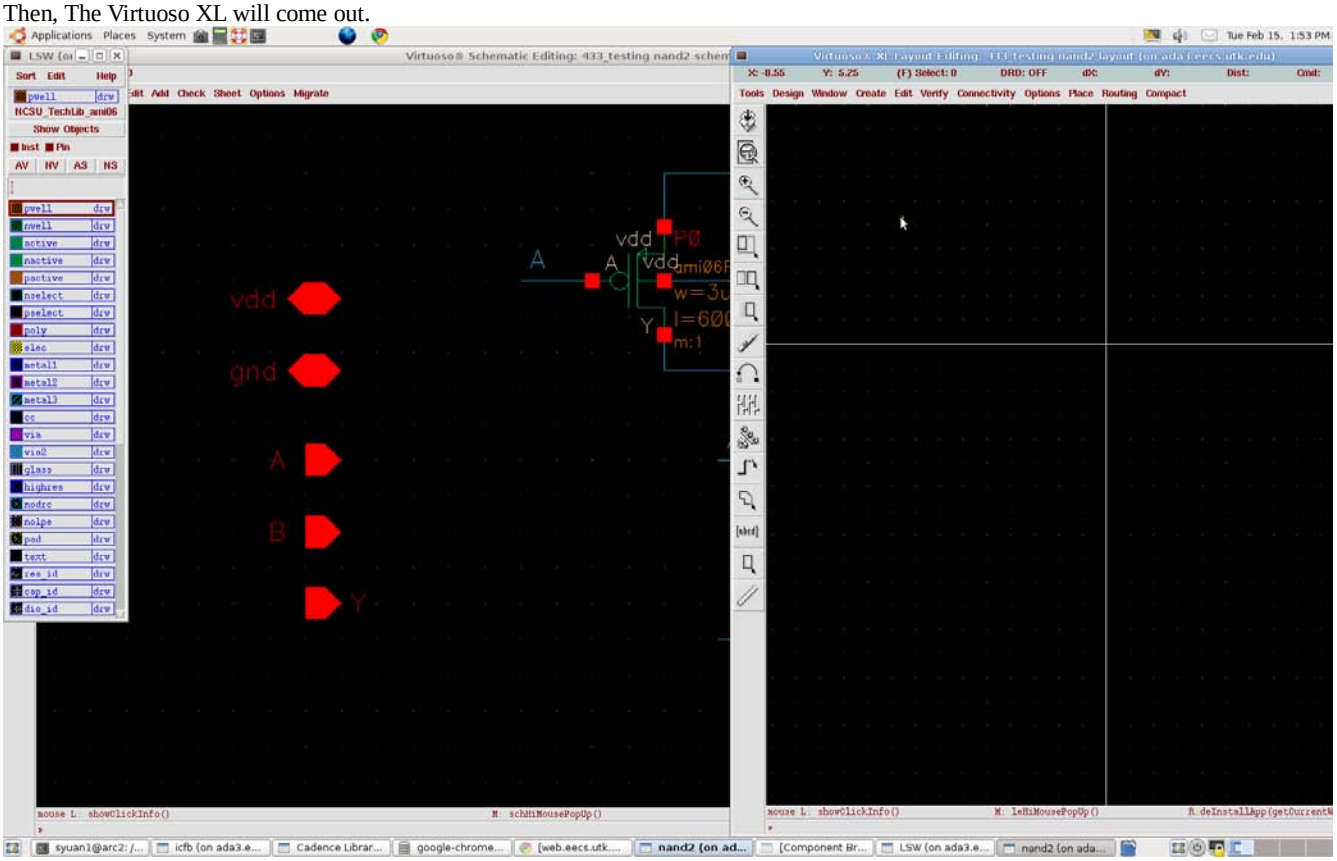


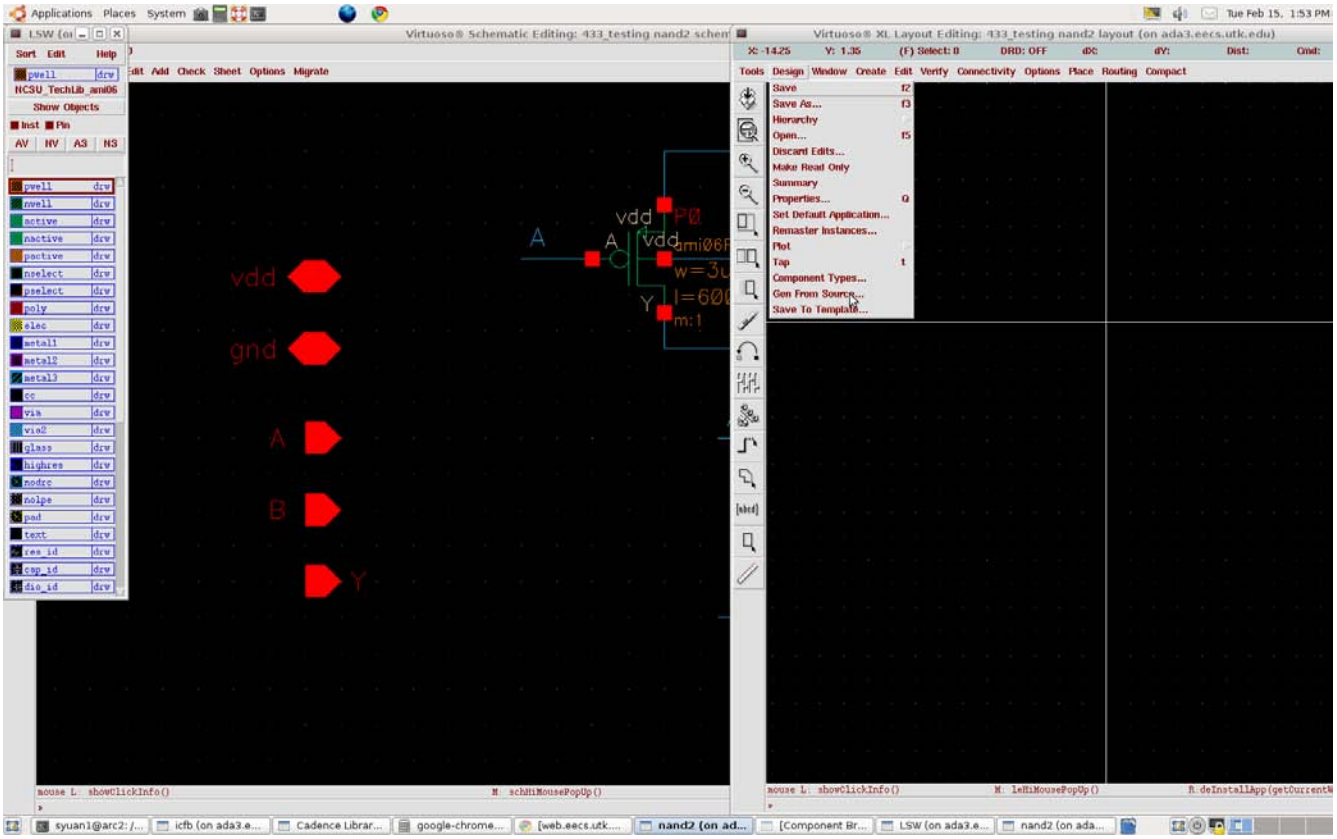


Another block will come out. Input the cell name. Click OK

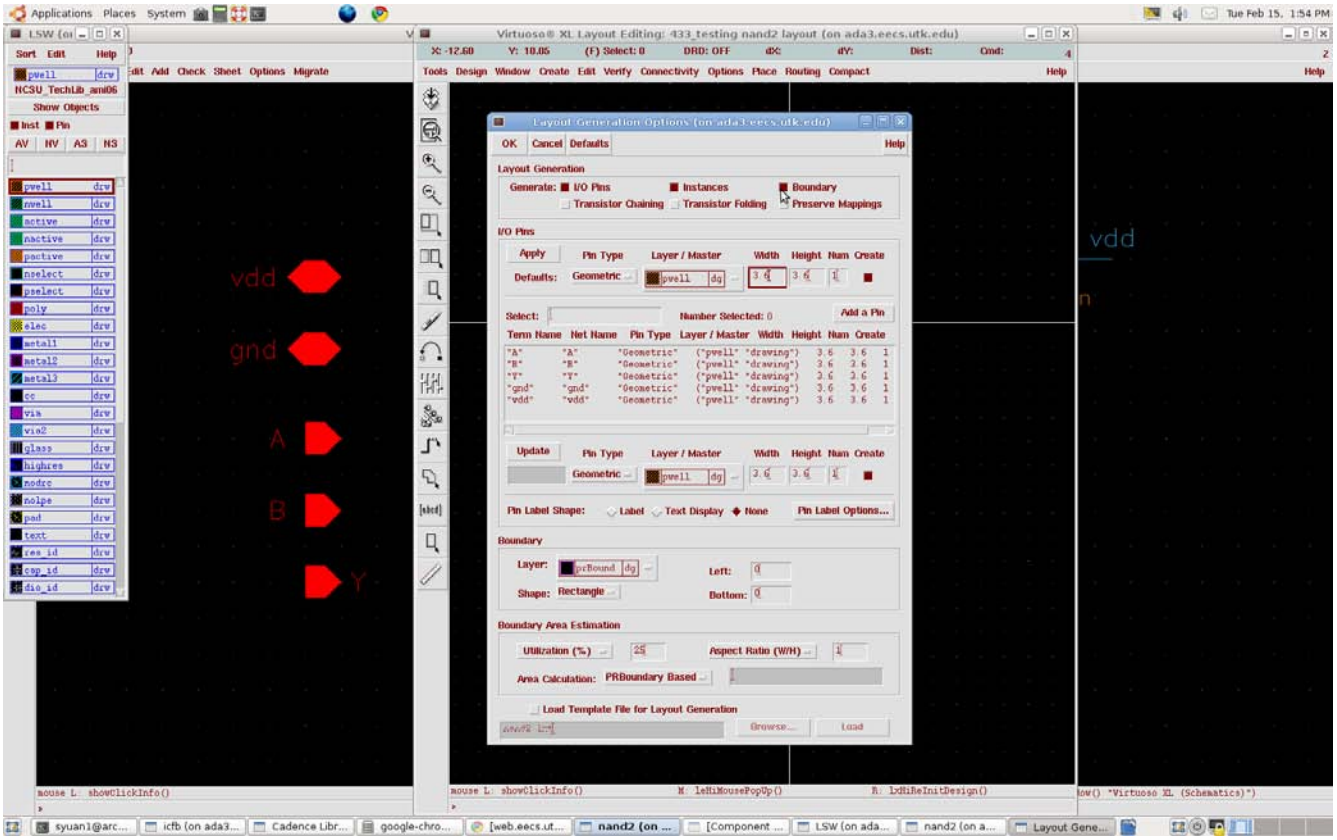


Then, The Virtuoso XL will come out.

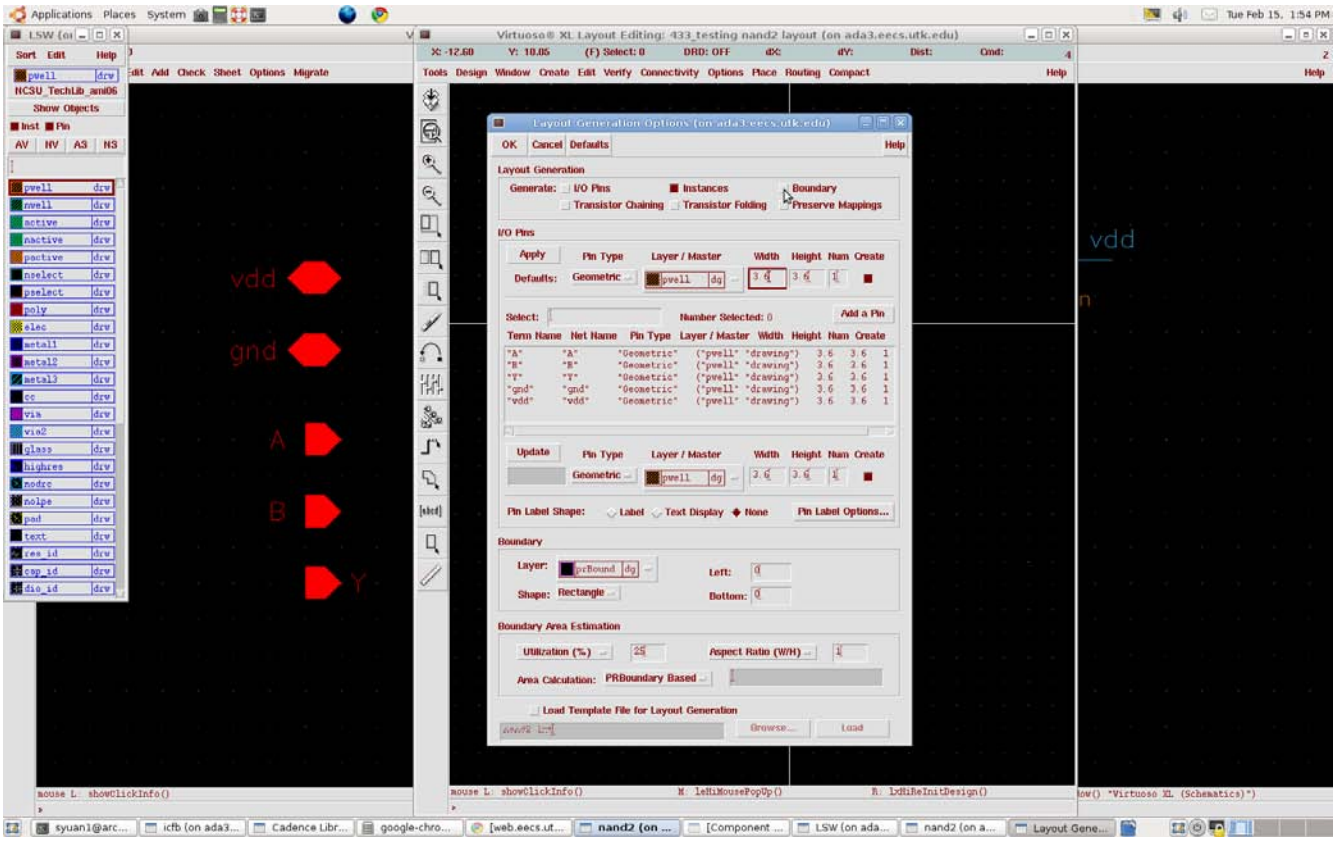




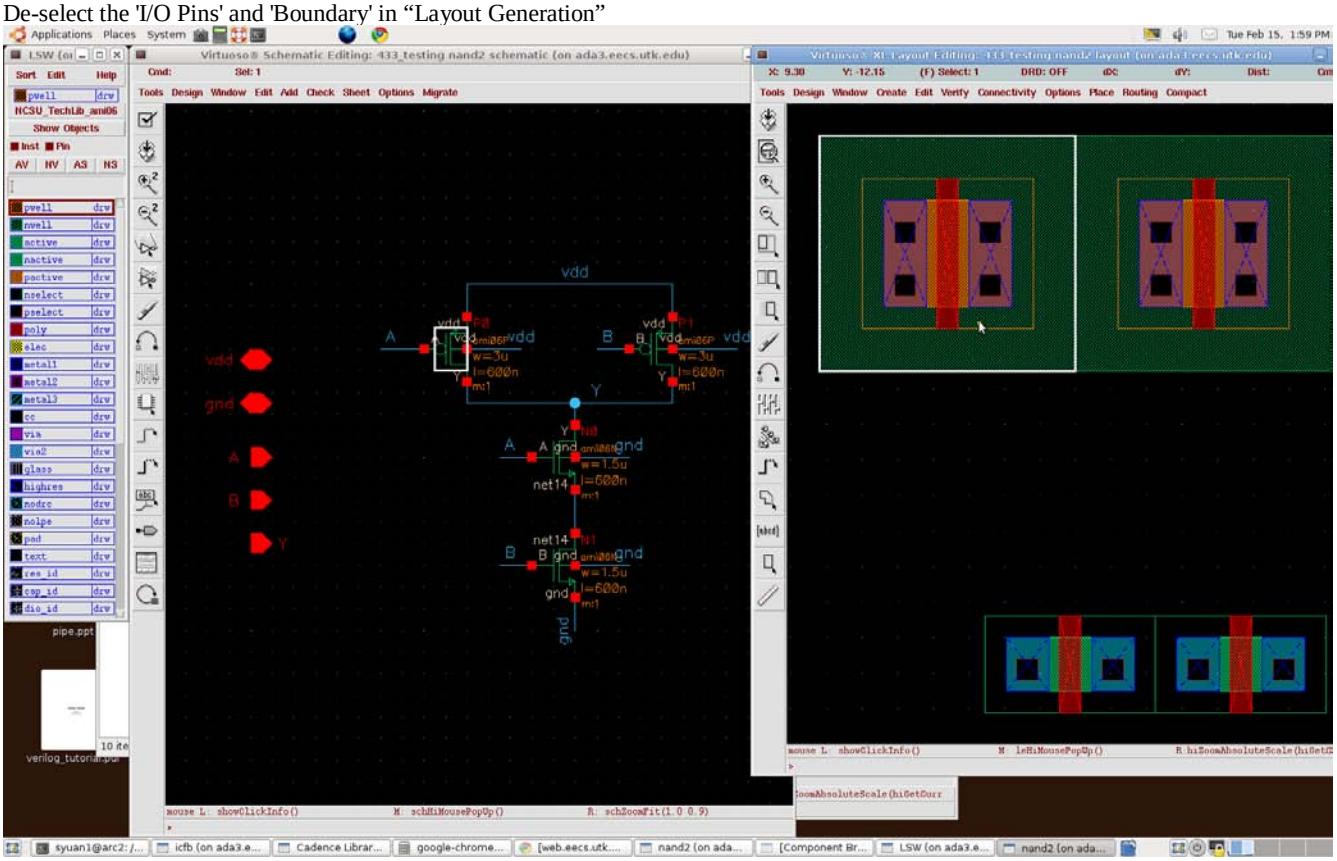
Click 'Design' ==> 'Gen From Source'



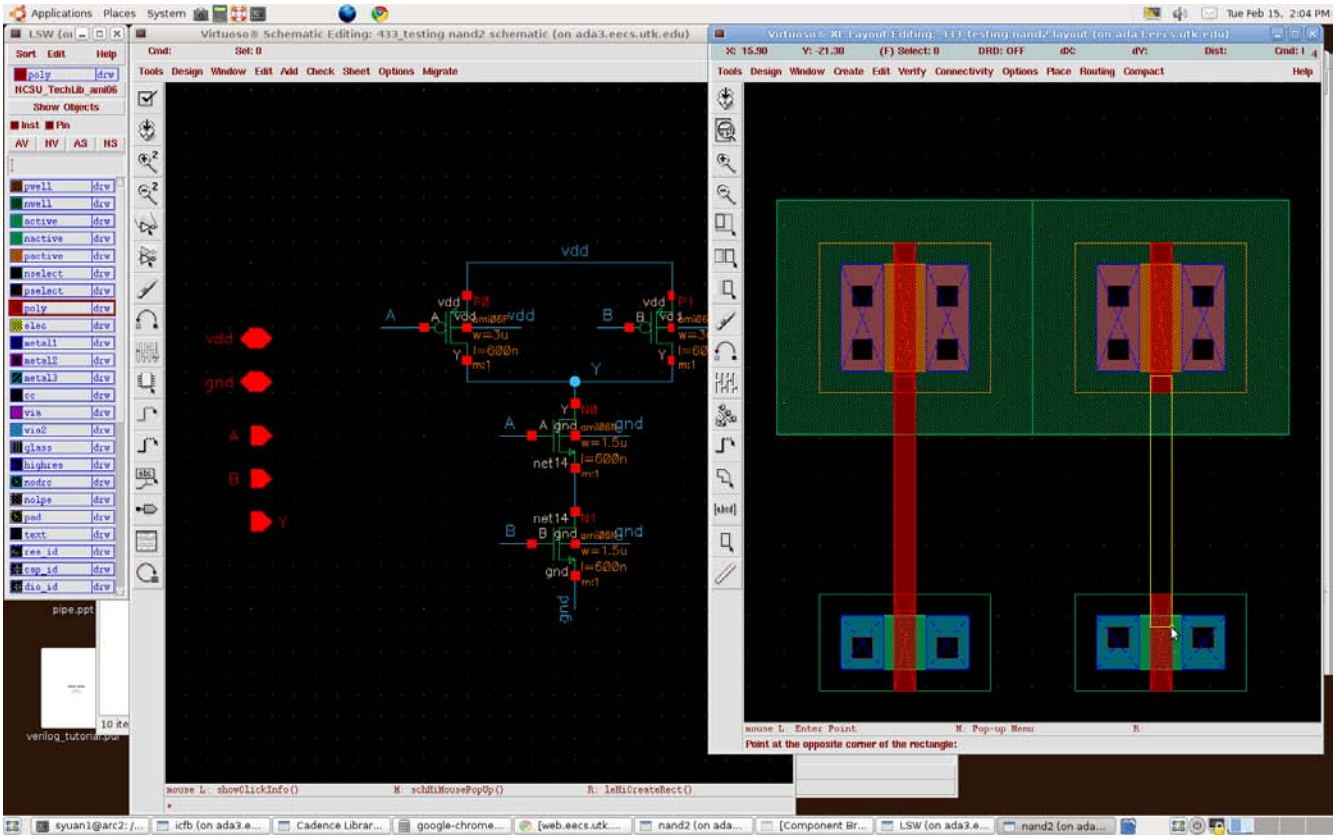
The dialog block will come out.



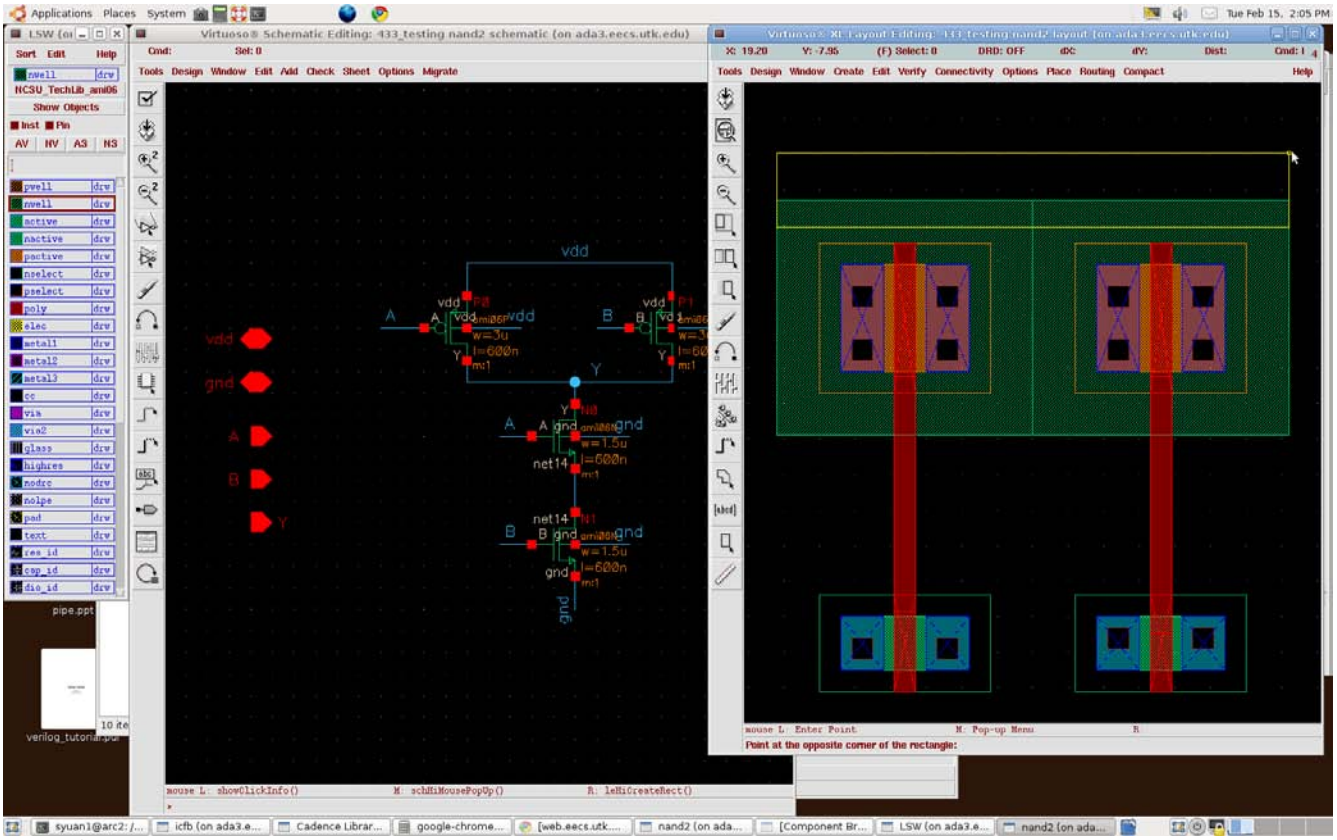
De-select the 'I/O Pins' and 'Boundary' in “Layout Generation”



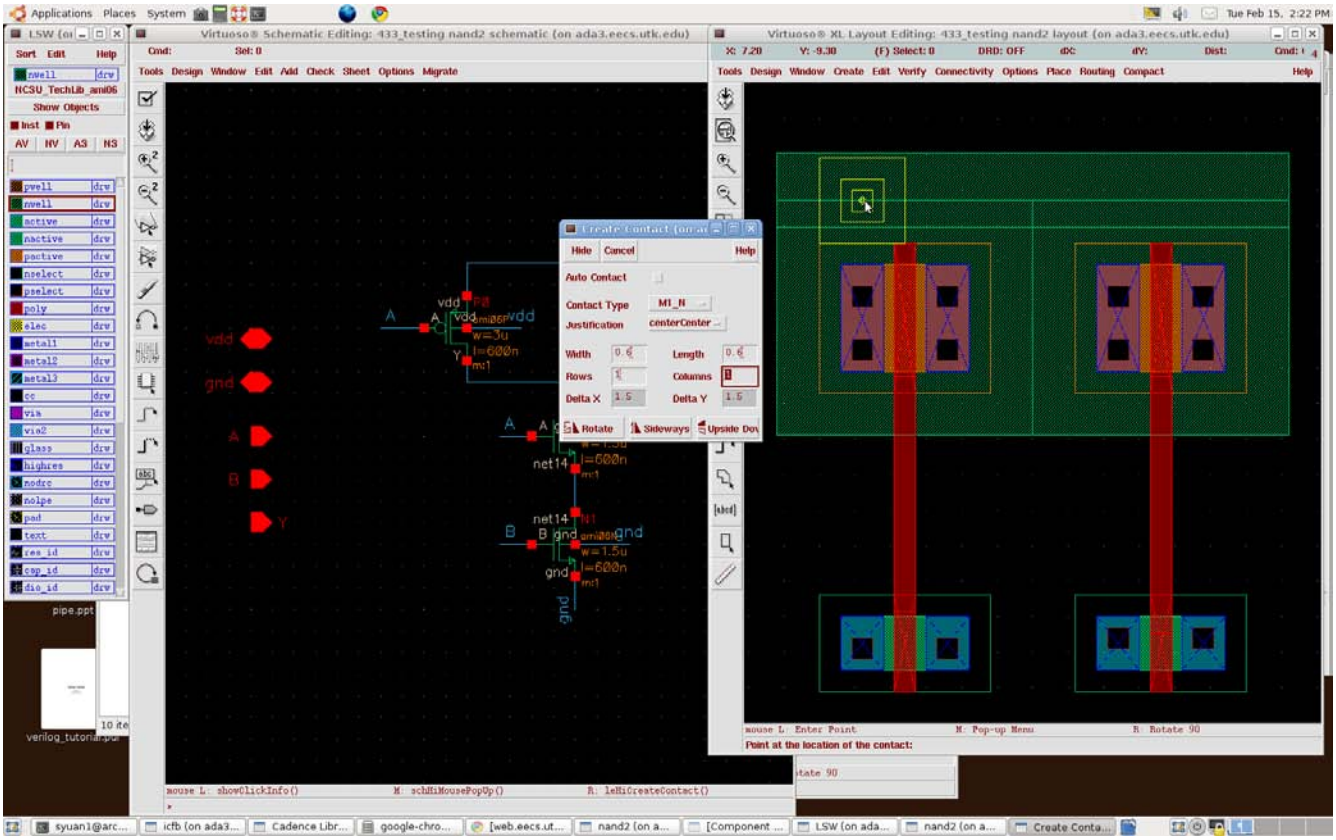
Oh yeah .... All the MOSFETs you created in schematic will show up in the 'Virtuoso XL' automatically. If you click on any one of them, a white outline will surround the MOSFET layout. And a more exciting thing is a white outline also shows on the schematic to tell you which respective MOSFET you select in schematic.

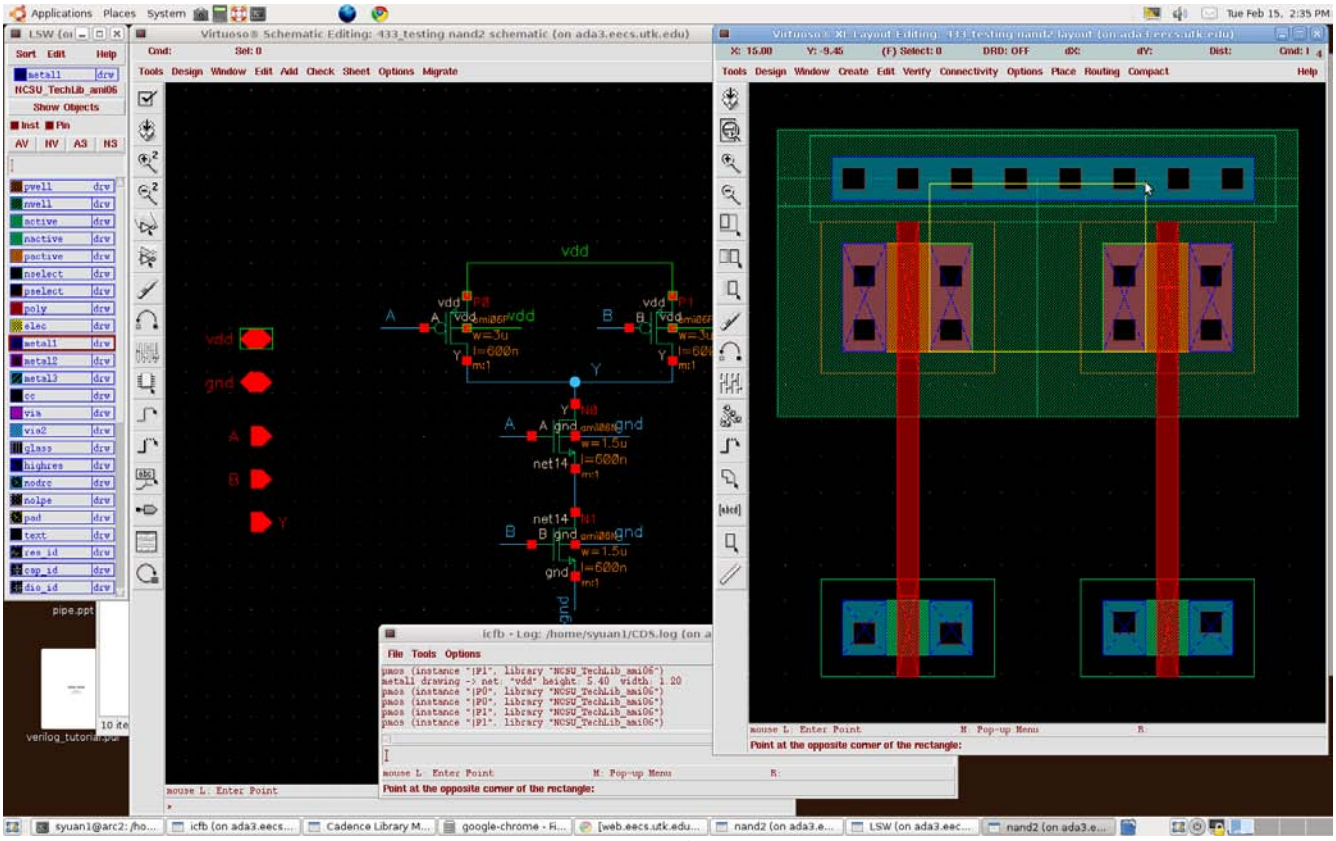


Use 'r' to create respective layer rectangles to connect the MOSFETs. Use 'm' to move the MOSFETs in proper positions. After you clicking 'm' and selecting the MOSFET, you can use your mouse's right click to rotate the MOSFET.

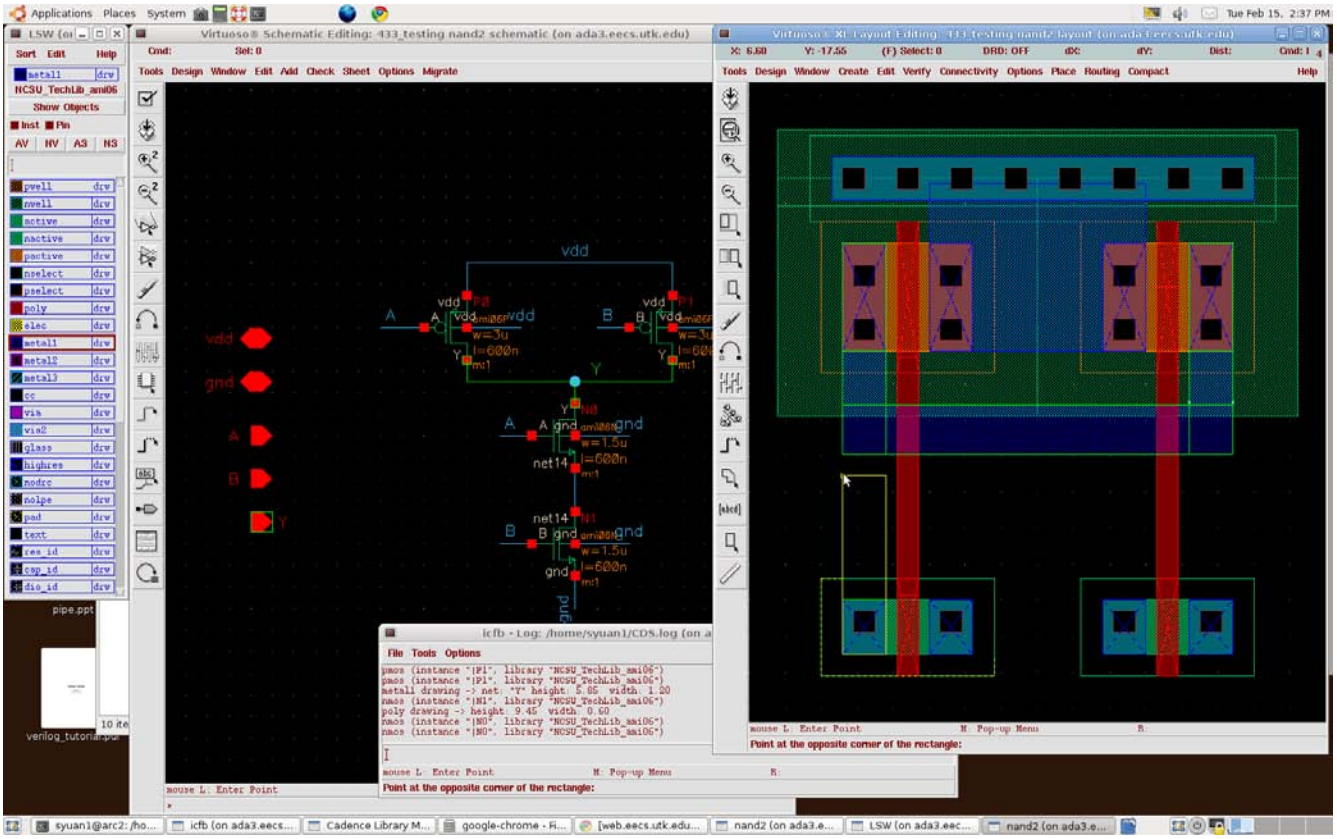


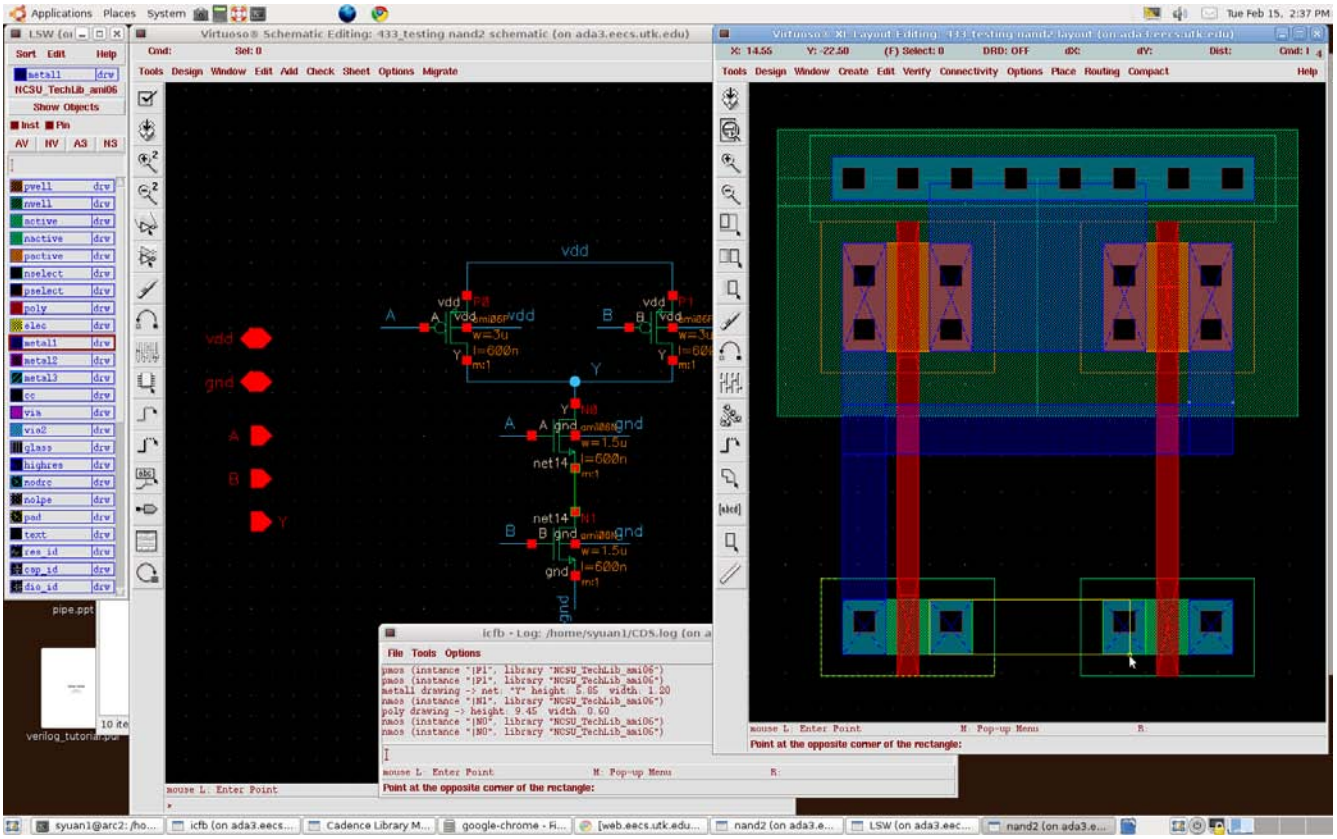
Do not forget to create body contacts for all MOSFETs!

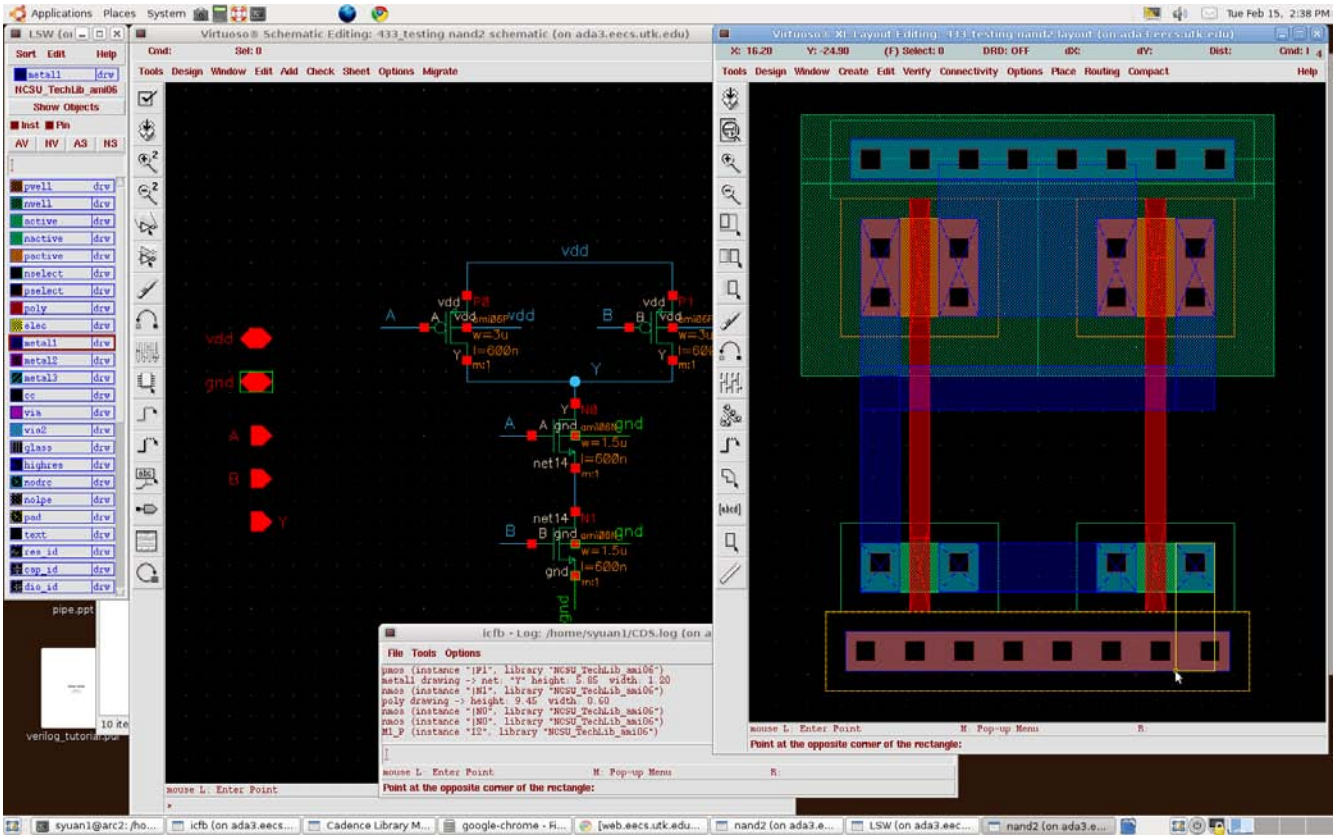


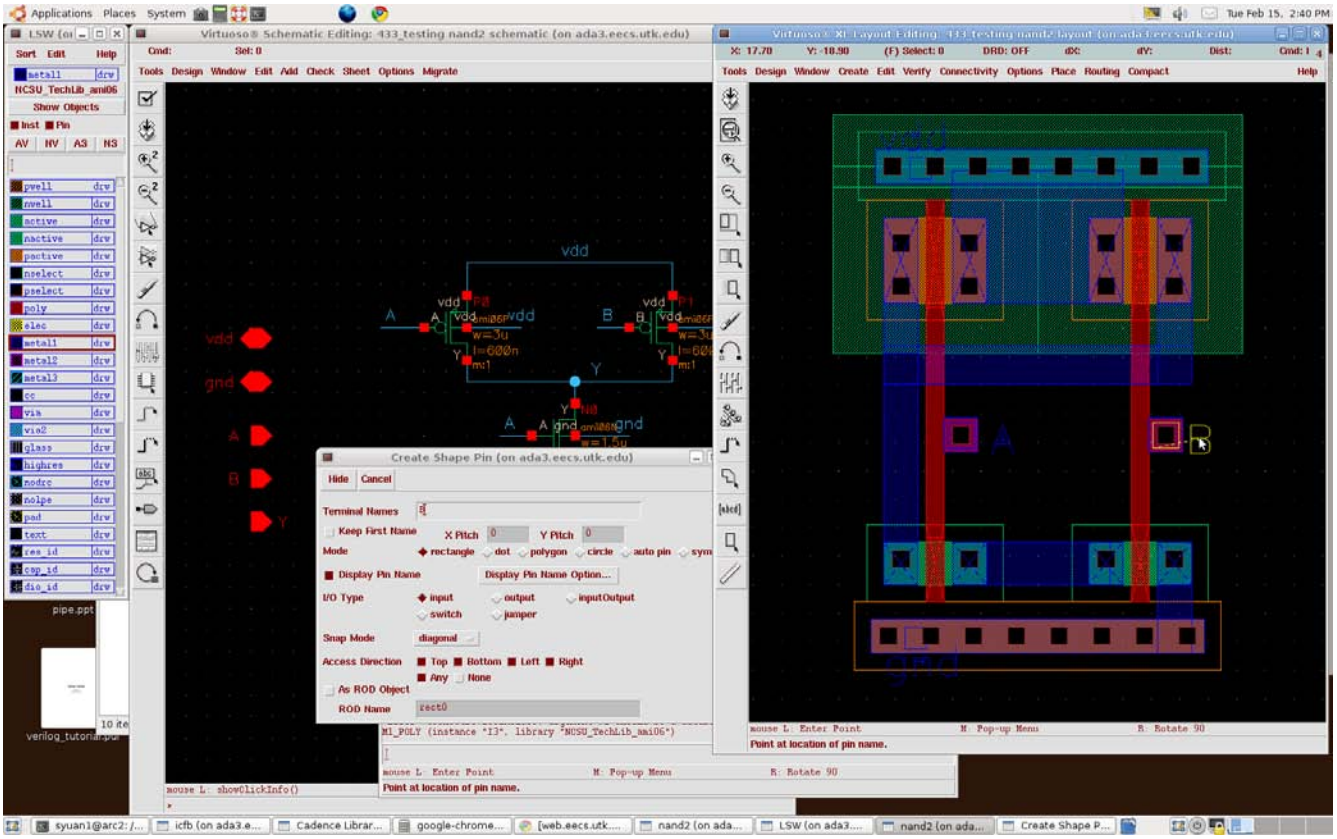


When you create rectangles and touch the source and drain terminals of MOSFETs, you will see the green outline showing out the connected netlist in both of them, the schematic and the layout.(Also shown in next four pictures.)

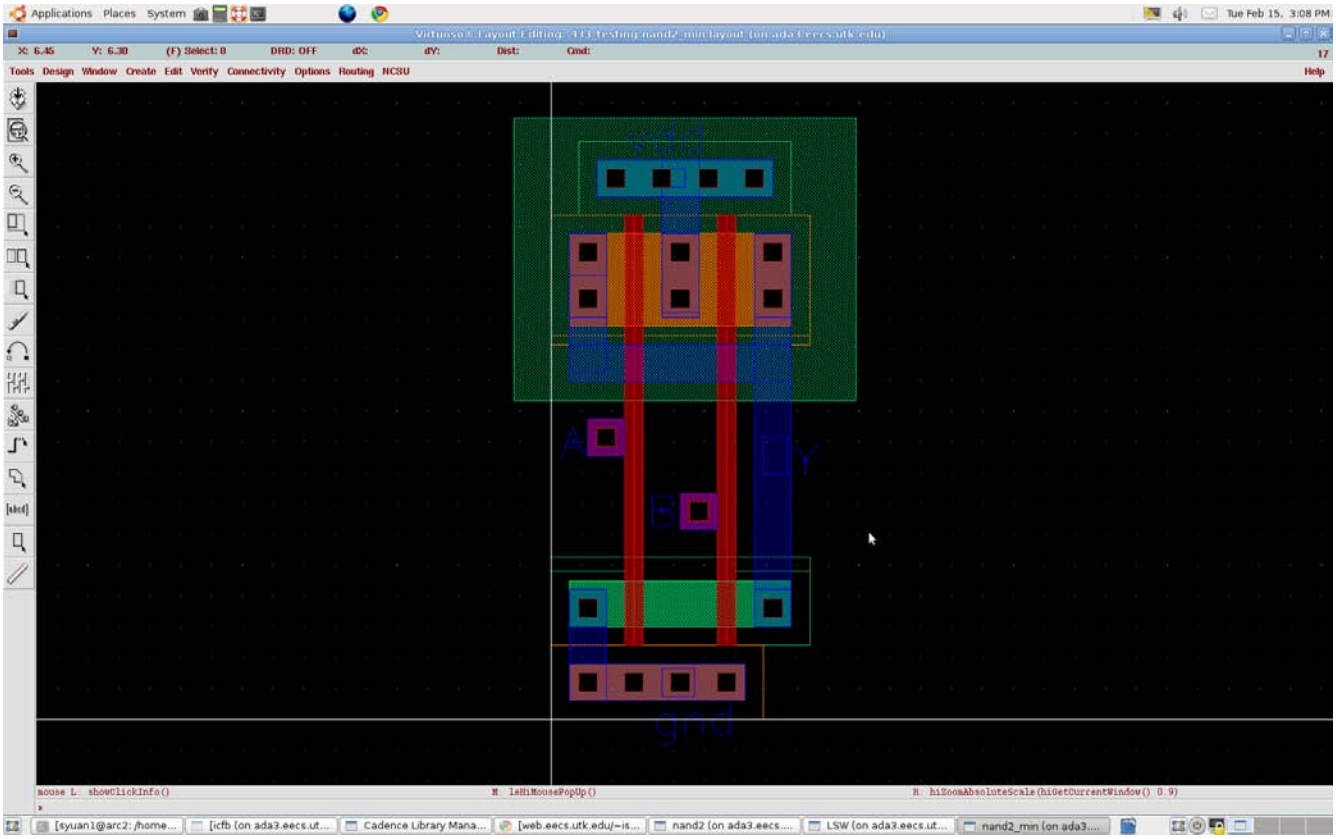

Virtuoso® Schematic Editing: 433_testing nand2 schematic (on ada3.eecs.utk.edu)
Virtuoso® XL Layout Editing: 433_testing nand2 layout (on ada3.eecs.utk.edu)
vdd
gnd
A
B
Y
net14
Point at the opposite corner of the rectangle:


Virtuoso® Schematic Editing: 433_testing nand2 schematic (on ada3.eecs.utk.edu)
Virtuoso® XL Layout Editing: 433_testing nand2 layout (on ada3.eecs.utk.edu)
vdd
gnd
A
B
Y
net14
Point at the opposite corner of the rectangle:





This should be your nand gate's final view. This is a fast and easy way to draw a layout; however the layout isn't the most compact one. Comparing with the following layout drawn by hands, you will find out two PMOSFETs share one contact connected with the vdd, and the NMOSFETs omit two contacts between two gate polly. These methods aim to reduce the sidewall and bottom parasitic capacitors which effect the performance of the circuit.


Applications Places System
Tue Feb 15, 3:08 PM
Tools Design Window Create Edit Verify Connectivity Options Routing NCSU
Help
vdd
A
B
Y
gnd
mouse L: showClickInfo()
M: leHiMousePopUp()
R: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9)