Final Project

Designing a 4-bit Counter or Flip-Flop

The final design project will require you to design a moderately complex VLSI design circuit. For this class we choose to design a Flip-flop for the Undergrad student and a 4-bit counter for Graduated Student. This project will be done **individually**.

Grad Student: Design a 4-bit Counter.

Undergrad : Design a flip-flop (J-K, T or D flip-flop) that has a Clocked Input with the option of Set/Reset, Clear or Enabled.

You need to **justify** in your presentation and Report, why you choose a particular type of flip-flop or counter. **Grading** will be done according to the quality of design.

Grading: This project will carry **20%** of the whole course.

Project grading is subdivided as follows:
25 – Project Presentation
25 – Report Writing
50 – Simulation & quality of project
100 – Total

Follow the UTK Cadence tutorial to draw a schematic of all the basic gates using the ami06 library. Use the Tutorial link

http://analog.ece.utk.edu/Cadence/utk_schematic.htm

Note that we are using AMI-0.6micron process for this final project.

Assume width, for

Length of the transistor will be 0.6 micron.

Pick up the width of p-mos and n-mos. You need to justify in the report regarding the width.

Creating the Symbol, http://analog.ece.utk.edu/Cadence/create_symbol.htm

Simulationg by Spectra http://analog.ece.utk.edu/Cadence/spectre.htm

LVS geneation http://analog.ece.utk.edu/Cadence/LVS.htm

Follow the following link to get a good example of the whole design: http://vlsi1.engr.utk.edu/~nislam/main.htm

You are required to do the following for the final project:

1. Enter a 1-bit fet-level schematic using Cadence Composer and perform pre-layout simulations

2. Use Virtuoso to produce a manual layout from the Composer schematic that conforms to the height format (any height), perform a DRC check and post-layout simulations using Spectre.

3. Students will run all simulations and generate **LVS**.

4. Rise time, Fall time, Propagation delay will also be calculated. Add capacitance to your output. Vary the Capacitance to get different delay.

Submit the plot of **delay vs Load capacitance** [use your favorite plotting tool, Matlab or Excel] .

5. Prepare the final report by capturing gif files to illustrate the layouts and simulations. Include a narrative description of your project.

6. Is there any application of your flip-flop or counter? Give details in your report.

Presentation will include all the simulation results. Rise time, Fall time, Propagation delay, plot of delay vs Load will also include in your presentation slide.