Lab 3
Create a Layout for the inverter

In this lab you will learn how to draw a layout for the inverter you created in Lab 2, and also check if the layout satisfies the design rules.

List of Useful Keyboard Shortcuts:

1. I: to add instance.
2. Q: to change the properties of an instance.
3. R: to draw a rectangle (in the layout window).
4. Esc: to cancel the current command.
5. Delete: to delete an instance.
7. Shift+K: to deactivate ruler.
8. E: to set display properties.
9. Shift+F: to view the inside of a cell.
10. CTRL+F: to go back to view the outline of a cell.
11. Shift+R: to reshape an instance.
12. P: to draw a path to connect the instances (in the layout window).

Create Layout Window (under the existing inverter cell “Inv”):

1. In lab 1, a brief introduction was given on how to create the layout window and add elements in your layout. Click on ECE433 library and click File → New → Cell View and choose “layout” as type and “Layout XL” as application.

Fig. 1. Create layout
2. In the opened layout editor window, add one NMOS and one PMOS. Press “I” and “Browse” to choose NMOS and PMOS from “NCSU_TechLib_ami06” Library. Resize the transistors by clicking on them and pressing “Q”. To view the inside of the cells, press E to open “Display Options” dialogue box and set the values of displayed levels to 10. Or you can just use Shift+F to view the inside of the cell, and CTRL+F to view only the outline of the cell.

Fig. 2 Display option window
Fig. 3. Add NMOS and PMOS to layout

**Draw the layout:**

1. The black empty layout page is equivalent to the p-type silicon, the substrate of the chip used for fabrication. Adding an NMOS means you want to create two small n plus area for source and drain and deposit silicon di-oxide and polysilicon for the gate. Similarly, adding a PMOS means you want to create an n well and two small p plus area for source and drain and deposit silicon di-oxide and polysilicon for the gate. To connect the gates of NMOS and PMOS, you can use polysilicon (poly). To do that in the “LSW” window click on “poly” to activate this layer.
Now press “R” as rectangular to start drawing a rectangular with poly that is activated layer. Click once on the layout window to mark the start node of the rectangle. Move your mouse to create any size of the rectangular you want and then click again to finalize the rectangle. To deactivate the rectangle drawing mode, press “ESC”. You can always delete elements by clicking...
on the element first and then pressing “delete”, or pressing “delete” first and then click as many elements as you want to delete, then deactivate deleting by pressing “Esc”. In “LSW” Window choose “metal 1” to connect the drain of transistors.

2. The n+p connection between the drain/source and the substrate of the NMOS creates parasitic diodes. To keep these diodes reverse biased you need to connect the body of NMOS (substrate) to lowest voltage in your circuit (GND). Similar situation arises in the p+n connection of the PMOS. Therefore, the body of PMOS (N-well) should be connected to highest voltage in your circuit (VDD). To connect one layer (in this case p-substrante or NWell) to another layer (Metal1), you can use vias. To add a via, Create → Via choose the two layers that you want to connect. For “Metal 1” and p-type substrate you can choose “M1-P” and for the Nwell to “metal 1” you can choose M1_N.

![Create Via](on ada10.eecs.utk.edu)

**Fig. 5. Add Via to the layout**

Now your layout should look like figure below:
Fig. 5. Layout of an Invertor

3. Now you need to add ports in the layout exactly in the same location as you had in your schematic. To create a pin, in your layout window click Create → Pin. The name of the pin and its I/O type should match the schematic; therefore for VDD we choose the I/O type to be input and since VDD is located at metal1 we choose Metal 1 in LSW. For input pin “in” the LSW should be changed to “poly”.
4. The final Drawing of the layout should look like Fig. 7. This layout completely matches the schematic you created in lab 2.

Fig. 7. Add Ports to layout

Fig. 8. Layout and Schematic completely match
5. Check Layout for Design Rule Violations (DRC): To check if your layout satisfies the design rules of the process, click Verify → DRC and click OK. Now look at the “icfb window”, if everything is correct and your layout does not violate any design rules, you should have zero errors. If there are errors in your layout, you can use Verify → Markers to find and explain the errors you made. Make your layout DRC clean by correcting those.

Fig. 9. Icfb window after running DRC