Lab 5

Create the Schematic, Symbol, Layout and Extracted view for the NOR Gate

This Lab is a repeat of everything you did in the previous labs for "Inverter", but this time you will create schematic, symbol, layout and extracted view for the "NOR" gate. Therefore after this lab your library manager window should look like figure 1.

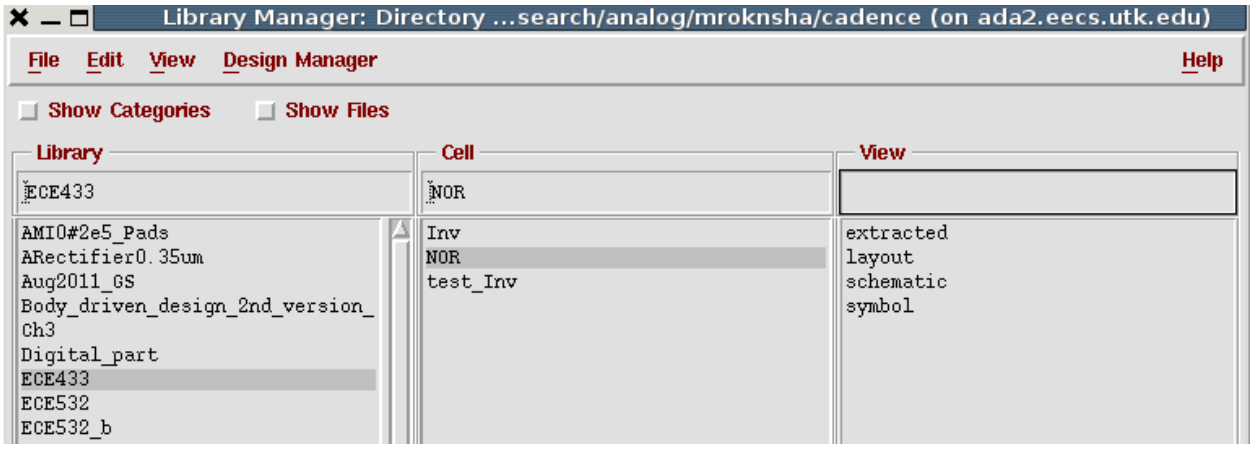

Figure 1. The new cell "NOR", with all four different views will be created in this lab

1. Create a new schematic cell view and name it "NOR", you can use the instruction in lab 2. Draw the schematic of a "NOR" gate as it is shown in figure 2.

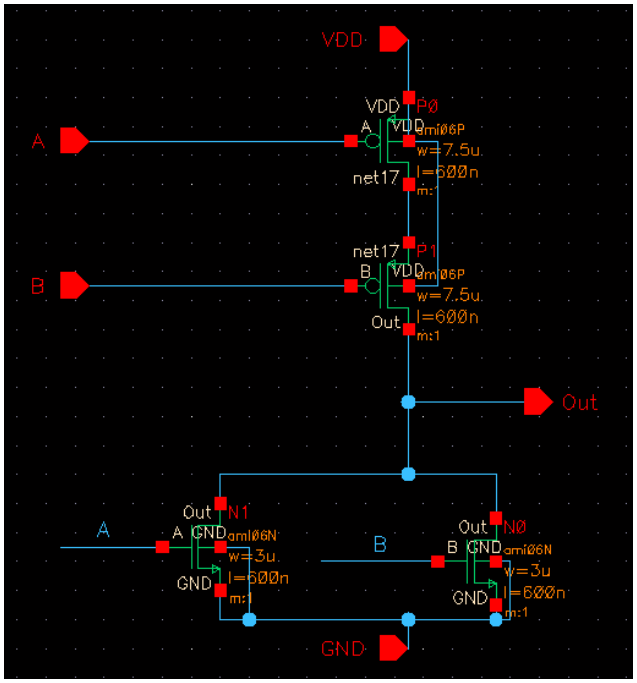

Figure 2. Schematic of a "NOR" gate

2. Create a Symbol from the schematic following the instructions in lab 2. The symbol should look like figure 3.

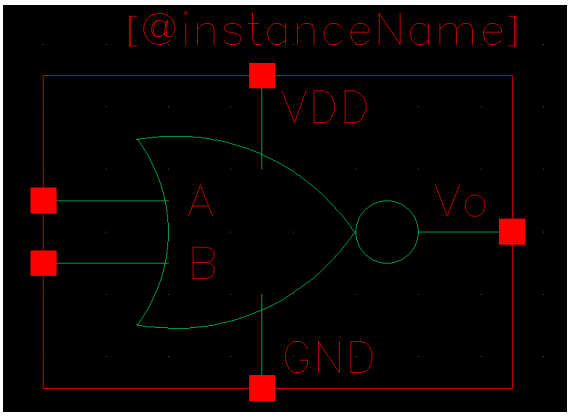

Figure 3. NOR Symbol

3. Create a new layout cell view following the instructions in Lab 3. Draw the "NOR" gate layout. The final layout should look like figure 4. (There are some important notes in the next page that you need to read before starting the layout). Get your layout DRC clean.

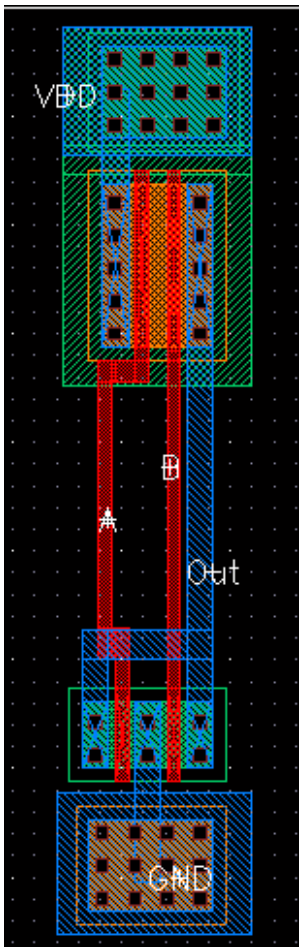

Figure 4. layout of a "NOR" gate

There are some important notes in the layout that you have to pay attention to.

1. If you want to create a multiplied transistor or a fingered transistor as shown in figure 4, you can change the properties of the transistor as it is shown in figure 5 and 6.

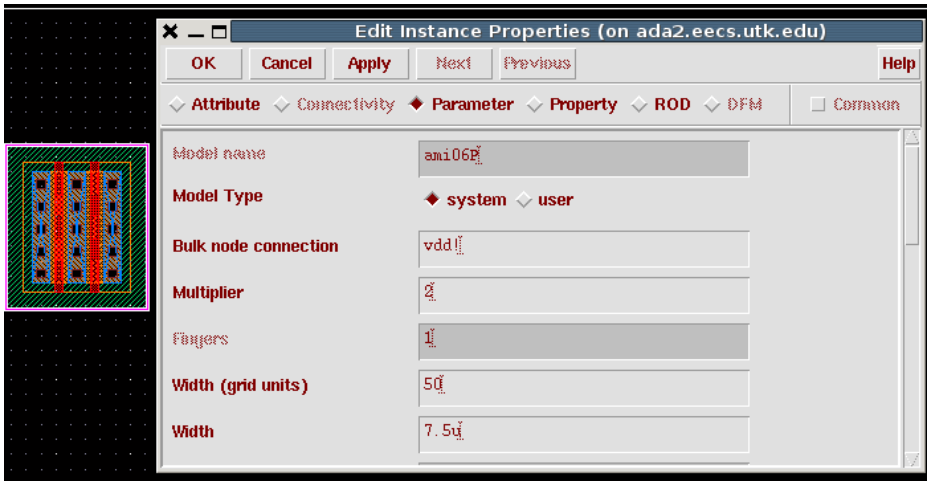

Figure 5. Change the transistor parameter to create multiplied transistor

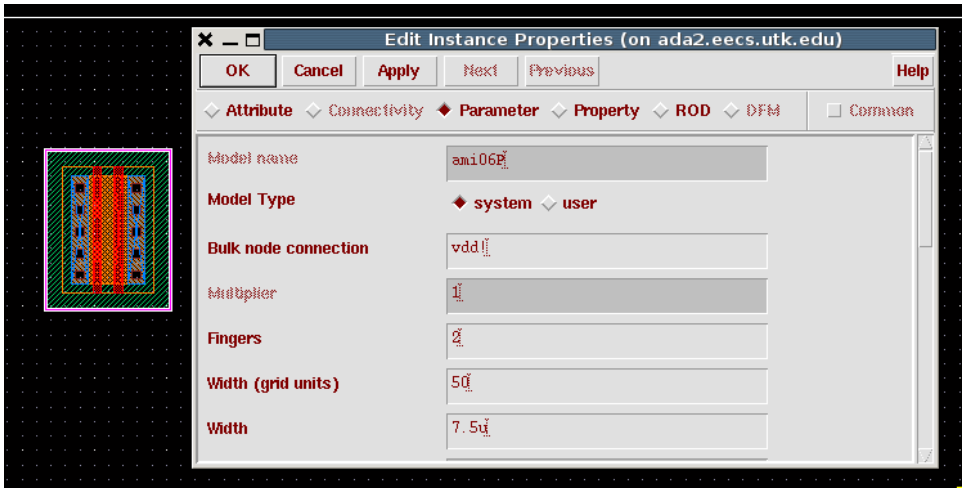

Figure 5. Change the transistor parameter to get fingered transistor

2. You need to leave enough space between the poly that connects the gates of transistors so that you are able to add via to this poly. You can use other layers of metal for connection. As an example, figure 6 shows a connection between two “NOR” gates. This connection can be possible with the help of via (poly-metal1) and (metal1-metal2).

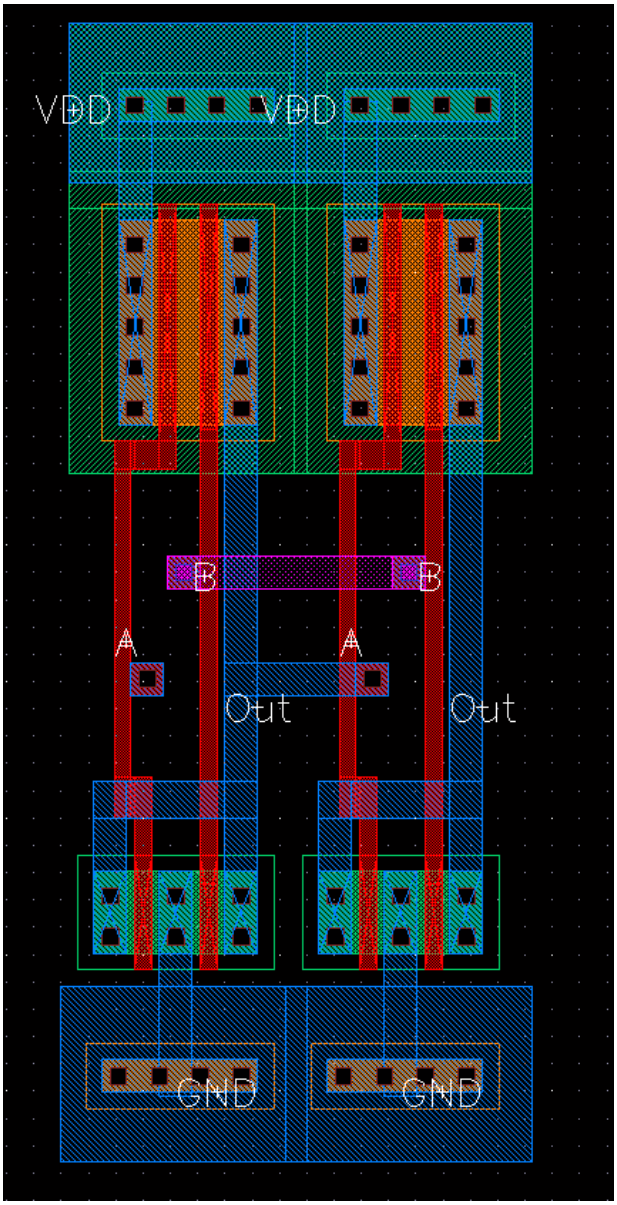

Figure 6. In the next lab you will need to make connections between your gates. It is wise to leave some area for this connection.

4. Create extracted cell view using the instructions for lab 4 and get the LVS clean for the “NOR” gate.