Lab 7

Create the Schematic, Symbol, Layout and Extracted for “MUX”

This Lab is about designing a “MUX” which contains all of the gates you previously designed.

Schematic and Symbol of the MUX

Use your own digital gates to create a MUX. Your MUX should look like figure 1. Create a symbol for this MUX as it is shown in figure 2.

Figure 1. The schematic for a 2_1 Mux

Figure 2. The symbol for a 2_1 Mux
Layout for the MUX

1. Create a layout page. Use “I” to bring the required gates in to this page.

2. Use “Shift+F” to see inside your gates. Align your gates and resize them if required. It is better to have them all almost in the same height.

3. Use “Metal1” and “Nwell” to cover over all the GND, VDD and Nwell area. It should be DRC clean.
4. To display the pins you created before, from “create → pin” activate “Display pin Name” and then press “cancel”.

5. Look at your schematic; each of the gates has a name. You can choose which one of your gates in layout matches the gates in your schematic. The figure 6 shows just one selection you can choose your own set of positioning for the gates. These selections will be used for the rest of this instructions set.
6. In your schematic the port “In” of gate I3 is connected to the port “B” of gate I0. Therefore we need to create the same connection. Figure 7 shows this connection by using metal2 which is one layer above metal1. Therefore there would be no connection between metal1 and metal2 unless you add a via named “M1_M2” between them. For a connection between poly and metal2, you need to add two via “M1Poly” and “M1_M2”. The demonstration of what is happening in this connection is shown in figure 8.
7. Complete all the other connections for this layout to design the MUX.

![Figure 9. Layout for the Mux with all the connections](image)

8. Add pins in the layout based on your schematic. You can increase the size of pins name and make them different than the gates pin name by clicking on “Display Pin Name option” and choose a bigger number.

![Figure 10. Increase the pin name size](image)
9. Figure 11 shows the final layout for this Mux, do DRC and LVS for your layout.

![Figure 11. Final layout of the Mux](image1)

10. Run the simulation and post layout simulation for your “MUX” using the testbench shown in figure 12. In this test bench v1 is has a pulse width of 100n with period of 200n, v2 has a pulse width of 10n with period of 20n and v3 has a pulse width of 5n with period of 10n. all of them changing from 0 to 5. You should run the simulation for 400n, the output should look like figure 12.

![Figure 11. Test bench for testing the “MUX”](image2)
Figure 12. Output result of the simulation