Laboratory 8 (for Honors Students)

Introduction to 45 nm process in Cadence 6

In this lab, you will be familiarized with a 45 nm technology using Process Design Kit (PDK) in Cadence platform 6. A PDK is a set of files used within the semiconductor industry to model transistors for a certain technology for a certain foundry, different kinds of libraries to be used with design software tool. Cadence 6 is installed in the Ada systems (ada6 through ada11).

Part 1: Setting Up Cadence

You need to do the initial set-up only once.

1. Log into the server
   a) Access the terminal in Linux from **Applications > Accessories > Terminal**.
   b) Type **ssh –Y ada7.eecs.utk.edu** (NB: You can use ada7 to ada11).
   c) Log in to the server.

2. Copy model files of cadence 45 nm process
   Type in the terminal
   mkdir model45
   cd model45
   cp ~analog/webhome/cadence_45/gpdk45nm.m . (NB: Don't miss the dot after .m).

3. Copy set-up files of cadence 45 nm process
   Type in the terminal
   cd
   mkdir cadence_45
   cd cadence_45
   cp ~analog/webhome/cadence_45/.cdsinit .
   cp ~analog/webhome/cadence_45/cds.lib .
   cp ~analog/webhome/cadence_45/common_bindkeys.il .
   cp ~analog/webhome/cadence_45/source4virtuouso .

4. Starting up cadence
   Now that you have copied all the set-up files, you can start cadence by typing in the terminal
   source source4virtuouso
   You will see that in the terminal it says,
   cds.lib was found. [(I)gnore/(O)verwrite/(A)ppend]?
   Press A to append.
   [NCSU PDK] cds.lib/.cdsinit/lib.defs found. [(I)gnore/(O)verwrite/(A)ppend]?
   Press A to append.
   [OSU PDK] cds.lib/lib.defs found. [(I)gnore/(O)verwrite/(A)ppend]?
   Press A to append.
   Then type in the terminal

virtuouso&

Cadence will start, and Virtuoso 6.1.4 Window will be opened before you.

Once you have performed the initial setup, you can just log into the server, go to your cadence_45 folder and follow step 4 to start cadence.

Part 2: Drawing Inverter Schematic

1. From the library manager, create a library named "ECE433" using "**File > New > Library**". Attach this library to the existing tech library "NCSU_TechLib_FreePDK45".

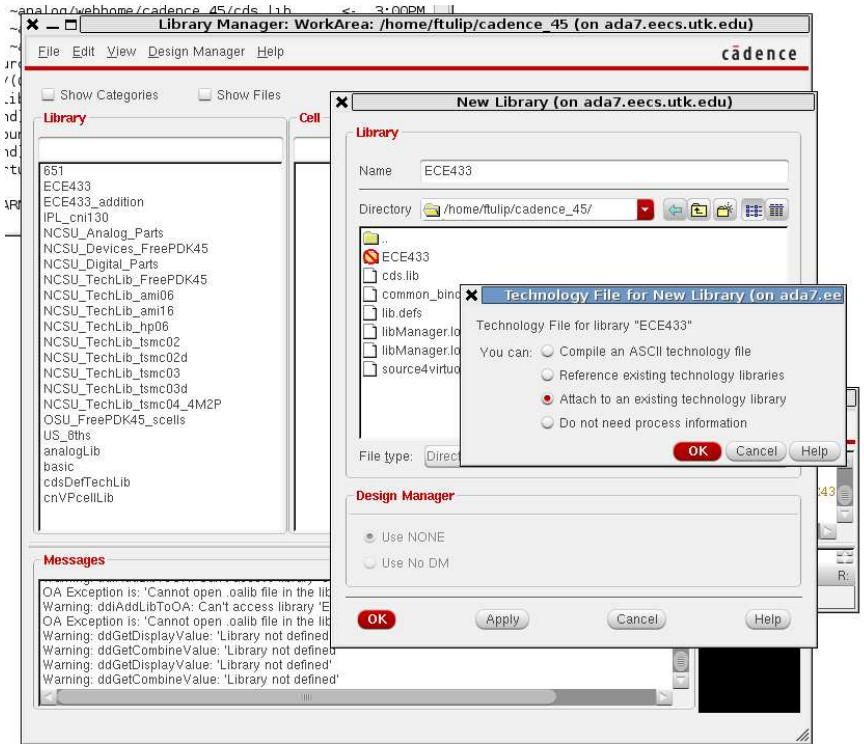

Figure 1: Creating new library in cadence 6.

2. Select the library ECE433 and then create a schematic using "**File > New> cell view**" and name it "Inv". Make sure that the type is selected as "Schematic" and application is selected as "Schematics L".

3. In your Schematic window press "I" to add instance. Add one NMOS (NMOS_VTL) and one PMOS (PMOS_VTL) from the library "NCSU_Devices_FreePDK45".

4. Change the properties of the transistors by pressing Q. For p-type transistor, set W=500 nm, L=50 nm, which gives an aspect ratio (W/L) of 10. For n-type transistor, set W=250nm, L=50 nm, so, the aspect ratio is 5.

5. Based on the inverter schematic, you need to connect the gates and the drains of the NMOS and PMOS together. You also need to connect the body of NMOS and PMOS to their sources. Press “W” to activate wire to make these connections. (Do not forget the connection of NMOS and PMOS body.)

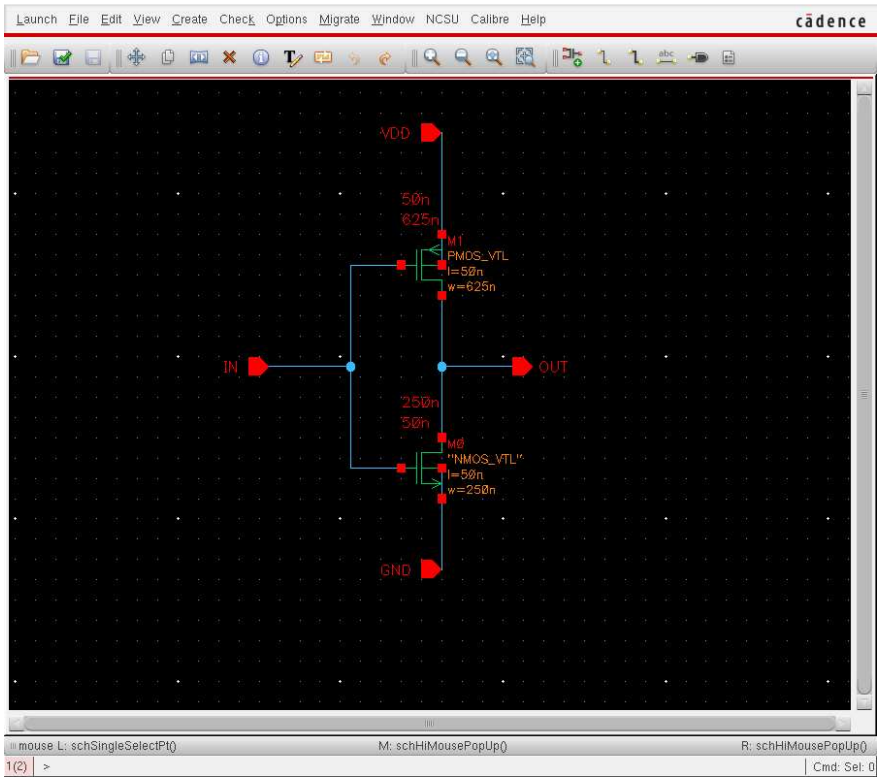

Figure 2: Schematic of the inverter.

6. Pins are used to create accessibly to the nodes inside the schematic that we need after creating the symbol. To add a pin, press “P”. In the newly opened window, write “VDD” to be the pin name. Choose the direction of VDD to be input. Add “GND” and “In” port in the same way. For the pin “Out” choose the direction to be output. The final Schematic should look like figure 2.

7. Click on “check and save” button on the top left of the toolbar. You should have no error or warning.

Part 3: Creating Inverter Symbol

1. In your Schematic window, go to “**Create > Cellview > from Cellview**” and click OK. A new window will open with options for symbol generation. Here you can the set positions of the pins as you desire, as shown in figure 3. Click OK.

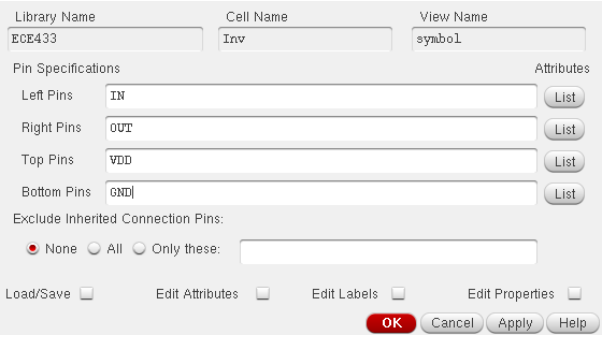

Figure 3: Direction of pins in the inverter.

2. A new window will open with a rectangular box and the pins as you directed. This is the default symbol created for your circuit. You can make it look like the familiar look of the symbol "Inverter". You can use the drawing components that look like square or circle on the toolbar at top of the page. Final Figure should look like figure 4. (Do not forget to save it.)

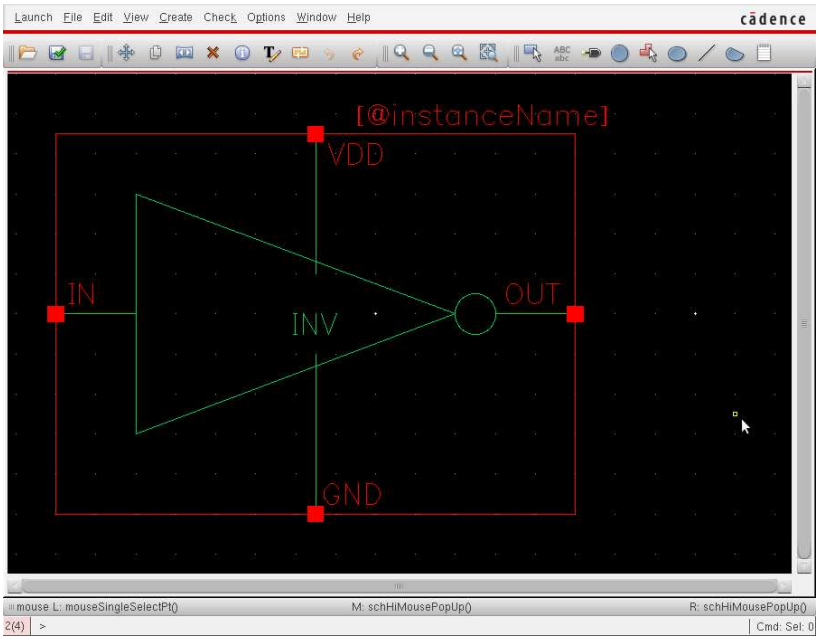

Figure 4: Symbol of the inverter.

Part 4: Drawing Inverter Layout

Instead of drawing an inverter layout from the scratch, we will use a standard inverter cell layout from the library and compare it with our schematic.

1. Create a new layout cellview for the inverter from "**File > New> cell view**". Select type "layout" and application "layout L".
2. Call a standard Inverter cell from OSU_FreePDK45_scells library. Press 'I', then browse to find "**OSU_FreePDK45_scells > INVX1 > layout**".

3. Create pins according to your schematic from "**Create > Pin**". Make sure that in your LSW window, you have **metal1**selected, and follow figure 5 to add the pins. Also, click on Display terminal name, and in the newly opened window, select **metal1** as layer. You have to click 3 times to add any pins.

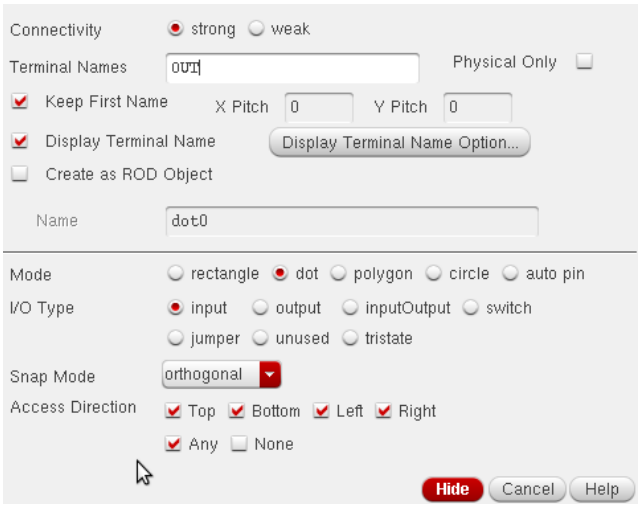

Figure 5: Creaing pins.

4. Your final layout should look like figure 6.

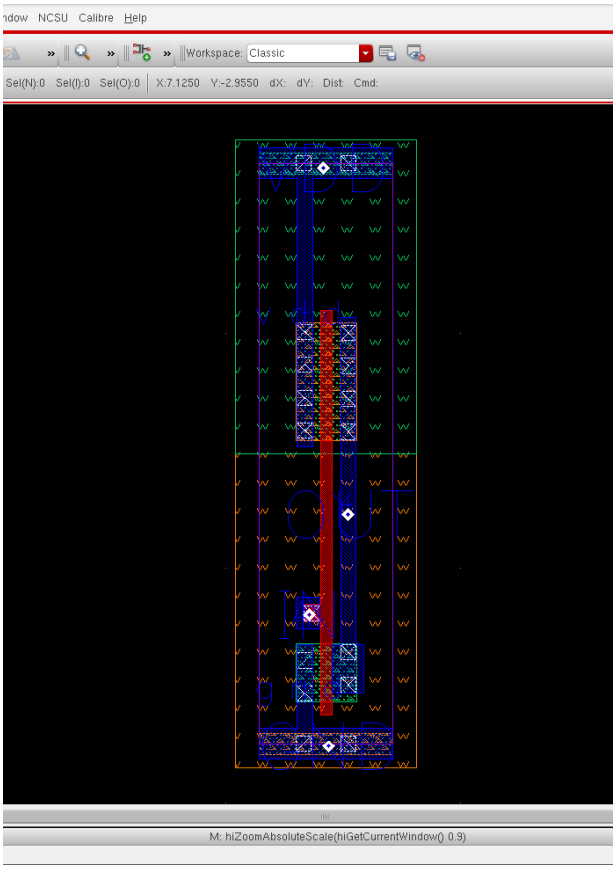

Figure 6: Layout of the Inverter.

5. To check any design rule violations, click on "**Calibre > Run DRC**", then click on the **Run DRC** button. If you have done every step correctly, you will get no errors, like figure 7.

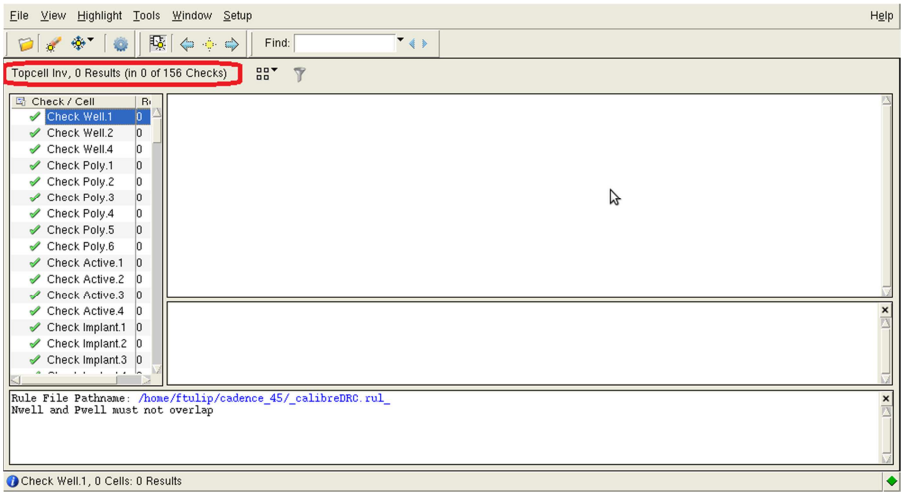

Figure 7: No DRC violation.

6. To compare the layout with your schematic, click on "**Calibre > Run LVS**". Make sure that in the Netlist tab, "Export from schematic viewer", and in the Layout tab, "Export from layout viewer", both are checked on. Then click on the **Run LVS** button. If you have done every step correctly, you will see a smiley face saying the LVS was correct.

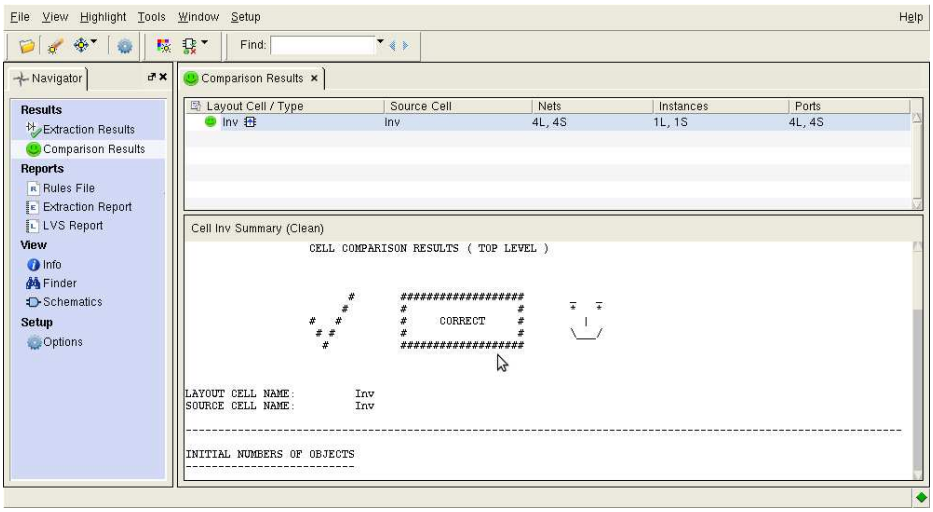

Figure 8: LVS comparison results.

7. If for some reason you do not get the LVS correct, you can click on the errors in the Comparison Results tab, and follow it to track the errors in both layout and schematic.

Part 5: Creating Test Bench to Simulate the Inverter

1. In your Library create a new schematic and name it "test_Inv". In this schematic window, press "I" to insert the inverter symbol you created. So, in the library part choose your own library "ECE433" and from this library choose "Inv". Click on the schematic page to have your inverter there.

2. To test the behavior of this circuit, you will need a supply voltage, a pulse generator and a ground for the reference of your simulation. To get these parts, press "I" and select the "**NCSU_Analog_Parts**" Library. In this library click on the "**Voltage_Sources**" and select "Vdc". Choose 5V for the DC voltage. From the same library choose "**Voltage_Sources** > **Vpulse**" and choose the parameters from figure 9.

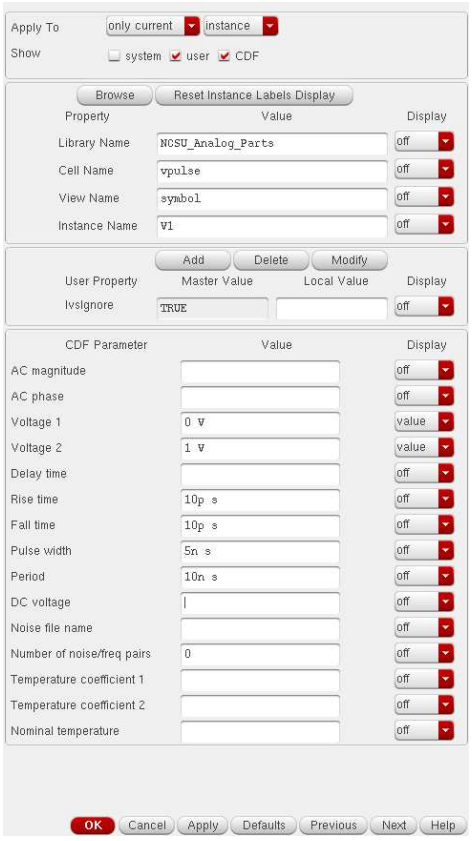

Figure 9: Parameters for Vpulse.

3. To define the nets VDD and GND in the "**NCSU_Analog_Parts**" Library choose "**Supply_Nets > vdd**". Add this symbol on top of the inverter and the DC voltage. Then from the same library choose "**gnd**" and connect it to all the grounds in your schematic. Click "ESC" to close the window. Your final circuit should look like figure 10.

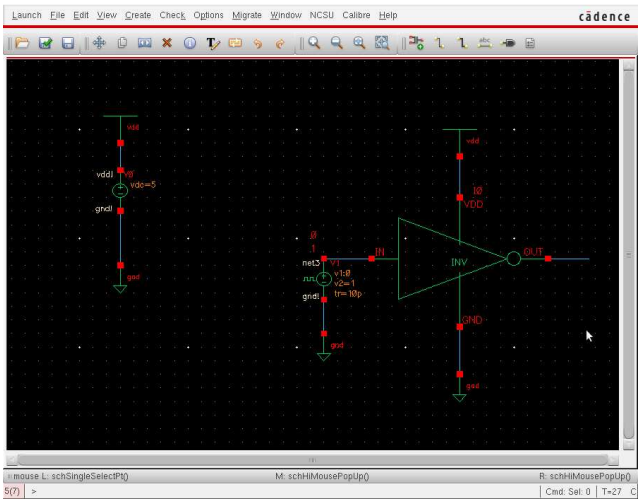

Figure 10: Test Bench schematic for inverter.

Part 6: Simulation

1. To start Simulation choose "**Launch > ADE L**". In the newly opened window click on "**Setup > Simulator/Directory/Host**". Choose "**spectre**" as your simulator.

2. To add the model library, click on "**Setup > Model Libraries**", then browse to find "gpdk45nm.m".

Figure 11: Adding model library.

3. Click "**Analyses > Choose**" and select the parameters as follows:

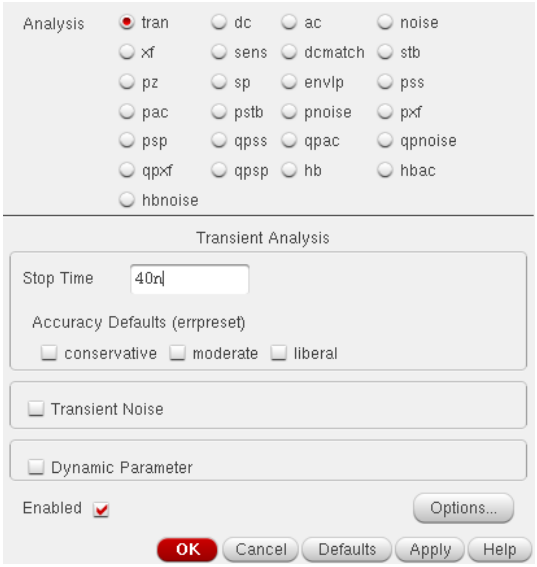

Figure 12: Setting up transient analysis.

4. To choose the nodes of which you want to see the response click "**Output >To Be Plotted> select on Schematic**" and then click on the wire input and output (nodes IN and OUT).

   Pay attention that if you click on nodes it will draw a circle around that node showing that you want to plot the current passing through that node. But in this lab you need to plot the voltages, and therefore you need to click on wires and not nodes.

5. Now Click "**Simulation> Netlist and Run**". You should see the input and output in one window like below.

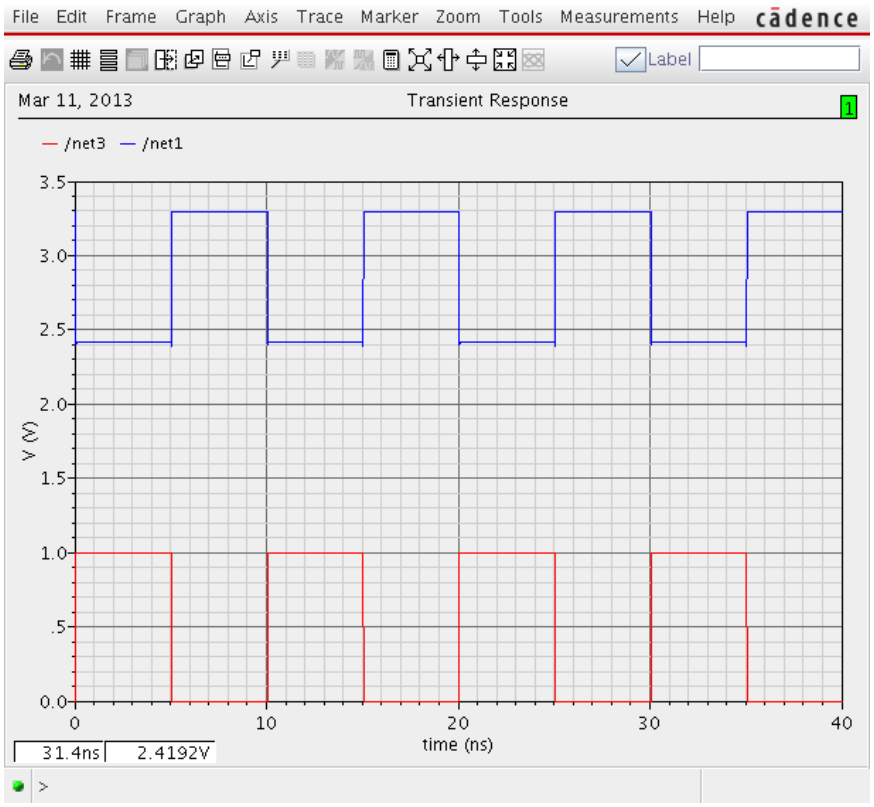

Figure 13: Simulated inverter input and output plots.

You can change the color of the background and plots by double clicking on them.