Design of a D Flip-Flop

Final Project
ECE 433
Why a D Flip-Flop?

- Preferred type for integrated circuit applications
  - One input
  - Fewer transistors leading to less delay
- SR Flip-Flop has indeterminate state when both inputs are high
- JK Flip-Flop keeps two inputs

- Designed a positive-edge-triggered D flip-flop with asynchronous set and reset signal
  - $S = 1$, $Q$ goes to 1
  - $R = 1$, $Q$ goes to 0

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>D</th>
<th>CLK</th>
<th>Q</th>
<th>~Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Rising</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Rising</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>0</td>
<td>$Q_0$</td>
<td>$\sim Q_0$</td>
</tr>
</tbody>
</table>
Building Blocks

- \((W/L)\rho = 7.5\mu m/0.6\mu m = 12.5\)
- \((W/L)n = 3\mu m/0.6\mu m = 5\)
- 6 Three-Input NAND Gates
- 2 Inverters
D Flip-Flop Layout, Schematic, & Symbol
Simulation: Pre-Layout
Simulation: Post-Layout
Rise Time, Fall Time, & Delay

- Rise Time = 1.9ns
- Fall Time = 12.3ns

Load Capacitance Versus Delay

<table>
<thead>
<tr>
<th>Load Capacitance (pF)</th>
<th>Average Propagation Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.3</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>2.6</td>
</tr>
<tr>
<td>4</td>
<td>3.2</td>
</tr>
<tr>
<td>5</td>
<td>3.6</td>
</tr>
</tbody>
</table>

Load Capacitance Compared to Delay

![Graph showing relationship between load capacitance and delay](image)
ECE 433 Project
D Flip Flop
Choice of D Flip Flop

- Before Project
  - Input = output; how can that be useful?
  - How does it work?

<table>
<thead>
<tr>
<th>D</th>
<th>Q_{n+1}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

- After Project
  - Uses I Learned About
    - Delays output by one clock pulse
    - Memory storage, registers
    - Solving glitches in counters

- Design Choice
  - As few transistors as possible (minimize chip area)
D Flip Flop Schematic

Inputs: D, CLK

Outputs: Q, Q_Bar
D Flip Flop Layout

Measurements: 39.9 microns x 45.6 microns
Simulation Results

- Schematic (Pre-Layout) Simulation
- Post-Layout Simulation
Effects of Capacitance

Capacitance vs. Rise Time

\[ y = 1.294x + 0.048 \]
\[ R^2 = 0.99997 \]

Capacitance vs. Delay

\[ y = 2.045x + 0.369 \]
\[ R^2 = 0.99981 \]

Capacitance vs. Fall Time

\[ y = 3.375x + 0.091 \]
\[ R^2 = 0.99993 \]