MOS Transistors as Switches

\[ \text{G (gate)} \]
\[ \text{D (drain)} \]
\[ \text{S (source)} \]

**nMOS transistor:**
Closed (conducting) when Gate = 1 (V\text{dd})
Open (non-conducting) when Gate = 0 (ground, 0V)

**pMOS transistor:**
Closed (conducting) when Gate = 0 (ground, 0V)
Open (non-conducting) when Gate = 1 (V\text{dd})

For \text{nMOS switch}, source is typically tied to ground and is used to *pull-down* signals:

\[ \text{G} \]
\[ \text{Out} \]
\[ \text{when Gate} = 1, \text{Out} = 0, (\text{OV}) \]
\[ \text{when Gate} = 0, \text{Out} = Z \text{ (high impedance)} \]

For \text{pMOS switch}, source is typically tied to V\text{dd}, used to *pull* signals *up*:

\[ \text{G} \]
\[ \text{S} \]
\[ \text{Out} \]
\[ \text{when Gate} = 0, \text{Out} = 1 \text{ (V\text{dd})} \]
\[ \text{when Gate} = 1, \text{Out} = Z \text{ (high impedance)} \]

Note: The MOS transistor is a symmetric device. This means that the drain and source terminals are interchangeable. For a conducting \text{nMOS transistor}, V_{DS} > 0V; for the \text{pMOS transistor}, V_{DS} < 0V (or V_{SD} > 0V).
The CMOS Inverter

Note: Ideally there is no static power dissipation. When "I" is fully is high or fully low, no current path between V_{DD} and GND exists (the output is usually tied to the gate of another MOS transistor which has a very high input impedance).

Power is dissipated as "I" transitions from 0→1 and 1→0 and a momentary current path exists between Vdd and GND. Power is also dissipated in the charging and discharging of gate capacitances.
Parallel Connection of Switches

\[ Y = 0, \text{ if } A \text{ or } B = 1 \]
\[ Y = 1, \text{ if } A \text{ or } B = 0 \]

Series Connection of Switches

\[ Y = 0, \text{ if } A \text{ and } B = 1 \]
\[ Y = 1, \text{ if } A \text{ and } B = 0 \]
**NAND Gate Design**

$p$-type transistor tree will provide "1" values of logic function

$n$-type transistor tree will provide "0" values of logic function

Truth Table (NAND):

<table>
<thead>
<tr>
<th>AB</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>1</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>11</td>
<td>0</td>
</tr>
</tbody>
</table>

K-map (NAND):

NAND circuit example:

\[ P_{\text{tree}} = \overline{A} + \overline{B} \]
\[ N_{\text{tree}} = A \cdot B \]
NOR Gate Design

*p*-type transistor tree will provide "1" values of logic function

*n*-type transistor tree will provide "0" values of logic function

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</tbody>
</table>

K-map:

NOR circuit example:

\[ P_{\text{tree}} = A \cdot B \]
\[ N_{\text{tree}} = A + B \]
What logic gate is this?

Answer: AND function, but poor design!

Why? $n$MOS switches cannot pass a logic "1" without a threshold voltage ($V_T$) drop.

where $V_T = 0.7V$ to $1.0V$ (i.e.,
threshold voltage will vary)
output voltage = $4.3V$ to $4.0V$,
a weak "1"
The $n$MOS transistor will stop conducting if $V_{GS} < V_T$. Let $V_T = 0.7V$.

\[
\begin{array}{c}
G \rightarrow 5V \\
S \rightarrow D \\
0V \rightarrow 5V \\
\end{array}
\quad \begin{array}{c}
D \rightarrow ? \\
0V \rightarrow ?
\end{array}
\]

As source goes from $0V \rightarrow 5V$, $V_{GS}$ goes from $5V \rightarrow 0V$.

When $V_S > 4.3V$, then $V_{GS} < V_T$, so switch stops conducting.

$V_D$ left at $5V - V_T = 5V - 0.7V = 4.3V$ or $V_{DD} - V_T$.

What about $n$MOS in series?

\[
\begin{array}{c}
0V \rightarrow 5V \\
0V \rightarrow 4.3V \\
0V \rightarrow 4.3V \\
0V \rightarrow 4.3V \\
0V \rightarrow (V_{DD} - V_T)
\end{array}
\]

Only one threshold voltage drop across series of $n$MOS transistors.
For pMOS transistor, \( V_T \) is negative.

pMOS transistor will conduct if \( |V_{GS}| > |V_{T_P}| \) \((V_{SG} > |V_{T_P}|)\),

or \( V_{GS} < V_{T_P} \)

\[
\begin{align*}
V_{T_P} &= -0.7V \\
V_{GS} &= 0V - 5V = -5V
\end{align*}
\]

How will pMOS pass a "0"?

When \( |V_{GS}| < |V_{T_P}| \), stop conducting

So when \( |V_{GS}| < |-0.7V| \), \( V_D \) will go from 5V → 0.7V, a weak "0"

How are both a strong "1" and a strong "0" passed?

Transmission gate pass transistor configuration

When \( I = 1 \),

\[ B = \text{strong 1, if } A = 1; \]
\[ B = \text{strong 0, if } A = 0 \]

When \( I = 0 \), non-conducting
About that AND Gate...

No!!!
Poorly designed AND
(circuit designer fired)

Instead use this,
More Complex Gates

\[ F = AB + CD \quad \Rightarrow \quad N_{tree} \text{ will provide 0's, } P_{tree} \text{ will provide 1's} \]

0's of function \( F \) is \( \overline{F} \), \( \Rightarrow \overline{F} = \overline{AB + CD} = AB + CD \)

\( n \text{MOS transistors need high true inputs, so it is desirable for all input variables to be high true, just as above.} \)

Likewise, a \( P_{tree} \) will provide 1's.

\( F = AB + CD, \quad \text{need a form involving } \overline{A}, \overline{B}, \overline{C}, \overline{D} \)

Apply DeMorgan's Theorem:

\[ F = \overline{AB \cdot CD} = (\overline{A + B}) \cdot (\overline{C + D}) \]

Implementation \( \Rightarrow \)
Can also use K-maps:

\[ F = AB + CD \]

For \( N_{\text{tree}} \), minimize 0's; for \( P_{\text{tree}} \), minimize 1's

\[ N_{\text{tree}} = AB + CD \]

\[ P_{\text{tree}} = \overline{A} \cdot \overline{C} + \overline{A} \cdot \overline{D} + \overline{B} \cdot \overline{C} + \overline{B} \cdot \overline{D} \]

\[ = \overline{A} (\overline{C} + \overline{D}) + \overline{B} (\overline{C} + \overline{D}) \]

\[ = (A + B) \cdot (C + D) \]
Introduction to Static Load Inverters

1) 

When I = 1, inverter dissipates static power.

Switching point of inverter depends on ratio of R to R_{ON} (on resistance of nMOS device).

V_{OH} = 5V,  
V_{OL} close to 0V, depends on ratio R/R_{ON}

Note: output can swing from almost 0V to 5V (V_{DD})

2) 

Again, static power dissipation occurs when I = 1.

Load is enhancement-mode nMOS device.

Note: output swings from nearly 0V to (V_{DD} - V_{Tn})

Using a transistor as a load tends to require much less silicon area than a resistor.

V_{OH} = V_{DD} - V_{Tn},  
V_{OL} can be close to 0V, depending on ratio of R_{ON} of two enhancement devices
Depletion-mode $n$MOS

$n$MOS device with $V_{Tn} < 0$V (negative threshold voltage). Device is always conducting if $V_{GS} > 0$V.

3)  

![Depletion-mode nMOS Diagram](image)

$V_{GS} = 0$V always

Load device is always on, looks like a load resistor.

Dissipates static power when $I = 1$

$V_{OH} = 5$V; $V_{OL}$ nearly 0V, depending on ratio of $R_{ON,dep}$ to $R_{ON,enh}$.

Depletion-mode devices were used before it was economical to put both $p$-type and $n$-type devices on the same die.

4) $p$MOS device as static load

![pMOS Diagram](image)

Here also the load device is always on (conducting).

Dissipates static power when $I = 1$.

$V_{OH} = 5$V; $V_{OL}$ nearly 0V, depending on ratio of $R_{ON,p}$ to $R_{ON,n}$.
Basic MOS Device Equations

![Diagram of MOS device with labels](image)

The $n$MOS device is a *four* terminal device: Gate, Drain, Source, Bulk.

Bulk (substrate) terminal is normally ignored at schematic level, usually tied to ground for the $n$MOS case. In analog applications, however, the bulk terminal may not be ignored.

Gate controls channel formation for conduction between Drain and Source. Drain at higher potential than Source — Source usually tied to GND to act as pull-down ($n$MOS).

Three regions of operations — first-order (*ideal*) equations:

**Cutoff region**

$$I_D = 0 \text{A} \quad \text{if} \quad V_{GS} \leq V_{Tn} \quad (n$MOS threshold voltage)$$

**Linear region**

$$I_D = \beta \left( (V_{GS} - V_{Tn})V_{DS} - \frac{V_{DS}^2}{2} \right) \quad 0 < V_{DS} < V_{GS} - V_{Tn}$$

Note: $I_D$ is linear with respect to $(V_{GS} - V_{Tn})$ only when $\left(V_{DS}^2/2\right)$ is small.

**Saturation region**

$$I_D = \frac{\beta}{2} \left(V_{GS} - V_{Tn}\right)^2 \quad 0 < V_{GS} - V_{Tn} < V_{DS}$$


Device parameters:

\[ \beta = \frac{\mu \varepsilon}{t_{ox}} \left( \frac{W}{L} \right) \]

- \( \beta \): transistor gain factor, dependent on process parameters and device geometry \( (K_n) \)
- \( \mu \): surface mobility of the carriers in the channel
- \( \varepsilon \): permittivity of the gate insulator
- \( t_{ox} \): thickness of the gate insulator

As \( W/L \) increases, effective \( R_{ON} \) of device decreases

SPICE represents \( \beta \) by a factor given by

\[ K' = \mu C_{ox} = \mu \frac{\varepsilon}{t_{ox}} = KP \]

So,

\[ I_D = \frac{K' W}{2 L} (V_{GS} - V_{th})^2 \]

saturation region
VI characteristic

![Diagram of a VI characteristic showing the boundary between linear and saturation regions, with the linear region indicated by a dashed line.](image)

**Things to note:**

In the "linear" region, $I_D$ becomes less and less linear with $V_{GS}$ as $V_{DS}$ becomes large. This is because the $\left(\frac{V_{DS}^2}{2}\right)$ term in the linear region grows large.

Higher $V_{GS}$ values increase channel conductance allowing for higher values of $I_D$ for a given $V_{DS}$. 
MOSFET Characteristics
Vds 1 0 DC 10
Vgs 2 0 DC -.723
Vdummy 3 0 DC 0
M1 1 2 3 3 Mfet
.MODEL Mfet NMOS(KP=3686U VTO=2.30 LAMBDA=0.137)
.DC Vds 0 10 .2 Vgs 2.5 5 .5
.probe
.end
What do $W$ and $L$ physically look like?

*nMOSFET layout:*

In digital logic, typically will draw all transistors with the minimum gate length and vary the width.

Larger $W \Rightarrow$ larger transconductance (more current flow for given gate voltage), higher gate capacitance

During fabrication process, the actual width and length of the channel can be reduced by diffusion from the bulk, source, and drain into the device channel.

SPICE has some MOSFET model parameters to account for this effect, LD and WD, where the actual the actual length and width is calculated as

$$L_{\text{effective}} = L_{\text{drawn}} - 2 \times LD$$

$$W_{\text{effective}} = W_{\text{drawn}} - 2 \times WD$$

If LD, WD parameters not specified in the model, then SPICE assumes they are 0.
**Ideal Inverter**

![Ideal Inverter Diagram]

**Actual Inverter Characteristics, some definitions**

- $V_{IL}$ represents the maximum logic 0 (LOW) input voltage that will guarantee a logic 1 (HIGH) at the output
- $V_{IH}$ represents the minimum logic 1 (HIGH) input voltage that will guarantee a logic 0 (LOW) at the output
Noise Margin

Illustration of Noise Margin:

Calculate noise margin using

\[ \text{NM}_L = V_{IL} - V_{OL} \quad \quad \quad \quad \quad \text{NM}_H = V_{OH} - V_{IH} \]

How do we determine \( V_{IL}, V_{OL}, V_{OH}, \) and \( V_{IH} \)?

We must exam the inverter's transfer characteristic.
CMOS Inverter Regions of Operation

Region A:

\[ 0 \leq V_{in} < V_{Tn} \quad \Rightarrow \quad p\text{MOS nonsaturated}; \, n\text{MOS cutoff} \]

- \( n\text{MOS} \) is cutoff because \( V_{in} < V_{Tn} \)

Why is the \( p\text{MOS} \) device in the linear region?

Linear region \( \equiv \quad V_{SDp} < V_{SGp} - |V_{Tp}| \)

\[ (5 - 5)V < (5 - 0)V - |-0.7|V \]

\[ 0V < 4.3V \]

Note that the \( p\text{MOS} \) device can be in linear region even if \( I_{DP} \approx 0\text{A}! \)
Region B:

\[ V_{Tn} \leq V_{in} < V_{th} \quad \Rightarrow \quad pMOS \text{ nonsaturated, } nMOS \text{ saturated} \]

Why is \( nMOS \) saturated? Is \( V_{DSn} > V_{GSn} - V_{Th} \)?

Because \((V_{DSn} = V_{out}) > V_{th}\) and \((V_{GSn} = V_{in}) < V_{th}\),

then \[ V_{DSn} > V_{GSn} - V_{Th} \]
\[ V_{out} > V_{in} - V_{Th} \quad \text{[B-1]} \]

Why is \( pMOS \) in linear region?

It started out in linear and will remain in linear as long as

\[ V_{SDp} < V_{SGp} - |V_{Tp}| \]
\[ (V_{DD} - V_{out}) < (V_{DD} - V_{in}) - |V_{Tp}| \]
\[ V_{in} < V_{out} - |V_{Tp}| \quad \text{[B-2]} \]

\( V_{out} \) in the above expression (Eqn. [B-2]) is decreasing towards \( V_{th} \) and \( V_{in} \) is increasing towards \( V_{th} \). When Eqn. [B-2] no longer holds, then the \( pMOS \) device will become saturated.

For the \( pMOS \) device, then

regions A \( \Rightarrow \) B \( \Rightarrow \) C correspond to

linear \( \Rightarrow \) linear \( \Rightarrow \) saturated, respectively.
How can you predict the output voltage for region B?

The nMOS is saturated, so

\[ I_{Dn} = \frac{\beta_n}{2} (V_{in} - V_{Tn})^2 = \frac{\beta_n}{2} (V_{GSn} - V_{Tn})^2 \]

The pMOS is linear, so

\[ I_{Dp} = \frac{\beta_p}{2} \left( 2(V_{SGp} - |V_{Tp}|)V_{SDp} - (V_{SDp})^2 \right) \]

\[ I_{Dp} = \frac{\beta_p}{2} \left( 2(V_{DD} - V_{in} - |V_{Tp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right) \]

Can solve for \( V_{out} \) since

\[ I_{Dn} = I_{Dp} \]

Equivalent circuit for region B ⇒

\[ V_{out} \]
Region C:

\[ V_{in} = V_{th} \quad \Rightarrow \quad \text{pMOS saturated, nMOS saturated} \]

In order for \( n \)MOS to be saturated, need

\[ V_{DSn} > V_{GSn} - V_{Tn} \]
\[ V_{out} > V_{in} - V_{Tn} \]

In order for \( p \)MOS to be saturated, need

\[ V_{SDp} > V_{SGp} - |V_{Tp}| \]
\[ V_{DD} - V_{out} > V_{DD} - V_{in} - |V_{Tp}| \]
\[ V_{out} < V_{in} + |V_{Tp}| \]

So \( V_{out} \) in region C,

\[ V_{in} - V_{Tn} < V_{out} < V_{in} + |V_{Tp}| \]

The CMOS inverter has very high gain in region C so small changes in \( V_{in} \) produce large changes in \( V_{out} \). No closed form equation for \( V_{out} \). Somewhere in this region, \( V_{out} = V_{in} \), which is the switching point for this gate.

Equivalent circuit for region C:
What is $V_{in}$ in region C?

In region C, both devices in saturation so

$$I_{Dp} = \frac{\beta_p}{2} (V_{DD} - V_{in} - |V_{T_P}|)^2$$

$$I_{Dn} = \frac{\beta_n}{2} (V_{in} - V_{T_n})^2$$

So, using $I_{Dn} = I_{Dp}$, $V_{in}$ can be solved for (more on this later....)

Region D:

$$V_{th} < V_{in} \leq V_{DD} - |V_{T_P}| \quad \Rightarrow \quad pMOS \text{ saturated, } nMOS \text{ linear}$$

Hence,

$$I_{Dp} = \frac{\beta_p}{2} (V_{DD} - V_{in} - |V_{T_P}|)^2$$

$$I_{Dn} = \frac{\beta_n}{2} \left(2(V_{in} - V_{T_n})V_{out} - V_{out}^2\right)$$

Again, since $I_{Dp} = I_{Dn}$, we can solve for $V_{out}$:

$$V_{out}^2 - 2(V_{in} - V_{T_n})V_{out} + \frac{\beta_p}{\beta_n} (V_{DD} - V_{in} - |V_{T_P}|)^2 = 0$$

using

$$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

and, recognizing from above,

$$a = 1, \quad b = -2(V_{in} - V_{T_n}), \quad c = \frac{\beta_p}{\beta_n} (V_{DD} - V_{in} - |V_{T_P}|)^2$$

we get
\[ V_{\text{out}} = (V_{\text{in}} - V_{Tn}) - \sqrt{(V_{\text{in}} - V_{Tn})^2 - \frac{\beta_p}{\beta_n} (V_{\text{in}} - V_{DD} - |V_{Tp}|)^2}. \]

Equivalent circuit for region D ⇒

Region E:

\[ V_{\text{in}} > V_{DD} - |V_{Tp}| \quad \Rightarrow \quad p\text{MOS is cutoff, } n\text{MOS is linear mode} \]

Since \( V_{SGp} = V_{DD} - V_{\text{in}} (< |V_{Tp}|) \),

\[ \therefore V_{\text{out}} \equiv 0V \]

due to \( n\text{MOS acting as pull-down while } p\text{MOS in cutoff} \).
CMOS Inverter Transfer Characteristic

Analysis:

**V\text{OH}:** \( V_{\text{in}} < V_{Tn} \), the \( n \)MOS transistor is in cutoff while the \( p \)MOS transistor is turned-on (inversion layer established). The result is

\[ V_{\text{OH}} \equiv V_{\text{DD}}. \]

**V\text{OL}:** \( (V_{\text{DD}} - V_{\text{in}}) < |V_{Tp}| \), the \( p \)MOS is in cutoff while the \( n \)MOS is on and providing a conduction channel to ground. Hence,

\[ V_{\text{OL}} \equiv 0V. \]

**V\text{IL}:** Input low voltage, here the \( n \)MOS transistor is saturated and the \( p \)MOS is nonsaturated. Equating the currents provides

\[
\frac{\beta_n}{2}(V_{\text{IL}} - V_{Tn})^2 = \frac{\beta_p}{2}(2(V_{\text{DD}} - V_{\text{IL}} - |V_{Tp}|)(V_{\text{DD}} - V_{\text{out}}) - (V_{\text{DD}} - V_{\text{out}})^2).
\]
V_{IL}: (continued) Since two unknowns exist, \( V_{in} = V_{IL} \) and \( V_{out} \), a second equation is needed. Use the unity-gain condition to obtain this second equation,

\[
\frac{dV_{out}}{dV_{in}} = \frac{(\partial I_{Dn}/\partial V_{in}) - (\partial I_{Dp}/\partial V_{in})}{(\partial I_{Dp}/\partial V_{out})} = -1,
\]

provides

\[
V_{IL} \left( 1 + \frac{\beta_n}{\beta_p} \right) = 2V_{out} + \left( \frac{\beta_n}{\beta_p} \right) V_{Tn} - V_{DD} - |V_{Tp}|.
\]

Now the two equations needed to solve for \( V_{IL} \) and \( V_{out} \) exist.

V_{IH}: Input high voltage, here the \( n \)MOS is nonsaturated and the \( p \)MOS is saturated. Equating the drain currents yields

\[
\frac{\beta_n}{2} \left( 2(V_{IH} - V_{Tn})V_{out} - V_{out}^2 \right) = \frac{\beta_p}{2} (V_{DD} - V_{IH} - |V_{Tp}|)^2,
\]

the first of two equations needed to solve two unknowns, \( V_{in} = V_{IH} \) and \( V_{out} \). Use the unity-gain condition to get the second,

\[
\frac{dV_{out}}{dV_{in}} = \frac{(\partial I_{Dp}/\partial V_{in}) - (\partial I_{Dn}/\partial V_{in})}{(\partial I_{Dn}/\partial V_{out})} = -1.
\]

This provides

\[
V_{IH} \left( 1 + \frac{\beta_p}{\beta_n} \right) = 2V_{out} + V_{Tn} + \frac{\beta_p}{\beta_n} (V_{DD} - |V_{Tp}|),
\]

the second equation needed to solve for the two unknowns.
**V\textsubscript{th}:** At the CMOS inverter's switching point, or *inverter threshold*, \( V\textsubscript{th} = V\textsubscript{in} = V\textsubscript{out} \) and both the \( p\)MOS and \( n\)MOS transistors are saturated. Again, equating the drain currents,

\[
\frac{\beta_n}{2}(V\textsubscript{th} - V\textsubscript{Tn})^2 = \frac{\beta_p}{2}(V\textsubscript{DD} - V\textsubscript{th} - |V\textsubscript{Tp}|)^2
\]

is obtained which can be easily solved to provide \( V\textsubscript{th} \),

\[
V\textsubscript{th} = \frac{V\textsubscript{Tn} + \sqrt{\frac{\beta_p}{\beta_n} (V\textsubscript{DD} - |V\textsubscript{Tp}|)}}{1 + \sqrt{\frac{\beta_p}{\beta_n}}}
\]

**Note:** switching point of gate (\( V\textsubscript{th} \)) is \( \frac{V\textsubscript{DD}}{2} \) *if* \( \frac{\beta_n}{\beta_p} = 1 \) and \( V\textsubscript{Tn} = -V\textsubscript{Tp} \).

So, switching point of inverter is function of the ratio of the \( n\)MOS/\( p\)MOS gains and the threshold voltages of the \( n\)MOS, \( p\)MOS transistors.
$\beta_n/\beta_p$ Ratio

The $\beta_n$ (gain of nMOS) / $\beta_p$ (gain of pMOS) ratio determines the switching point of the CMOS inverter.

\[ \frac{\beta_n}{\beta_p} = 10 \]
\[ \frac{\beta_n}{\beta_p} = 1 \]
\[ \frac{\beta_n}{\beta_p} = 0.1 \]

Strong pull-down

Equal pull-up/pull-down "strength"

Switching point = $V_{DD}/2$
if $\beta_n/\beta_p = 1$ and $V_{Tn} = |V_{Tp}|$
Recall that
\[ \beta = \frac{\mu e W}{t_{\text{ox}} L} . \]

If we assume that the nMOS and pMOS transistors have equal W/L ratios, then
\[ \frac{\beta_n}{\beta_p} = \frac{\mu_n e W_n}{\mu_p e W_p} = \frac{\mu_n}{\mu_p} = \frac{\text{electron mobility}}{\text{hole mobility}} . \]

In silicon, the ratio \( \mu_n/\mu_p \) is usually between 2 to 3.

This means, that if \( L_n = L_p \),
then \( W_p \) must be 2 to 3 times \( W_n \)
in order for \( \beta_n = \beta_p \).
Calculate the switching point of a static load inverter as function of $\beta_n/\beta_p$:

In region C, already know $n$MOS device is saturated from previous analysis.

For $p$MOS to be saturated need:

\[
V_{SDp} > V_{SGp} - |V_{Tp}|
\]
\[
V_{DD} - V_{out} > V_{DD} - 0V - |V_{Tp}|
\]
\[
V_{out} < |V_{Tp}|
\]
Not true!!!

(If $V_{out}$ in region C is about $\frac{V_{DD}}{2}$ and $\frac{V_{DD}}{2} > |V_{Tp}|$
(typically this is true))

$\therefore$ $p$MOS must be in linear region
Then
\[ I_{Dn} = \frac{\beta_n}{2} (V_{GSn} - V_{Th})^2 = \frac{\beta_n}{2} (V_{in} - V_{Th})^2 \]
and
\[ I_{Dp} = \frac{\beta_p}{2} \left( 2(V_{SGp} - |V_{Tp}|)V_{SDp} - V_{SDp}^2 \right) \]
\[ I_{Dp} = \frac{\beta_p}{2} \left( 2(V_{DD} - |V_{Tp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right) \]
Equate \( I_{Dn} = I_{Dp} \) and solve for \( V_{out} \).
\[ V_{out} = |V_{Tp}| + \sqrt{(V_{DD} - |V_{Tp}|)^2 - \frac{\beta_n}{\beta_p} (V_{in} - V_{Th})^2} \]
Can also solve for \( \beta_n/\beta_p \),
\[ \frac{\beta_n}{\beta_p} = \frac{(V_{DD} - |V_{Tp}|)^2 - (V_{out} - |V_{Tp}|)^2}{(V_{in} - V_{Th})^2} \]
Consider again

\[
\frac{\beta_n}{\beta_p} = \frac{(V_{DD} - |V_{TP}|)^2 - (V_{out} - |V_{TP}|)^2}{(V_{in} - V_{Tn})^2}
\]

for the pseudo-\textit{n}MOS inverter.

Let \(|V_{TP}| = V_{Tn} = 0.2V_{DD}\) and \(V_{in} = V_{out} = \frac{V_{DD}}{2}\). Then, for \(V_{DD} = 5V\),

\[
\frac{\beta_n}{\beta_p} \cong 6.1 !!!
\]

Note that this is \textit{very} different result from the CMOS inverter case!

If \(V_{DD} = 3.3V\), but the value of \(V_{Tn} = |V_{TP}|\) is unchanged (i.e., 1V in the above example), then

\[
\frac{\beta_n}{\beta_p} \cong 11.5
\]

for a switching point equal to \(\frac{V_{DD}}{2}\).

The \(\beta_n/\beta_p\) ratio depends on the absolute value of \(V_{DD}\)! This means that the operation of the pseudo-\textit{n}MOS inverter will NOT scale with \(V_{DD}\) (for a given CMOS technology).

For the CMOS inverter, the \(\beta_n/\beta_p\) ratio for a switching point of \(V_{DD}/2\) is \textit{independent} of \(V_{DD}\) so its operation \textit{will} scale with supply voltage. This is another big advantage of CMOS technology.

Not unusual for static CMOS circuits to operate over a \textit{very large} range of power supply voltages, i.e., 2.0V to 6.0V is common.