Homework 1

1. Estimate all the junction areas and perimeters at the labeled nodes of the circuit in Figure 1. Assume that all the $p$-channel transistors have sizes of 10 $\mu$m/0.5 $\mu$m and all the $n$-channels have sizes of 4 $\mu$m/0.5 $\mu$m.

![Figure 1](image1)

2. Sketch the layout for the circuit in Figure 1 using $\lambda$ design rules.

3. Draw the schematic of the circuit that the layout in Figure 2 represents.

![Figure 2](image2)

Due 02.05.18
Homework 2

3.1, 3.2, 3.6, 3.11, 3.15

Due 02.19.18