ECE433 Introduction to VLSI  
Spring 2018  
S.K. Islam, 504 Min Kao Building, 974-8531, sislam@utk.edu
Office Hours: MWF 11:00 am-12:00 noon

Teaching Assistants: Peixing Liu (pliu7@vols.utk.edu)


References:
• Class handouts

Grading:

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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</thead>
<tbody>
<tr>
<td>Midterm Exams</td>
<td>40%</td>
</tr>
<tr>
<td>Final</td>
<td>25%</td>
</tr>
<tr>
<td>Laboratory Assignments</td>
<td>10%</td>
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<tr>
<td>Homework</td>
<td>5%</td>
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<tr>
<td>Final Project</td>
<td>20%</td>
</tr>
<tr>
<td>Total</td>
<td>100%</td>
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</tbody>
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Grading Scale:
A(>90%), A- (88 to 89%), B+(85 to 87%), B(80 to 84%), B- (78 to 79%), C+(75 to 77%), C(70 to 74%), C- (68 to 69%), D+ (65 to 67%), D(60 to 64%), D- (58-59%), F(<59%)

Lecture Classes will meet in MK 525 from 10:10-11:00 am on Mondays, Wednesdays and Fridays. Class attendance is encouraged and strongly recommended.

VLSI Laboratory
Lab/Project policy — If you fail to hand in TWO or more labs you will be assigned an 'F' in the course regardless of test average. If you fail to hand in the Project you will also be assigned an 'F' in the course regardless of test average.

All labs will meet in MK 228.

There will be four laboratory periods of approximately two hours long per week administered by the TAs. All labs will involve probably approximately 1/2 hour of lecture before starting, so BE ON TIME! Unless otherwise noted, labs will be due at the beginning of your assigned lab period one week after the lab was handed out. Outside of these lab periods, MK 228 will be open from 10 am to 5 pm every weekday. However, TAs support will be available only during the assigned lab hours or by appointment with the TAs.

The labs are designed to give advanced undergraduates and beginning graduate students a working knowledge of CMOS digital integrated circuit technology, circuit design methodologies, including simulation and physical layout of CMOS digital circuit structures. Cadence and HSpice will be used widely for circuit simulation.
Details of the Lab will be posted on the course website.

Lab 1: Introduction
Lab 2: Simulation of Inverter using Spectre
Lab 3: Schematic Entry of Inverter & Simulation
Lab 4: Schematic Entry of Complex Gate (NAND, NOR or XOR)
Lab 5: Cadence Layout of Inverter
Lab 6: Layout Simulation & generating LVS (Layout vs Schematic)
Lab 7: Cadence Layout of Complex Gate (NAND, NOR or XOR)
Lab 8: Transistor Sizing & Rise Time, Fall Time calculation
Lab 9: Design of a Full Adder
Lab 10: Design of a Full Adder (contd.)

Final Project:

Design of a Flip-Flop (T Flip-flop, D Flip-flop, JK flip flop or JK Master Slave flip flop)

Course Topics:

Introduction to CMOS Circuits
MOS Transistor Theory
CMOS Process Video
CMOS Processes
CMOS Layout
Modeling of MOS transistors
Combinational MOS logic circuits
Transmission Gates and Fully-Differential Logic
Delay Characterization
Lathes, Flip-Flops and Synchronous System Design
I/O circuits
Bipolar and BiCMOS Logic Gates
Standard Cell Methodology
Capacitance Characterization
Transient Analysis
Clocked Systems
Dynamic Logic
Integrated Memories

Academic Dishonesty: Will NOT be tolerated and NO WARNINGS will be given. It is the responsibility of the student to review UT policy and procedures in this area since they will be strictly adhered to. Cheating will result in an F in the course, and possible university sanctions.