3D Tri-Gate Transistors

I. Introduction

In 2011 Intel Corporation announced production of new transistor technology called "3D Tri-Gate" that incorporated a three dimensional structure. The advancement resulted in faster on-off speeds and lower power without an increase in transistor size. This paper documents the Tri-Gate concept and considers results, disadvantages and future applications.

II. Background

Figure 1 shows typical MOSFET transistor layout. A P-type silicon substrate has Source and Drain wells implanted and a polysilicon gate etched on top. The result is a planar structure. Driven by the need for higher on-off speeds and reduced power consumption, planar transistor size had been reduced to nanometer sized width and lengths, while the silicon dioxide insulating layer between gate and channel had been reduced to five atomic layers. Resultant problems included growing leakage currents from gate to channel and increasingly unreliable transistor characteristics.

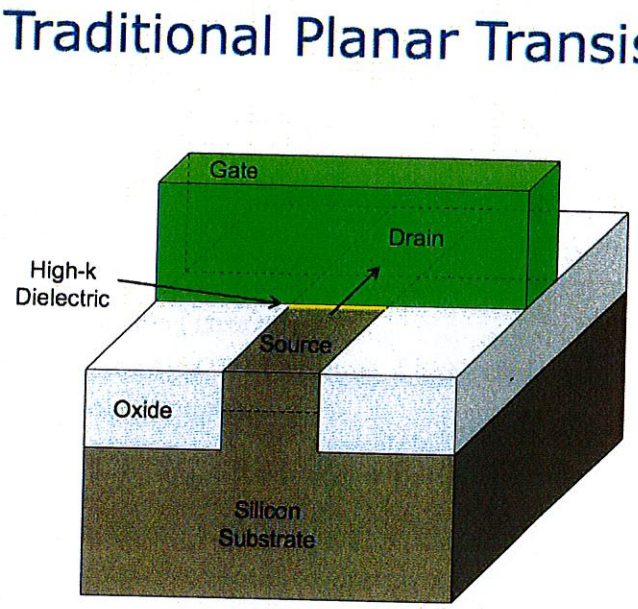

Fig. 1 Image Courtesy Intel Corporation

One adverse effect of shrinking transistor size is called "short-channel effect". [1] [2] When the channel length approaches depletion layers widths of the source and drain, several problems arise:

1. The decreased channel width allows the depletion layers from both source and drain to overlap. Punchthrough occurs when current flows from source to drain in spite of voltage potential at the gate.
2. Reduction of channel length allows the longitudinal nature of the E-field (E_y) in the depletion region to interfere with gate potentials. This affects electron scattering in the surface region and causes a drop in electron mobility in the channel. See Figure 2.

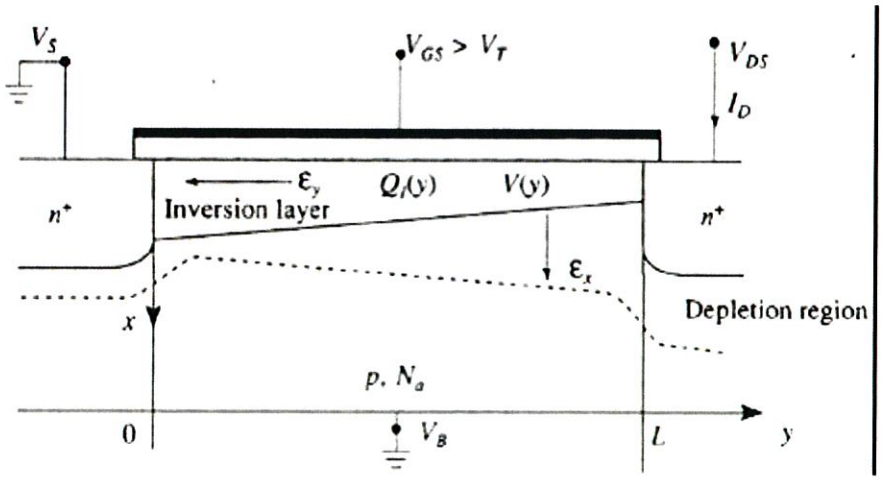

Fig. 2 Depletion regions interfering with electron transport in the Inversion layer

3. The high E-fields in the depletion layers can accelerate electrons and cause the generation of electron-hole pairs. Substantial currents result, in essence turning the transistor on. Also, accelerated electrons can escape the local transistor and develop as leakage currents in adjoining structures.
4. Determination of VT0 for a MOSFET assumes a large channel length relative to depletion layer width. The standard equation

$$V_T = V_{T0} + \gamma * (\sqrt{V_{SB} + |-2\varphi_{F|}} - \sqrt{|-2\varphi_{F|}})$$

assumes a rectangular shape. However, a short channel changes the inversion layer geometry, leaving the equation for V_T overestimating channel charge.
5. Velocity saturation occurs due to localized high E-fields. Transistor transconductance is reduced, restricting current flow and transistor gain.

Summarizing, relatively short channels made gate control "fuzzy". Another approach was necessary to reverse this effect.

III. Concept

Three dimensional transistors were introduced more than a decade ago. Figure 3 displays the general structure outline. Instead of the planar structure, the gate wraps around source and drain "fins" that protrude upward. The result is increased surface area between gate and the inversion layer, allowing narrow lengths but significantly improved gate control.

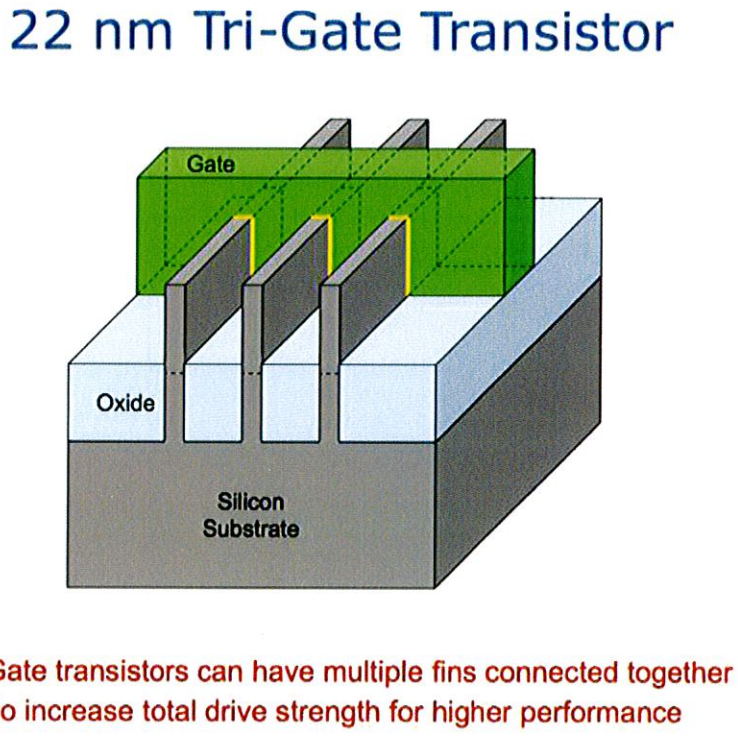

Fig. 3 Image Courtesy Intel Corporation

The technology has been otherwise dubbed "FinFet", with other semiconductor manufacturers involved in similar designs. The difference between Intel's Tri-Gate and FinFets relates to manufacturing issues rather than substantive design.

Figures 4 and 5 show the fin construct for NMOS source and drain channel. Figure 5 shows the electron microscope cutaway of the fin structure taken from actual integrated circuits.

1. Because of the gate wrap-around, the overall inversion layer is larger (the blue area in Figure 4), so more current can flow from source to drain. Multiple fins enhance this advantage.
2. Better control of current flow is attained through this design, reducing gate leakage when off and allowing greater gate control when on.

3. Overall size of the transistor is not changed, allowing similar densities as the planar construct.

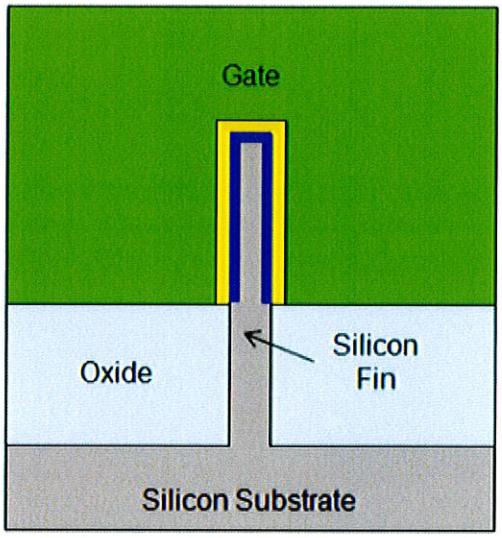

Fig. 4 Intel Corporation Fin Construct

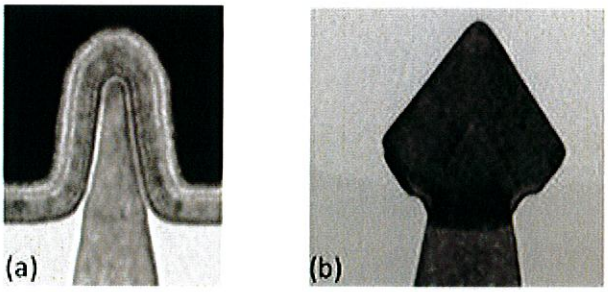

Fig. 5 Electron Microscope Image of Actual Mosfet Fins

IV. Some Device Advantages Vs. Planar Transistors

1. Drain Induced Barrier Lowering (DIBL)

In large MOSFET structures, voltage applied at the drain increases the depletion region under the drain and into the gate region. As a result, the drain takes a greater role in attracting electrons across the inversion layer, lessening the role of the gate. The gate

then has greater ability to attract electrons, effectively reducing the threshold voltage V_T and making it easier for electrons to cross the source to drain channel. The electron barrier is reduced, hence the name "Barrier Lowering".

As channel length shrinks, this barrier lowering begins to affect the "subthreshold region", i.e., the region that is created when $V_{GS} < V_T$ for cutoff (but not when $V_{GS} \ll V_T$). The subthreshold current change with respect to gate bias and drain voltage reduces to threshold change with drain voltage, and further channel shrinking causes the slope of the current vs. gate bias to also shrink. At very small lengths, the gate fails entirely to turn the channel off.

Figure 6 shows a plot of drain current vs. gate bias. In the subthreshold region, the slope of the Tri-Gate current is considerably better. The result is less leakage, faster switching and less power consumption with the same gate voltage. [3]

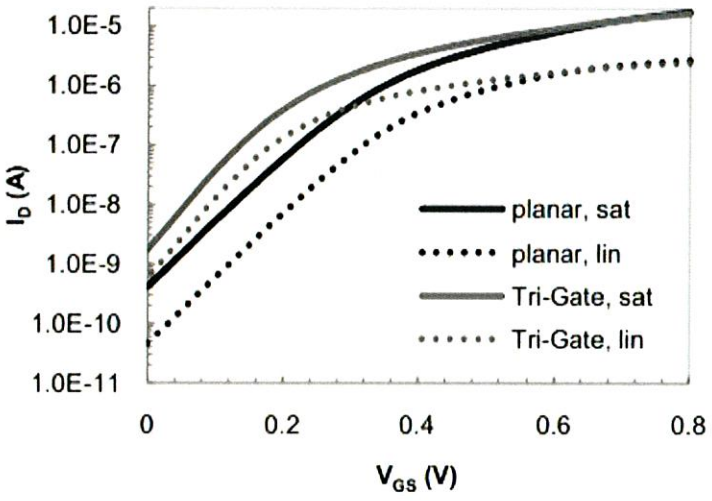

Fig. 6 Comparison of Tri-Gate to Planar Id vs. Vgs

2. Threshold Voltage

Figure 7 compares threshold voltages for Tri-Gate and planar transistors. As channel length is reduced, planar transistors show a significant degradation in threshold voltage while Tri-Gate remains flat.

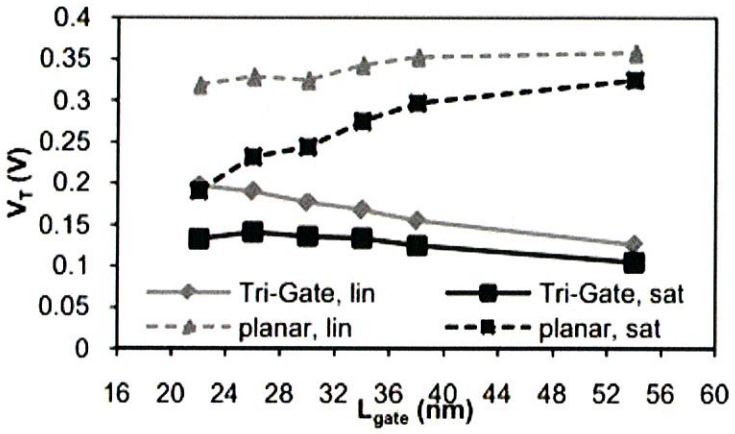

Fig. 7 Threshold voltages for planar and Tri-Gate transistors

V. Fin Optimization

Simulation [3] performed on fin height and width demonstrated optimum sizes for 25 nm compared to 26 nm planar transistors. Fins too wide and short degenerate to planar-like transistors. If they are too tall and too narrow, fin resistance becomes a factor. Fig 8 shows the optimal ratio of height to width for best On vs. Off current ratios. For NMOS transistors with smaller fin width, the ratio improves. However, increasing the fin height above about 7 nm shows a ratio decrease.

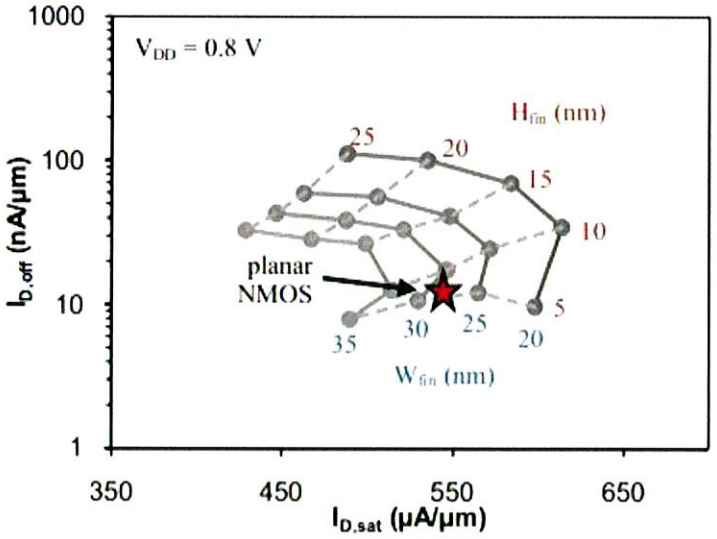

Fig. 8 Fin height and width for optimal On/Off ratios

Figure 9 displays optimization of fin height and width for subthreshold slope, clearly demonstrating tri-gate improvement over a planar transistor. The slope of 73mV/dec does not drift much with a fin ratio between 0.25 and 1.3. However, with a small and wide fin, subthreshold slope approaches the planar transistor values. The simulations demonstrate an optimum height of 5 to 10 nm and smallest possible width, in this case, 20 nm.

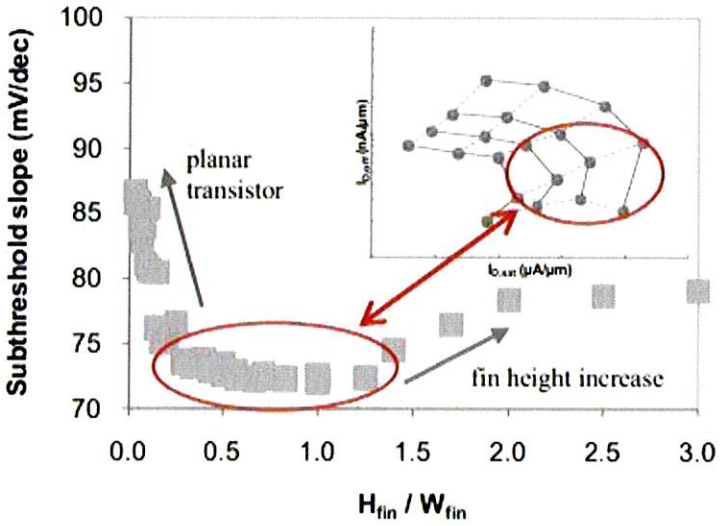

Fig. 9 Subthreshold slope optimization with fin height

VI. Making the Fin

To manufacture a fin or fins, a silicon substrate is marked and etched to fin depth. [4] See Figure 10. Next, an oxide layer fills the deep trenches and must be without defects or voids. The oxide layer is then polished back to set the fin height, and a recess etch removes the oxide from the sides of the fins.

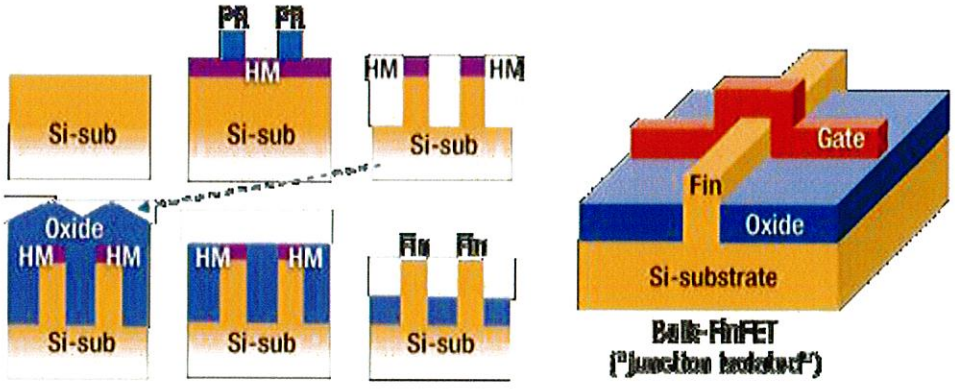

Fig. 10 Fin manufacturing process

The etch has no stop guide, so timing and careful process control is necessary. Finally, an angled dopant implant at the base of the fin creates doped junctions.

VII. Tri-Gate Performance

Intel claims a significant decrease in transistor delay, as shown in Figure 11.

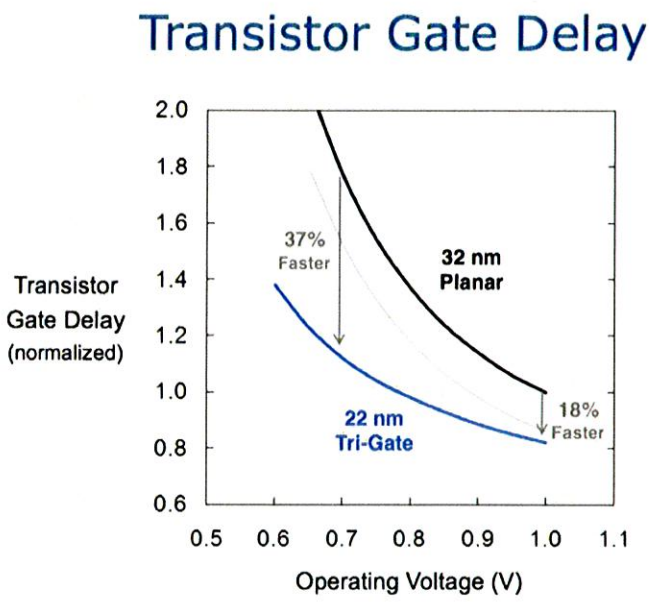

Fig. 11 Image Courtesy Intel Corporation

This results in either a faster transistor or less operating voltage for the same delay, compared to the 32 nm planar technology. Intel actually claims a 50% power reduction. High-end desktops as well as mobile, low-power devices should see Intel's new technology sometime this year.

VIII. Conclusion

Innovative ideas such as FinFets and 3D Tri-Gates continue to push the envelope of Moore's Law. Substantial improvements in power reduction, gate speed and miniaturization have been seen. Other possibilities, such as gate-surround, also offer potential improvements.

Bibliography

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