7.1 (a)
(7.5)

(a) The worst case input combinations are those that cause only one current path from output to ground. The combinations are listed in the following table:

<table>
<thead>
<tr>
<th>A = 1</th>
<th>C = 1</th>
<th>B = 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>A = 1</td>
<td>C = 1</td>
<td>D = 0</td>
</tr>
<tr>
<td>B = 1</td>
<td>D = 1</td>
<td>A = 0</td>
</tr>
<tr>
<td>B = 1</td>
<td>D = 1</td>
<td>C = 0</td>
</tr>
<tr>
<td>B = 1</td>
<td>E = 1</td>
<td>A = 0</td>
</tr>
<tr>
<td>B = 1</td>
<td>E = 1</td>
<td>C = 0</td>
</tr>
</tbody>
</table>

(b) The worst case equivalent circuit can be represented by a simple inverter. Both transistors are operating in linear region. \((V_{\text{out}} = V_{\text{in}} - V_{\text{DD}} = 1.2 \, \text{V})\)

\[
V_{\text{up}} = V_{T0} + \frac{8}{\sqrt{2}} \left( 2 \Phi_f + V_{SB} - \sqrt{2} \Phi_f \right) = 0.5468 \, \text{V}
\]

\[
V_{\text{down}} = 0.53 \, \text{V}
\]

\[
\left(\frac{W}{L}\right)_{\text{up}} = \frac{5}{5} \quad \left(\frac{W}{L}\right)_{\text{down}} = \frac{100}{5+5} = \frac{100}{10}
\]

\[
J_{\text{up}} = J_{\text{down}}
\]

\[
\Rightarrow \quad \frac{\mu_n C_w}{\frac{W}{L}} \left[ (V_{\text{GS,up}} - V_{\text{TN,up}}) V_{\text{DS,up}} - \frac{V_{\text{DS,up}}^2}{2} \right]
\]

\[
= \mu_n C_w \left(\frac{W}{L}\right)_{\text{down}} \left[ (V_{\text{GS,down}} - V_{\text{TN,down}}) V_{\text{DS,down}} - \frac{V_{\text{DS,down}}^2}{2} \right]
\]

\[
= \frac{5}{5} \left[ (2 - V_{\text{OL}} - 0.5468)(1.2 - V_{\text{OL}}) - \frac{(1.2 - V_{\text{OL}})^2}{2} \right] \Rightarrow V_{\text{OL}} \approx 0.13 \, \text{V}
\]

\[
= \frac{100}{10} \left[ (1.2 - 0.53) V_{\text{OL}} - \frac{V_{\text{OL}}^2}{2} \right]
\]
The equivalent inverter for the NOR gate

\[(\frac{W}{L})_{n\_eq} = 2 (\frac{W}{L})_n = 2\]
\[(\frac{W}{L})_{p\_eq} = \frac{1}{2} (\frac{W}{L})_p = 2\]

Therefore, \[K_{n\_eq} = K_n' (\frac{W}{L})_{n\_eq} = 196.4 \text{ mA}/V^2\]
\[K_{p\_eq} = K_p' (\frac{W}{L})_{p\_eq} = 92 \text{ mA}/V^2\]

\[V_{OL} = 0V \quad V_{OH} = V_{DD} = 1.2V\]

**Calculate \(V_{IL}\)**

\[V_{OUT} = \frac{1}{2} \left\{ \left(\frac{K_n}{K_p} + 1\right) V_{IL} - \frac{K_n}{K_p} V_{T_{0,n}} - V_{T_{0,p}} + V_{DD} \right\}\]

\[\Rightarrow V_{OUT} = 1.567 V_{IL} + 0.289\]

\[\frac{K_n}{2} \left(V_{IL} - V_{T_{0,n}}\right)^2 = K_p \left[ V_{IL} - V_{DD} - V_{T_{0,p}} - \frac{V_{OUT} - V_{DD}}{2} \right] (V_{OUT} - V_{DD})\]

\[V_{IL} = 0.207V\]

**Calculate \(V_{IH}\)**

\[V_{OUT} = \frac{1}{2} \left\{ \left(1 + \frac{K_p}{K_n}\right) V_{IH} - V_{T_{0,n}} - \frac{K_p}{K_n} (V_{DD} + V_{T_{0,p}}) \right\}\]

\[V_{OUT} = 0.734 V_{IH} - 0.427\]

\[K_n \left(V_{IH} - V_{T_{0,n}} - \frac{V_{OUT}}{2}\right) V_{OUT} = \frac{K_p}{2} \left(V_{IH} - V_{DD} - V_{T_{0,p}}\right)^2\]

\[V_{IH} = 0.61V\]

\[NM_L = 0.207 - 0 = 0.207V\]

\[NM_H = 1.2 - 0.61 = 0.59V\]
(a) \[ F = \frac{L}{(B+c)} + D \]

(b) The worst case inputs \((A=1, B=1, c=1, D=0)\) using eq (7.27), we can find the effective \(\frac{W}{L}\) of driver

\[
\left(\frac{W}{L}\right)_{\text{effective}} = \left[ \frac{1}{(WL)A} + \frac{1}{(WL)B+c} \right]^{-1} = \left[ \frac{1}{8A} + \frac{1}{4/4} \right]^{-1} = \frac{2}{3}
\]

And \(V_{OL}\) have to satisfy below condition (eq 7.4)

\[
V_{OH} - V_{TO,n} - \sqrt{(V_{OH} - V_{TO,n})^2 - \left(\frac{K_{load}}{K_{driver}}\right) F_c \cdot L_p \left(\frac{V_{DD} - 1V_{TO,pl}}{V_{DD} - V_{TO,pl} + F_c \cdot L_p}\right)^2} \\
\Rightarrow \left(\frac{W}{L}\right) = 0.2 \leq 80\text{mV}
\]

(c) Threshold voltage of depletion nMOS is changed due to the body effect. So drain current of load is reduced. Then \(V_{OL}\) will be increased. In order to make its drain current larger, \(\frac{W}{L}\) should be increased.
(7.11) \[ F = A\bar{B} + \bar{A}\bar{B} = A + B \]

(b) Using NOR gates

\[ A\bar{B} + \bar{A}\bar{B} = (A + B)(\bar{A} + \bar{B}) = \bar{A} + B + (\bar{A} + \bar{B}) \]
(c) Using AND gates

\[ f = \overline{A}B + \overline{A}\overline{B} \]

\[ f = \overline{f} = \overline{A}\overline{B} + \overline{A}B \]