A 100 MHz 4-bit Synchronous Counter

1. Introduction
This paper documents the design and implementation of a high speed, 4-bit synchronous counter. Reliable and industry-standard Master-Slave JK Flip-Flops were combined with 4-stage output buffers to drive a 5 pF load to at least 100 MHz. The counter operated with low output rise, fall, and delay times synchronously at the falling edge of the clock.

2. Design
Master-Slave JK Flip-Flops were chosen because their behavior was completely predictable under all conditions. Also, their states could be changed synchronously, that is, at the same clock edge. Thus, no cascading delays would be introduced. Fig. 1 shows the Flip-Flop schematic.

![Fig. 1. JK Flip-Flop schematic](image)

A truth table was constructed as shown in Fig. 2 to implement the 4-bit, 16 state automaton. Present State and Next State were represented as a 1-bit shift “up” in count. Set, Reset, or other control pins could easily be added to this design if deemed necessary in the future.
From the Truth table, K-maps generated the following minimal sum of products:

$$J_0 = K_0 = 1 \quad J_1 = K_1 = Q_4 \quad J_2 = K_2 = Q_1 \cdot Q_0 \quad J_3 = K_3 = Q_2 \cdot Q_1 \cdot Q_0$$

Notice that the J and K inputs were equal for each Flip-Flop, essentially converting them to "T" Flip-Flops. Also, because the last two sum of products required AND gates, they were converted to NOR products using De Morgan’s law,

$$J_2 = K_2 = \overline{Q_1 + Q_0} \quad J_3 = K_3 = \overline{Q_2 + \overline{Q_1} + Q_0}$$

allowing the use of NOR gates from the inverted outputs of the counter. Fig. 3 shows the final circuit diagram.
For high speed operation greater than 100 MHz, multi-stage buffers were added. The optimization equation for large capacitive loads,

\[ n_{opt} = \ln \left( \frac{C_L}{C_g} \right) = \ln \left( \frac{5000 \text{ pF}}{100 \text{ fF}} \right) = 3.91 \]

yielded \( n = 4 \), i.e., a four stage buffer constructed with CMOS inverters. The area for each inverter increased approximately 2.7 times in accordance with optimal load handling. See Fig. 4.

![Fig. 4. 4-stage output buffer](image)

3. **Layout**

Figures 5, 6 and 7 show transistor layouts for the JK Flip-Flops, 4-stage buffer, and 4-bit counter respectively. For the buffer in Fig. 6, parallel transistors replaced transistors with very large areas using the “multiply” feature in Cadence. Adding a buffer for each counter output resulted in an additional 32 transistors per stage. Fig. 7 shows the counter divided into 4 parts, with each part primarily containing one Flip-Flop and the accompanying buffer for the “Q” output. The layout measured 235 X 140 microns, or approximately 32,000 microns\(^2\).
Fig. 5. Layout of each JK Flip-Flop.

Fig. 6. Output buffer layout.
4. Results

Fig. 8 captures output response of the counter to a 100 MHz input clock, while Fig. 9 and 10 depict typical rise, fall and delay times for the counter. Little difference existed in output times from Q0 to Q3, as shown from the data table in Fig. 7. Fig. 8 demonstrates transitions of the Q output by falling clock edges. Note that rise and fall times were in the picosecond range, while delay from clock to Q was on the order of 1.25 nanoseconds.

<table>
<thead>
<tr>
<th>Load Capacitance (pF)</th>
<th>Q0 Rise (ns)</th>
<th>Q0 Fall (ns)</th>
<th>Q0 Delay (ns)</th>
<th>Q1 Rise (ns)</th>
<th>Q1 Fall (ns)</th>
<th>Q1 Delay (ns)</th>
<th>Q2 Rise (ns)</th>
<th>Q2 Fall (ns)</th>
<th>Q2 Delay (ns)</th>
<th>Q3 Rise (ns)</th>
<th>Q3 Fall (ns)</th>
<th>Q3 Delay (ns)</th>
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</table>

Fig. 7. Simulated data results for rise, fall and delay times of the 4-bit counter.
Fig. 8. Simulated results showing a 100 MHz input clock

Fig. 9

Typical Output Rise and Fall Times

![Graph showing typical output rise and fall times vs load capacitance.]

- Blue line: Rise Time
- Red square: Fall Time
5. Conclusion
A 100 MHz synchronous 4-bit counter was successfully designed and implemented in an AMI-0.6 micron process. Results demonstrated fast rise and fall times and low clock to output delays driving 5 pF loads. Good results could be anticipated for even greater clock frequencies and/or capacitive loads.