1. Draw the schematic of the circuit that the layout in Figure 1 represents.

![Figure 1](image)

2. Estimate all the junction areas and perimeters at the labeled nodes of the circuit in Figure 2. Assume that all the $p$-channel transistors have sizes of 10 $\mu$m/0.5 $\mu$m and all the $n$-channels have sizes of 4 $\mu$m/0.5 $\mu$m.

![Figure 2](image)

3. Sketch the layout for the circuit in Figure 2 using $\lambda$ design rules.

**Due 02.05.18**