ECE533 Advanced MOS Concepts and VLSI Design
Spring 2015
S.K. Islam, 504 Min Kao Building, 974-8531, sislam@utk.edu
Office Hours: MWF 10:00-11:00 am

Textbook:

Reference:
- Class handouts

Grading:

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Midterm Exams</td>
<td>40%</td>
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<tr>
<td>Final</td>
<td>25%</td>
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<tr>
<td>Research Paper</td>
<td>10%</td>
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<td>Homework</td>
<td>5%</td>
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<td>Final Project</td>
<td>20%</td>
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<tr>
<td>Total</td>
<td>100%</td>
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Grading Scale:
A(>90%), B+(86 to 89%), B(80 to 85%), C+(76 to 79%), C(70 to 75%), D(60 to 69%), F(<60%)

Lecture Classes will meet in MK 405 from 9:05-9:55 am on Mondays, Wednesdays and Fridays. Class attendance is encouraged and strongly recommended.

The labs are designed to give advanced undergraduates and beginning graduate students a working knowledge of CMOS digital integrated circuit technology, circuit design methodologies, including simulation and physical layout of CMOS digital circuit structures. Cadence and HSpice will be used widely for circuit simulation.

MK 228 VLSI laboratory will be open from 10 am to 5 pm every weekday. However, TAs support will be available by appointment only with the TAs.

Details of the Lab will be posted on the course website.

Lab 1: Set-up of Cadence on Ada Machines
Lab 2: Schematic Entry of Inverter and Simulation
Lab 3: Cadence Layout of Inverter
Lab 4: Post Layout Simulation of Inverter and Generation of LVS
Lab 5: Schematic Entry, Symbol and Layout of Complex Gate (NOR)
Lab 6: Schematic Entry, Symbol and Layout of Complex Gate (NAND)
Lab 7: Schematic, Layout and Simulation of a 2X1 Multiplexer

Final Project:
Design of a 4-bit counter
Course Topics:

Introduction to CMOS Circuits
MOS Transistor Theory
CMOS Process Video
CMOS Processes
CMOS Layout
Modeling of MOS transistors
Combinational MOS logic circuits
Transmission Gates and Fully-Differential Logic
Delay Characterization
Latches, Flip-Flops and Synchronous System Design
I/O circuits
Bipolar and BiCMOS Logic Gates
Standard Cell Methodology
Capacitance Characterization
Transient Analysis
Clocked Systems
Dynamic Logic
Integrated Memories

Academic Dishonesty: Will NOT be tolerated and NO WARNINGS will be given. It is the responsibility of the student to review UT policy and procedures in this area since they will be strictly adhered to. Cheating will result in an F in the course, and possible university sanctions.