ECE533 Advanced MOS Concepts and VLSI Design
Spring 2018
S.K. Islam, 504 Min Kao Building, 974-8531, sislam@utk.edu
Office Hours: MWF 11:00-12:00 noon

Teaching Assistants: Peixing Liu (pliu7@vols.utk.edu)


Reference:
- Class handouts

Grading:  
- Midtem Exams 40%
- Final 25%
- Research Paper 10%
- Homework 5%
- Final Project 20%
- Total 100%

Grading Scale:
A(>90%), A-(88 to 89%), B+(85 to 87%), B(80 to 84%), B-(78 to 79%), C+(75 to 77%), C(70 to 74%), D (60 to 69%), F(<60%)

Lecture Classes will meet in MK 525 from 10:10-11:00 am on Mondays, Wednesdays and Fridays. Class attendance is encouraged and strongly recommended.

The labs are designed to give advanced undergraduates and beginning graduate students a working knowledge of CMOS digital integrated circuit technology, circuit design methodologies, including simulation and physical layout of CMOS digital circuit structures. Cadence and HSpice will be used widely for circuit simulation.

MK 228 VLSI laboratory will be open from 10 am to 5 pm every weekday. However, TAs support will be available by appointment only with the TAs.

Details of the Lab will be posted on the course website.

Lab 1: Set-up of Cadence on Ada Machines
Lab 2: Schematic Entry of Inverter and Simulation
Lab 3: Cadence Layout of Inverter
Lab 4: Post Layout Simulation of Inverter and Generation of LVS
Lab 5: Schematic Entry, Symbol and Layout of Complex Gate (NOR)
Lab 6: Schematic Entry, Symbol and Layout of Complex Gate (NAND)
Lab 7: Schematic, Layout and Simulation of a 2X1 Multiplexer
**Final Project:**

Design of a 4-bit counter

**Course Topics:**

- Introduction to CMOS Circuits
- MOS Transistor Theory
- CMOS Process Video
- CMOS Processes
- CMOS Layout
- Modeling of MOS transistors
- Combinational MOS logic circuits
- Transmission Gates and Fully-Differential Logic
- Delay Characterization
- Latches, Flip-Flops and Synchronous System Design
- I/O circuits
- Bipolar and BiCMOS Logic Gates
- Standard Cell Methodology
- Capacitance Characterization
- Transient Analysis
- Clocked Systems
- Dynamic Logic
- Integrated Memories

**Academic Dishonesty:** Will *NOT* be tolerated and **NO WARNINGS** will be given. It is the responsibility of the student to review UT policy and procedures in this area since they will be strictly adhered to. Cheating will result in an F in the course, and possible university sanctions.