Multilevel Converters for Large Electric Drives

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***Abstract*¾ Traditional 2-level high-frequency pulse width modulation (PWM) inverters for motor drives have several problems associated with their high frequency switching which produces common-mode voltage and high voltage change (dV/dt) rates to the motor windings. Multilevel inverters solve these problems because their devices can switch at a much lower frequency. Two different multilevel topologies are identified for use as a converter for electric drives, a cascade inverter with separate dc sources and a back-to-back diode clamped converter. The cascade inverter is a natural fit for large automotive all-electric drives because of the high VA ratings possible and because it uses several levels of dc voltage sources which would be available from batteries or fuel cells. The back-to-back diode clamped converter is ideal where a source of ac voltage is available such as a hybrid electric vehicle. Simulation and experimental results show the superiority of these two converters over PWM based drives.**

I. INTRODUCTION

A. Background

Large electric drives will require advanced power electronic inverters to meet the high power demands (>1 MW) required of them. One inverter type which is uniquely suited for this application is the multilevel inverter [1]. Two different multilevel converter topologies are ideal for use as large electric drives. The cascaded inverter with separate dc sources closely fits the needs of all-electric vehicles because it can use the onboard batteries or fuel cells to synthesize a sinusoidal voltage waveform to drive the main vehicle traction motor. Where generated ac voltage is available, a back-to-back diode clamped converter can be used to output variable frequency ac voltage for the driven motor.

Multilevel inverters also solve problems with present 2-level pulse width modulation (PWM) adjustable speed drives (ASD's). Adjustable speed drives usually employ a front-end diode rectifier to convert utility ac voltage to dc voltage and an inverter to convert the dc voltage to variable frequency and variable voltage for motor control. Motor damage and failure has been reported by industry as a result of adjustable speed drive inverters' high frequency PWM switching. The main problems reported have been "motor bearing failure" and "motor winding insulation breakdown" because of circulating currents, dielectric stresses, voltage surge, and corona discharge [2-4]. The cause of these circulating currents are related to the capacitive elements between different winding layers and between the winding conductor and motor shaft being subjected to common-mode voltage and high voltage transients.

Only recently have motor insulation failures become a problem with adjustable speed drives because the power semiconductor switches are now able to switch fast enough such that the voltage change rate (dV/dt) is high enough to induce the damaging circulating currents and corona discharge between the winding layers. Present power semiconductors can be turned on and off within one microsecond for 600 V and higher voltages which can generate broadband electromagnetic interference (EMI). Although the fast switching can increase the motor running efficiency and the switching frequency is well above the acoustic noise level, the dV/dt associated capacitive coupling currents in the motor and dielectric stresses between insulated winding turns are also greatly increased.

Another drawback of conventional adjustable speed drives is efficiency. Because the inverter must switch at supersonic frequency, the associated switching losses (turn-on and turn-off losses) are normally much higher than the device conduction loss, which results in low efficiency power conversion from dc to ac [5].

In summary, the problems associated with conventional adjustable speed drive inverters are as follows:

1. High dV/dt and voltage surge because of switching causes motor bearing failure and stator winding insulation breakdown.
2. High-frequency switching requires significant derating of switching devices and generates large switching losses.
3. High-frequency switching generates broadband (10 kHz to 30 MHz) EMI to nearby communication or other electronic equipment.

B. Multilevel Inverters

The multilevel voltage source inverters' unique structure allows them to reach high voltages with low harmonics

Prepared by the Oak Ridge National Laboratory, Oak Ridge, Tennessee 37831-8058, managed by Lockheed Martin Energy Research, Inc. for the U.S. Department of Energy under contract DE-AC05-96OR22464.

without the use of transformers. The general function of the multilevel inverter is to synthesize a desired voltage from several levels of dc voltages. For this reason, multilevel inverters can easily provide the high power required of a large electric drive.

As the number of levels increases, the synthesized output waveform has more steps, which produces a staircase wave that approaches a desired waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases approaching zero as the number of levels increases. As the number of levels increases, the voltage which can be spanned by connecting devices in series also increases. The structure of the multilevel inverter is such that no voltage sharing problems are encountered by the series-connected devices.

Three types of multilevel inverters have been proposed by researchers thus far: the diode-clamped inverter, the flying-capacitor inverter, and the cascade inverter. Proposed uses for these converters have included static var compensation [5-12], back-to-back high voltage intertie [13-15], and adjustable speed drives [15-20].

Using multilevel inverters as drives for electric motors is a much different application than for static var compensation. Only reactive power flows between the converter and the system in static var compensation, whereas the converters must handle bidirectional real power flow in the case of motor drives.

Three, four, and five level rectifier-inverter drive systems which have used some form of multilevel PWM as a means to control the switching of the rectifier and inverter sections have been investigated in the literature [16-20]. Multilevel PWM reduces the high dV/dt experienced in traditional high frequency PWM drives because switching is between several smaller voltage levels. However, switching losses and voltage total harmonic distortion (THD) are still relatively high for these proposed schemes; the output voltage THD at was reported to be 19.7% for a four-level PWM inverter [19].

This paper proposes two multilevel inverter control schemes where devices are switched only at the fundamental frequency and the inverter output line voltage THD is 5 percent. In addition, a control scheme will be demonstrated in the multilevel diode clamped converter that obtains well balanced voltages across the dc link capacitors.

II. CASCADED INVERTERS WITH SEPARATE DC SOURCES

A. General Structure

One converter structure proposed for use as an adjustable speed drive is a multilevel inverter which uses cascaded inverters with separate dc sources (SDCSs). The general function of this multilevel inverter is to synthesize a desired voltage from several sources of dc voltages, which may be obtained from batteries, fuel cells, or solar cells. Fig. 1 shows a single-phase structure of the cascade inverter with SDCSs [6]. Each SDCS is connected to a single-phase full-bridge inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output side by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on. Turning on switches S_2 and S_3 yields $-V_{dc}$. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0.

The ac output of each of the different level full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels in a cascade-inverter is defined by $m=2s+1$, where s is the number of dc sources. An example phase voltage waveform for an 11-level cascaded inverter with five SDSCs and five full bridges is shown in Fig. 2. The phase voltage $v_{an} = v_1 + v_2 + v_3 + v_4 + v_5$.

For a stepped waveform such as the one depicted in Fig. 2 with s steps, the Fourier Transform for this waveform is as follows:

$$V(wt) = \frac{4V_{dc}}{p}\sum_n \left[\cos(nq_1) + \cos(nq_2) + \ldots + \cos(nq_s)\right]\frac{\sin(nwt)}{n}$$

where n = 1, 3, 5, 7, ... (1)

From (1), the magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows:

$$H(n) = \frac{4}{pn}\left[\cos(nq_1) + \cos(nq_2) + \ldots + \cos(nq_s)\right] \quad (2)$$

where n = 1, 3, 5, 7, ...

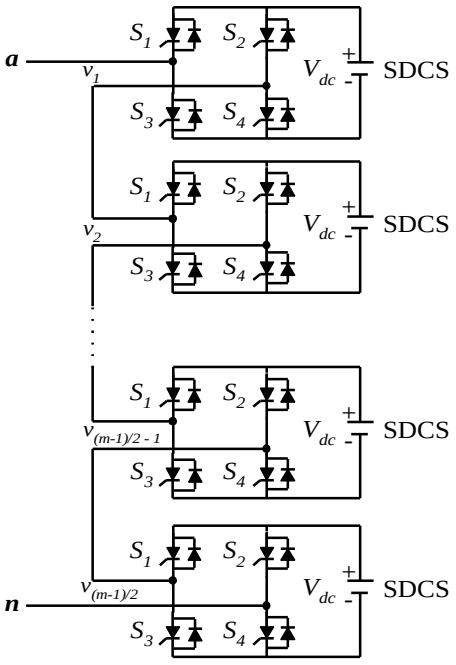

Fig. 1. Single phase structure of a multilevel cascaded inverter.

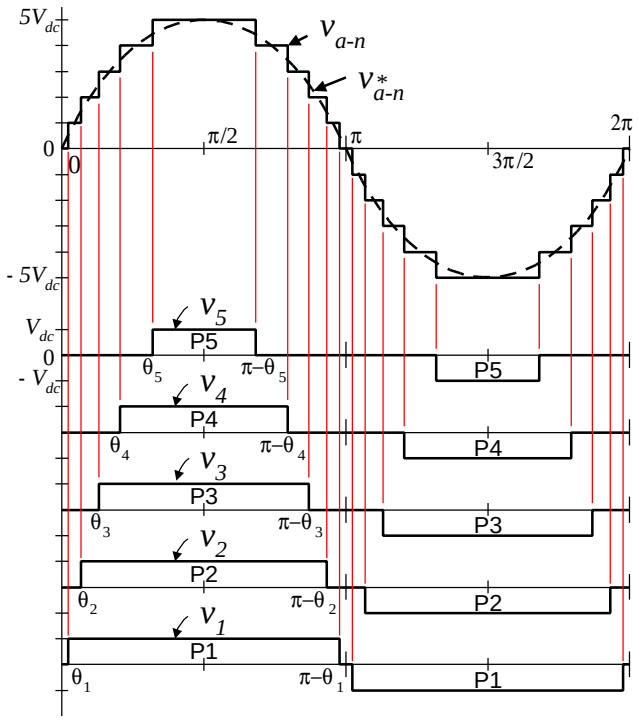

Fig. 2. Output voltage waveform of an 11-level cascade inverter.

The conducting angles, q_1, q_2, ... q_s, can be chosen such that the voltage total harmonic distortion is a minimum. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics [12]. For the 11-level case in Fig. 2, the 5th, 7th, 11th, and 13th harmonics can be eliminated with the appropriate choice of the conducting angles. One degree of freedom is used so that the magnitude of the output waveform corresponds to the reference modulation index, M_i, which is defined as V_L^*/V_{Lmax}, where V_L^* is the amplitude command of the inverter output phase voltage, and V_{Lmax} is the maximum attainable amplitude of the converter, i.e $V_{Lmax} = s \times V_{dc}$ [15]. Let the equations from (2) be as follows:

$$\cos(5q_1) + \cos(5q_2) + \cos(5q_3) + \cos(5q_4) + \cos(5q_5) = 0$$

$$\cos(7q_1) + \cos(7q_2) + \cos(7q_3) + \cos(7q_4) + \cos(7q_5) = 0$$

$$\cos(11q_1) + \cos(11q_2) + \cos(11q_3) + \cos(11q_4) + \cos(11q_5) = 0$$

$$\cos(13q_1) + \cos(13q_2) + \cos(13q_3) + \cos(13q_4) + \cos(13q_5) = 0$$

$$\cos(q_1) + \cos(q_2) + \cos(q_3) + \cos(q_4) + \cos(q_5) = 5M_i \quad (3)$$

The set of equations (3) are nonlinear transcendental equations which can be solved by an iterative method such as the Newton-Raphson method. For example, using a modulation index of 0.8 obtains:

$$q_1 = 6.57°, q_2 = 18.94°, q_3 = 27.18°, q_4 = 45.14°, q_5 = 62.24°.$$

This means that if the inverter output is symmetrically switched during the positive half cycle of the fundamental voltage to $+V_{dc}$ at 6.57°, $+2V_{dc}$ at 18.94°, $+3V_{dc}$ at 27.18°, $+4V_{dc}$ at 45.14°, and $+5V_{dc}$ at 62.24°, and similarly in the negative half cycle to $-V_{dc}$ at 186.57°, $-2V_{dc}$ at 198.94°, $-3V_{dc}$ at 207.18°, $-4V_{dc}$ at 225.14°, $-5V_{dc}$ at 242.24°, the output voltage of the 11-level inverter will not contain the 5th, 7th, 11th, and 13th harmonic components.

B. Three Phase Motor Drive

For a three-phase system, the output voltages of three single phase cascaded inverters can be connected in either a wye or delta configuration. Fig. 3 illustrates the connection diagram for a wye-configured 11-level converter using cascaded-inverters with five SDCSs per phase. In the motoring mode, power flows from the batteries through the cascade inverters to the motor. In the charging mode, the cascade converters act as rectifiers, and power flows from the charger to the batteries.

From Fig. 2, note that the duty cycle for each of the voltage levels is different. If this same pattern of duty cycles is used on a motor drive continuously, then the level 1 battery is cycled on for a much longer duration than the level 5 battery. This means that the level 1 battery will discharge much sooner than the level 5 battery. However, by rotating the duty cycles among the various levels as shown in Fig. 4, the batteries will be discharged or charged evenly, and they all should reach the end of their lifetime near the same time.

In Fig. 4, the fundamental active component of the load current, I_{LaA}, is shown to be in phase with the output load voltage, $V_{La\text{-}n}$. This is the portion of the current that is responsible for charge or discharge of the batteries and contributes to real power flow. The nonactive portion of the current is orthogonal to the output load voltage and does not contribute to charging or discharging of the batteries.

Fig. 5 shows the system configuration and control block diagram of an ASD using an 11-level cascade inverter. The duty cycle look up table contains switching timings to

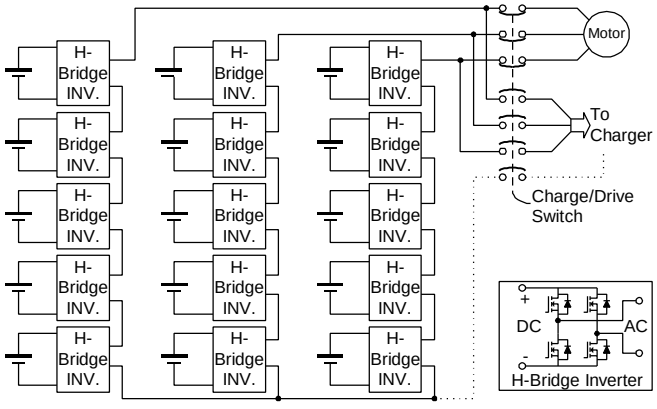

Fig. 3. Three phase wye-connection structure using 11-level cascade inverters for motor drive and battery charging.

generate the desired output voltage as shown in Fig. 2. The switching angles, q_s, (s = 1, 2, 3, 4, 5), are calculated off-line to minimize harmonics for each modulation index, M_i.

An 11-level prototype cascade inverter has been built and used for static var compensation with great success [6-8]. The control scheme for this application is much more complicated than using the inverter as an electric drive because the power phase angles and voltages must be measured and synchronized with the utility. In the near future, this same 11-level prototype will be connected to a battery bank and used to drive an induction motor.

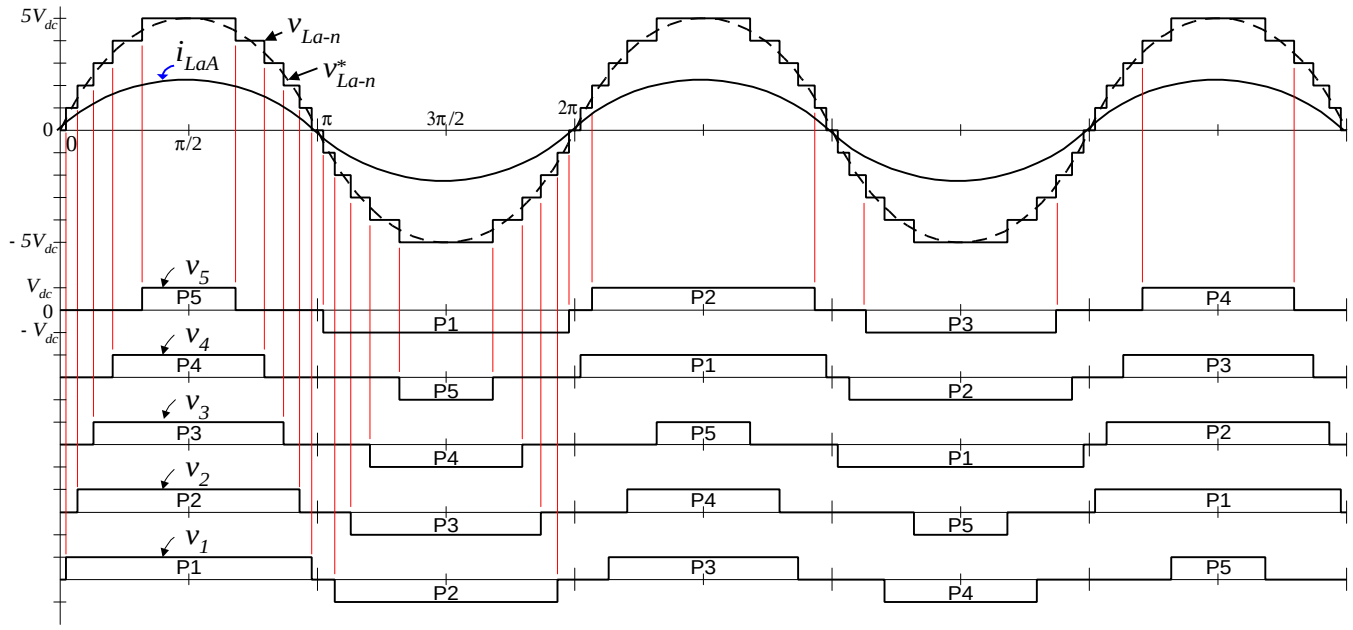

Fig. 4. Cascade inverter drive output voltage levels using duty cycle swapping circuit.

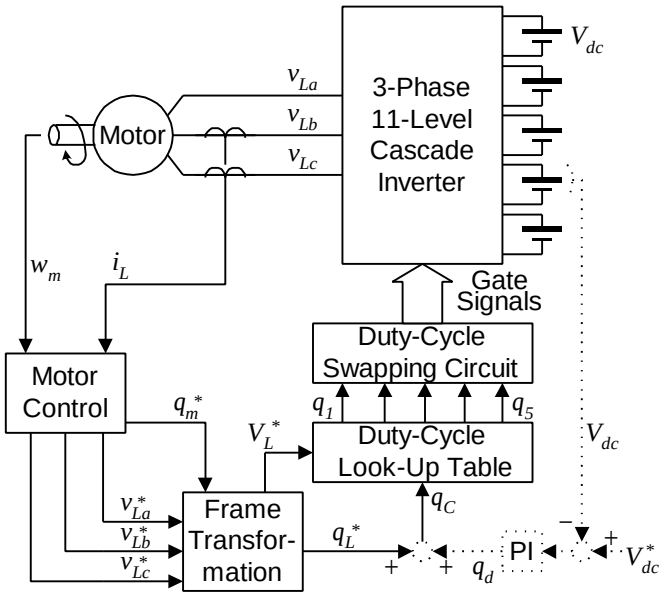

Fig 5. System configuration of an ASD using the cascade inverter.

III. BACK-TO-BACK DIODE CLAMPED CONVERTER DRIVE

Two 6-level diode clamped inverters connected back-to-back are shown in Fig. 6. The dc bus for these two inverters consists of five capacitors in series, and the voltage across each capacitor is V_{dc}. The voltage stress across each switching device is limited to V_{dc} through the clamping diodes.

A. Design and Simulation

Table I lists the voltage output levels possible for one phase of the inverter using the negative dc rail V_1 as a reference voltage. State condition 1 means the switch is on, and 0 means the switch is off. Note that each active device is only switched once per cycle. Each phase has five complementary switch pairs such that turning on one of the switches of the pair requires that the other switch be turned off. The complementary switch pairs for phase leg a are (S_{a1}, $S_{a'1}$), (S_{a2}, $S_{a'2}$), (S_{a3}, $S_{a'3}$), (S_{a4}, $S_{a'4}$), and (S_{a5}, $S_{a'5}$).

Fig. 7 shows phase and line voltage waveforms for one phase of a 6-level inverter. The line voltage V_{ab} consists of a positive phase-leg a voltage and a negative phase-leg b voltage. The resulting line voltage is an 11-level staircase waveform. This means that an m-level diode clamped inverter has an m-level output phase voltage and a (2m-1)-level output line voltage.

Although each active switching device is only required to block a voltage level of V_{dc}, the clamping diodes require different voltage ratings for reverse voltage blocking. Using phase a of Fig. 6 as an example, when all the lower switches $S_{a'1}$ through $S_{a'5}$ are turned on, D_4 must block four capacitor

voltages, or $4V_{dc}$. Similarly, D_3 must block $3V_{dc}$, D_2 must block $2V_{dc}$, and D_1 must block V_{dc}. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, D_n will require n diodes in series; consequently, the number of diodes required for each phase is $(m\text{-}1)\times(m\text{-}2)$. Thus, the number of blocking diodes are quadratically related to the number of levels in a diode clamped converter [13-15].

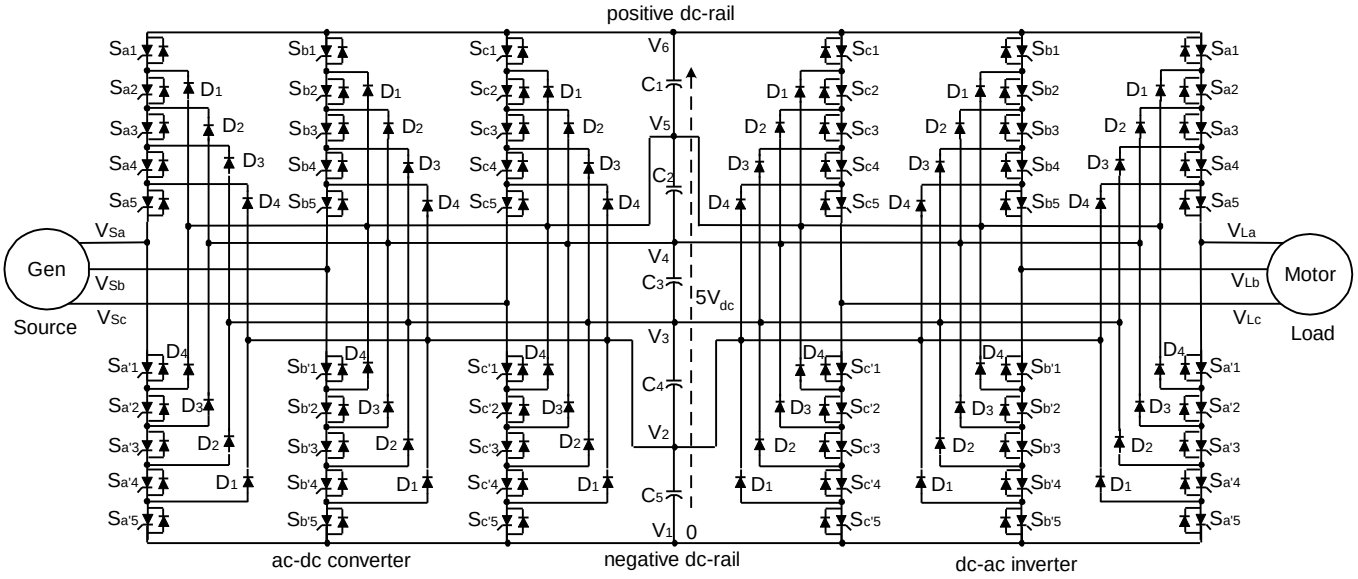

Fig. 6. 6-level diode clamped back-to-back converter structure for motor drive.

B. Experimental Results

A 6-level back-to-back 10 kW converter prototype that was designed to operate at a three phase line voltage of 208 V has been built. The controllable switching devices used for the converter were 100 V, 50 A MOSFETs. Each internal dc level of the converter had a capacitance of 6.72 mF.

Fig. 8 shows the source voltage, V_{Sab}; the source current, I_{Sa}, drawn by the converter; the inverter output load voltage, V_{Lab}; and the load current, I_{La}, drawn by an inductive-resistive load. This prototype diode clamped rectifier drew a source current that had a THD of 3% and could be controlled such that the input power factor was 1.0. The output voltage at the motor terminals had a THD that varied between 4.5% and 5.3%, and the converter output current had a THD of 3%.

Additionally, the experiment shows that the output line voltage dV/dt is reduced by 11 times with the 6-level converter as compared to a traditional 2-level PWM drive. The dramatic one order of magnitude reduction in dV/dt can prevent motor windings and bearings from failure. This 11-step staircase output voltage waveform approaches a sinewave, thus having no common-mode voltage and no voltage surge to the motor windings.

TABLE I
Diode-clamp 6-level converter voltage levels and corresponding switch states

Output	Switch State									
V_{La}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$	$S_{a'5}$
$V_6 = 5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_5 = 4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$V_3 = 2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_2 = V_{dc}$	0	0	0	0	1	1	1	1	1	0
$V_1 = 0$	0	0	0	0	0	1	1	1	1	1

C. Efficiency Measurements

Power at the input and the output of the 10 kW multilevel ASD prototype was measured at several different operating points from no load up to full load. Efficiency of the

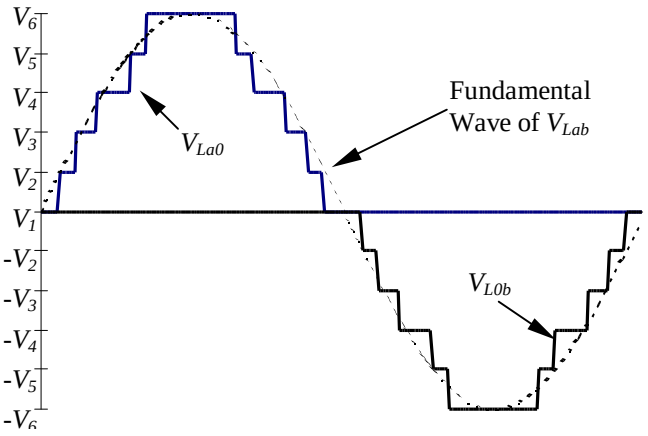

Fig. 7. Phase and line voltage waveforms for six-level diode clamped inverter.

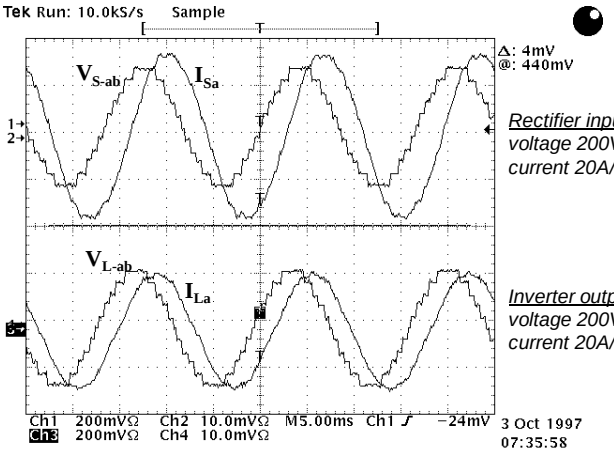

Fig. 8. Experimental voltage and current waveforms at the input and output of the converter prototype operating at a power level of 6 kW.

multilevel converter, which actually consists of *two* multilevel inverters connected back to back, was then calculated to be

$$Efficiency = \frac{Power\ Out}{Power\ In\ (including\ Control\ Power)}, \qquad (5)$$

where *Power In* was measured at the input to the ac-dc converter, *Power Out* was measured at the output of the dc-ac inverter, and *Control Power* was measured to be 25 W.

Fig. 9 shows a graph comparing the efficiency of the back-to-back multilevel converter to a typical industry PWM inverter as a function of their fraction of rated output power. The multilevel converter has an efficiency greater than or equal to 96% for loads greater than 10% rated power, whereas the PWM inverter did not achieve 90% efficiency until it was loaded to greater than 30% rated power. The multilevel converter had an efficiency greater than 98% for loads greater than 40% rated power, but the PWM inverter had a maximum efficiency of 95.6% which was achieved at a loading factor of 95%. The efficiency for a *single* multilevel inverter is greater than 99% over most of its operating range.

D. Capacitor Voltage Balance

One of the keys to using multilevel converters is balancing the voltage across the series connected dc bus capacitors. Capacitors will tend to overcharge or completely discharge at which condition the multilevel converter will revert to a 3-level converter unless an explicit control is devised to balanced the capacitor charge. The method used to accomplish voltage balancing in this back-to-back configuration was to use proportional switching patterns for the rectifier and the inverter portions of the converter. Thus, the real power flow into a capacitor was the same as the real power flow out of the capacitor, and the net charge on the capacitor over one cycle remained the same.

If for some reason the dc capacitors start to have an unbalance in their voltage levels, a modification to the previously described control scheme can be implemented, as shown by the dashed lines in Fig. 5. By monitoring the voltages of each of the dc link levels, minor adjustments can be made to the either the inverter switching angles or the rectifier switching angles which will transfer a net charge into or out of a particular voltage level to adjust the voltage level.

The output of the inverter was connected to a 5 hp, 208 V, three-phase induction motor. Three of the dc voltage levels are shown in Fig. 10 for an output frequency of 32 Hz. The waveforms show that the overall bus voltage remains fairly constant over a cycle, and the internal bus voltages vary only slightly. The figure shows that if the prototype multilevel converter is applied to loads whose speed does not change often or rapidly, the 6.72 mF of capacitance is sufficient for good dc bus voltage regulation.

The inverter was controlled to deliver a continuously varying frequency between 30 Hz and 60 Hz; it took approximately 35 seconds to change between these frequency limits. Fig. 11 shows the same waveforms as Fig. 10 but for a period of 100 seconds. Without active dc bus voltage control, the overall bus voltage varied from 258 Vdc to 304 Vdc. The internal dc voltage levels varied by as much as 16 Vdc. Deceleration of the motor by regenerative braking caused the voltage to increase from its nominal value, and acceleration caused the voltage to decrease from its nominal value. The experimental results have shown that active control of the dc bus voltage by the converter or a larger capacitance is required for the dc voltage levels if the motor speed is going to change fairly rapidly and less variation in the overall dc bus voltage is desired.

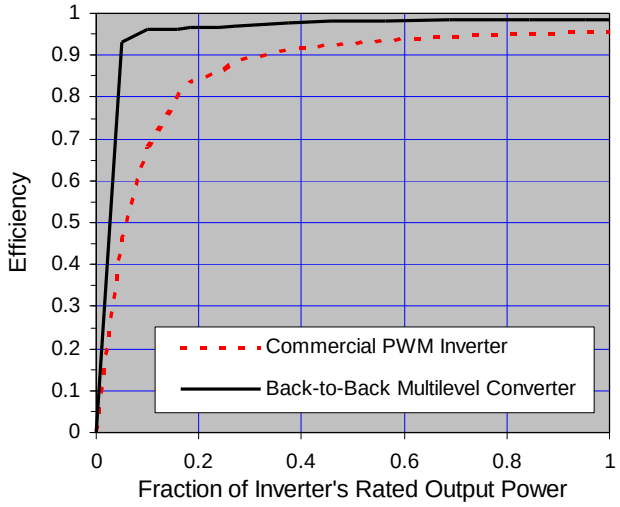

Fig. 9. Plot of converter efficiency as a function of fraction of converter's rated output power.

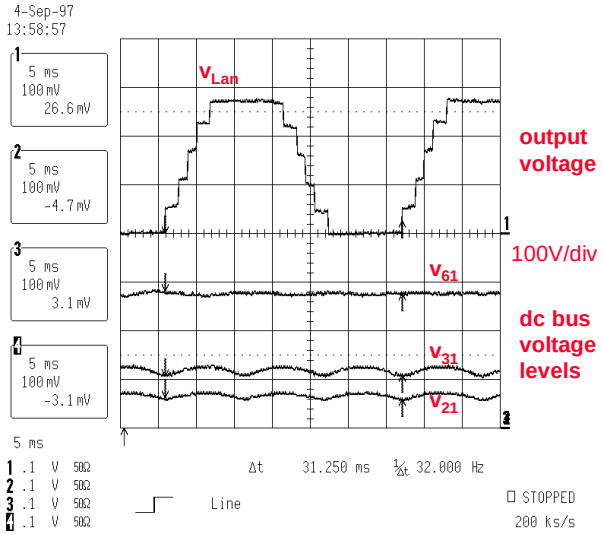

Fig. 10. Internal dc bus voltage levels of the back-to-back converter.

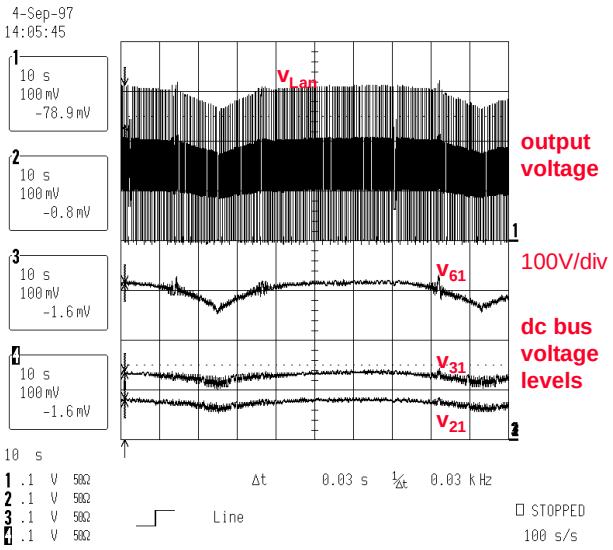

Fig. 11. Internal dc bus voltage levels as converter output frequency is continuously varied between 30 Hz and 60 Hz.

IV. CONCLUSIONS

A multilevel cascade inverter with separate dc sources and a multilevel diode clamped back-to-back converter have been proposed for use in large electric drives. Simulation and experimental results have shown that with a control strategy that operates the switches at fundamental frequency, these converters have low output voltage THD and high efficiency and power factor.

In addition, multilevel converters have been shown to have the following advantages over the traditional PWM inverter:

1. They are more suitable for large VA rated motor drives.
2. Their efficiency is much higher because of the minimum switching frequency.
3. Power factor is close to unity for multilevel inverters used as a rectifier to convert generated ac to dc.
4. No voltage sharing problems exist for series connected devices unlike traditional inverters.
5. Switching stress and EMI are low.

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