

Multilevel PWM Methods at Low Modulation Indices

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Abstract When utilized at low amplitude modulation indices, existing multilevel carrier-based PWM strategies have no special provisions for this operating region, and several levels of the inverter go unused. This paper proposes some novel multilevel PWM strategies to take advantage of the multiple levels in both a diode-clamped inverter and a cascaded H-bridges inverter by utilizing all of the levels in the inverter even at low modulation indices. Simulation results show what effects the different strategies have on the active device utilization. A prototype 6-level diode-clamped inverter and an 11-level cascaded H-bridges inverter have been built and controlled with the novel PWM strategies proposed in this paper.

I. INTRODUCTION

Transformerless multilevel inverters have been proposed for such uses as static var compensation, motor drives, and active power filters. For many of these applications, multilevel inverters will operate in the low amplitude modulation index region, and some levels of the inverter will go unused most of the time if conventional multilevel carrier-based PWM techniques are used.

Many large variable speed drives operate the majority of the time at just a fraction of their rated load. Static var generators and active filters may also operate for long durations well below their rated capabilities, such as at night when production has stopped at a commercial or industrial facility. The multilevel inverters that are the backbone of

these products have to be sized for the largest rated load that will be demanded of them; however, they also should be optimized to operate proficiently over most of their operating regions including at low amplitude modulation indices.

While the multilevel PWM techniques developed thus far have been extensions of two-level PWM methods, the multiple levels in these inverters offer extra degrees of freedom and greater possibilities in terms of device utilization, state redundancies, and effective switching frequency. A need exists for using all of the levels in the inverter at these low modulation index-operating conditions; otherwise, the multilevel inverter loses some of its advantages over the traditional two-level inverter.

Existing multilevel carrier-based PWM strategies have no special provisions when inverters operate at low amplitude modulation indices [1-6]. Multilevel subharmonic PWM developed by Carrara [1] and switching frequency optimal PWM developed by Steinke [2] center the modulation waveform in the carrier bands, and some levels go unused in both these methods at low amplitude modulation indices. The space vector technique developed by Liu [7] for low modulation index regions was because of the use of slow-switching thyristors and not as a means to maximize device utilization. Sinha [8] developed multilevel space vector techniques that use redundant voltage states at low modulation indices to balance dc link capacitor voltages.

In this paper, novel carrier-based multilevel PWM strategies are proposed to increase device utilization in both a diode-clamped inverter and a cascaded H-bridges inverter at low modulation indices. One way to use all of the multiple levels in the inverter, even during low modulation periods, is to take advantage of the redundant output voltage states and to rotate level usage in the inverter during each cycle. This will reduce the switching stresses on some of the lower levels by making use of those higher voltage levels that otherwise would go unused. A procedure is developed in this paper that enables the inverter to switch at higher frequencies during low modulation indices. This increases the frequency spectrum and hastens the dynamic response of the inverter,

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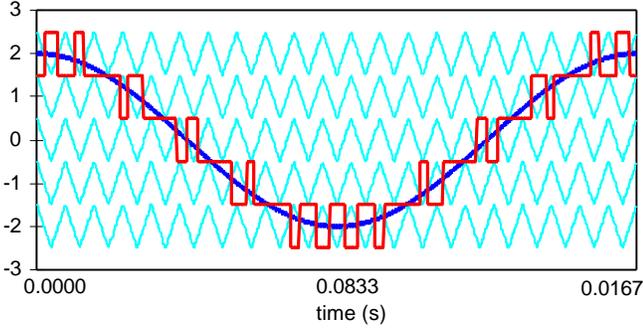


Fig. 1. Multilevel carrier-based SH-PWM showing carrier bands, modulation waveform, and inverter output waveform ($m = 6, m_f = 21, m_a = 0.8$).

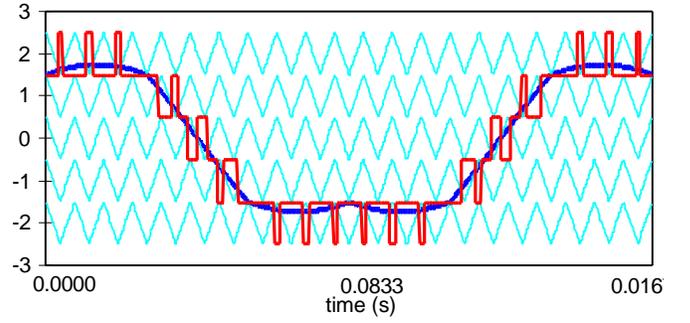


Fig. 2. Multilevel carrier-based SFO-PWM showing carrier bands, modulation waveform, and inverter output waveform ($m = 6, m_f = 21, m_a = 0.8$).

yet does not exceed the allowable switching loss of the active devices.

II. EXISTING MULTILEVEL PWM METHODS

A. Subharmonic PWM Method

Other authors have extended two-level carrier-based PWM techniques to multilevel inverters by making the use of several triangular carrier signals and one reference signal per phase. Carrara [1] developed multilevel subharmonic PWM (SH-PWM) as follows. For an m -level inverter, $m-1$ carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy are contiguous. The reference, or modulation, waveform has peak-to-peak amplitude A_m and frequency f_m , and it is centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off.

In multilevel inverters, the amplitude modulation index, m_a , and the frequency ratio, m_f , are defined as

$$m_a = \frac{A_m}{(m-1) \cdot A_c}, \quad (1)$$

$$m_f = \frac{f_c}{f_m}. \quad (2)$$

Fig. 1 shows a set of carriers ($m_f = 21$) with all of the carriers in phase for a 6-level inverter and a sinusoidal reference voltage with $m_a = 0.8$. The resulting output voltage of the inverter is also shown in Fig. 1.

B. Switching Frequency Optimal PWM Method

Steinke [2] proposed a carrier-based method termed switching frequency optimal PWM (SFO-PWM) which was similar to Carrara's except that a zero sequence (triplen harmonic) voltage is added to each of the carrier waveforms. This method takes the instantaneous average of the maximum and minimum of the three reference voltages (V_a^*, V_b^*, V_c^*) and subtracts this value from each of the individual reference voltages to obtain the modulation waveforms, i.e.,

$$V_{offset} = \frac{\max(V_a^*, V_b^*, V_c^*) + \min(V_a^*, V_b^*, V_c^*)}{2}, \quad (3)$$

$$\begin{aligned} V_{aSFO}^* &= V_a^* - V_{offset}, \\ V_{bSFO}^* &= V_b^* - V_{offset}, \\ V_{cSFO}^* &= V_c^* - V_{offset}. \end{aligned} \quad (4)$$

SFO-PWM is illustrated in Fig. 2 for the same sinusoidal reference voltage waveform that was used in Fig. 1. The resulting modulation waveform and output voltage of the inverter is shown in Fig. 2. The zero sequence modification made by the SFO-PWM technique restricts its use to three-phase three-wire systems; however, it enables the modulation index to be increased by 15% before overmodulation, or pulse dropping, occurs.

III. REDUNDANT SWITCHING STATES

Redundant switching states are those states for which a particular output phase voltage or line-line voltage can be generated by more than one switch combination.

A. Diode-Clamped Inverter

Diode-clamped inverters have redundant line-line voltage states for low modulation indices, but have no phase

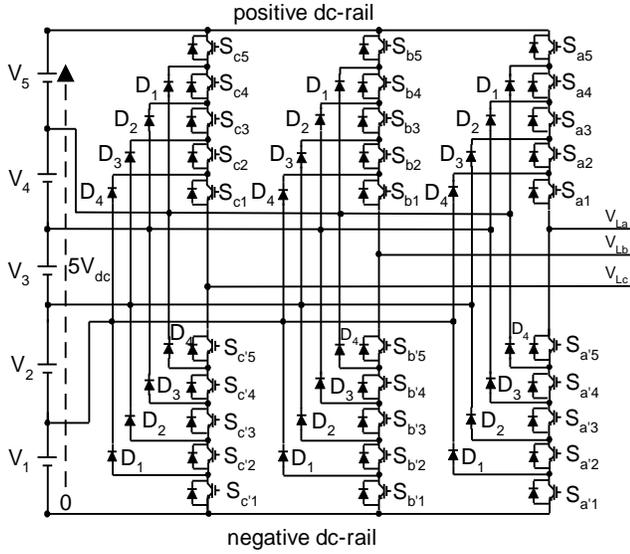


Fig. 3. Three-phase 6-level diode-clamped inverter circuit structure.

redundancies [8-10]. A three-phase 6-level diode-clamped inverter is shown in Fig. 3. As a way to illustrate redundant voltage levels, Sinha [8] developed a set of algebraic matrices to represent the state of the load voltages in terms of the active switches and dc link voltages as follows (from Fig. 3):

$$V_{Labc0} = S_{abc} V_{dc}, \quad (5)$$

$$\text{where } V_{dc} = [V_1 \ V_2 \ V_3 \ \dots \ V_n]^T,$$

$$S_{abc} = \begin{bmatrix} S_{a1} & S_{a2} & S_{a3} & \dots & S_{an} \\ S_{b1} & S_{b2} & S_{b3} & \dots & S_{bn} \\ S_{c1} & S_{c2} & S_{c3} & \dots & S_{cn} \end{bmatrix}, \quad V_{Labc0} = \begin{bmatrix} V_{La0} \\ V_{Lb0} \\ V_{Lc0} \end{bmatrix},$$

$$\text{and } S_{aj} = \sum_j^n \delta(S_a - j),$$

where S_a is the switch state indicating how many upper switches in phase leg a are conducting and is an integer from 0 to n , and where $\delta(x) = 1$ if $x \geq 0$, $\delta(x) = 0$ if $x < 0$.

As an example, assume that the voltage across each of the individual dc sources is identical. If $V_{Labc0} = [1 \ 0 \ 3]^T$, then the line-line voltages are $V_{Lab} = 1$, $V_{Lbc} = -3$, and $V_{Lca} = 2$. The line-line voltages will stay the same if $V_{Labc0} = [2 \ 1 \ 4]^T$ or $[3 \ 2 \ 5]^T$. This example shows that redundant line-line switching states differ from each other by an identical integral value $[h \ h \ h]^T$.

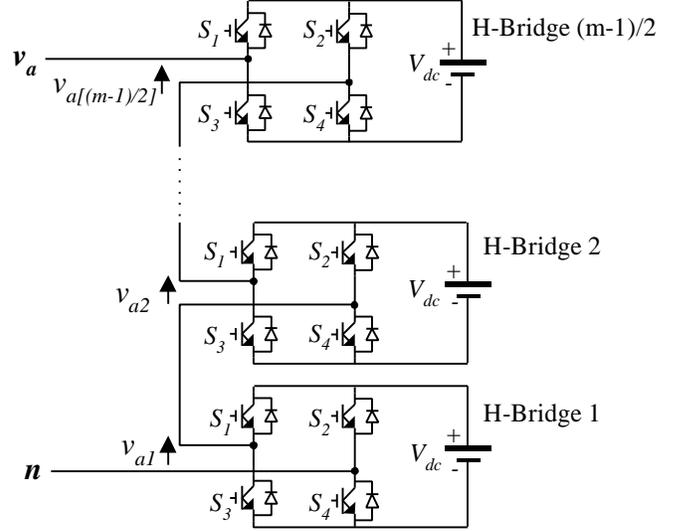


Fig. 4. Single phase cascade inverter structure.

For an output voltage state (i, j, k) in a m -level diode-clamped inverter, the number of redundant states available is given by

$$N_{\text{redundancies available}} = m - 1 - [\max(i, j, k) - \min(i, j, k)]. \quad (6)$$

As the modulation index decreases, more redundant states are available. Table I shows the number of distinct and redundant line-line voltage states available in a six-level inverter for different output voltages.

TABLE I
Diode-clamped 6-level inverter line-line voltage redundancies

| $\max(i,j,k) - \min(i,j,k)$ | # Distinct States | # Redundancies per Distinct State | Total # States |
|-----------------------------|-------------------|-----------------------------------|----------------|
| 0 | 1 | 5 | 6 |
| 1 | 6 | 4 | 30 |
| 2 | 12 | 3 | 48 |
| 3 | 18 | 2 | 54 |
| 4 | 24 | 1 | 48 |
| 5 | 30 | 0 | 30 |
| <i>Total</i> | <i>91</i> | <i>----</i> | <i>216</i> |

In section V, a method is given that makes use of line-line redundancies in a diode-clamped inverter operating at a low modulation index so that active device usage is balanced among the levels.

B. Cascaded H-Bridges Inverter

Unlike the diode-clamped inverter, the cascaded H-bridges inverter has phase redundancies in addition to the aforementioned line-line redundancies. An m -level cascade inverter consists of $N_H = (m-1)/2$ single-phase full bridge inverters connected in series as shown in Fig. 4. The multilevel inverter's output phase voltage V_{an} is formed from the summation of each of the output voltages of the individual H-bridges, which can be controlled independently of one another.

Phase redundancies are much easier to exploit than line-line redundancies because the output voltage in each phase of a three-phase inverter can be generated independently of the other two phases when only phase redundancies are used. In section V, a method is given that makes use of these phase redundancies so that each active device's duty cycle is balanced over $(m-1)/2$ reference waveform cycles regardless of the modulation index.

IV. MODULATION INDEX EFFECT ON SWITCHING UTILIZATION

For very low modulation indices, a multilevel inverter controlled with conventional carrier-based PWM techniques will not make use of all of its levels and thus lose some of its advantages over traditional two-level inverters. The minimum modulation index for which a multilevel inverter controlled with SH-PWM makes use of all of its levels, m , can be calculated as

$$m_{a_{\min}} = \frac{m-3}{m-1}. \quad (7)$$

Table II lists the minimum modulation indices where a multilevel inverter uses all of its possible voltage levels for both SH-PWM and SFO-PWM techniques. Table II also shows that the maximum modulation index before pulse dropping occurs is 1.000 for SH-PWM and 1.155 for SFO-PWM.

As shown in Table II, when a multilevel inverter operates at modulation indices much less than 1.00, not all of its levels are involved in the generation of the output voltage and simply remain in an unused state until the modulation index increases sufficiently. Level usage is more likely to suffer to a greater extent as the number of levels in the inverter increases.

One way to make use of the multiple levels, *even during low modulation periods*, is to take advantage of the redundant output voltage states and to rotate level usage in the inverter during each cycle. This will reduce the switching stresses on some of the lower levels by making use of those higher voltage levels that otherwise would go unused.

For modulation indices less than 0.5, the level usage in odd-level inverters can be sufficiently rotated so that the switching frequency can be doubled and still keep the thermal losses within the limits of the device. For inverters with an even

TABLE II.
MODULATION INDEX RANGES WITHOUT LEVEL REDUCTION (MIN) OR PULSE DROPPING DUE TO OVERMODULATION (MAX) IN MULTILEVEL INVERTER

| | SH-PWM | | SFO-PWM | |
|----|-----------|-----------|-----------|-----------|
| | Min m_a | Max m_a | Min m_a | Max m_a |
| 3 | 0.000 | 1.000 | 0.000 | 1.155 |
| 4 | 0.333 | 1.000 | 0.385 | 1.155 |
| 5 | 0.500 | 1.000 | 0.578 | 1.155 |
| 6 | 0.600 | 1.000 | 0.693 | 1.155 |
| 7 | 0.667 | 1.000 | 0.770 | 1.155 |
| 8 | 0.714 | 1.000 | 0.825 | 1.155 |
| 9 | 0.750 | 1.000 | 0.866 | 1.155 |
| 10 | 0.778 | 1.000 | 0.898 | 1.155 |
| 11 | 0.800 | 1.000 | 0.924 | 1.155 |

TABLE III.
INCREASED CARRIER FREQUENCY POSSIBLE AT LOW MODULATION INDICES

| | Modulation Index, m_a | | Frequency Multiplier |
|---|-------------------------|---------|----------------------|
| | Minimum | Maximum | |
| 3 | 0.000 | 0.500 | 2X |
| 4 | 0.000 | 0.333 | 3X |
| 5 | 0.250 | 0.500 | 2X |
| | 0.000 | 0.250 | 4X |
| 6 | 0.200 | 0.400 | 2X |
| | 0.000 | 0.200 | 5X |
| 7 | 0.333 | 0.500 | 2X |
| | 0.167 | 0.333 | 3X |
| | 0.000 | 0.167 | 6X |
| 8 | 0.285 | 0.428 | 2X |
| | 0.142 | 0.285 | 3X |
| | 0.000 | 0.142 | 7X |
| 9 | 0.250 | 0.500 | 2X |
| | 0.125 | 0.250 | 4X |
| | 0.000 | 0.125 | 8X |

number of levels, the modulation index at which frequency doubling can be accomplished varies with the levels as shown in Table III. This increase in switching frequency enables the inverter to compensate for higher frequency harmonics and will yield a waveform that more closely tracks a reference.

V. LOW MODULATION INDEX PWM TECHNIQUES

A. Diode-Clamped Inverter

As an example of how to accomplish this doubling of inverter frequency, an analysis of a 7-level diode-clamped inverter with an amplitude modulation index, m_a , of 0.4 is

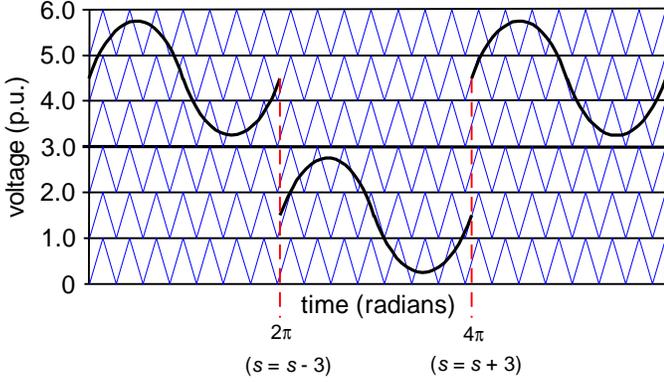


Fig. 5. Reference rotation among carrier bands at low modulation index to achieve carrier frequency doubling ($m = 7$, $m_a = 0.4$, $m_a < 0.5$).

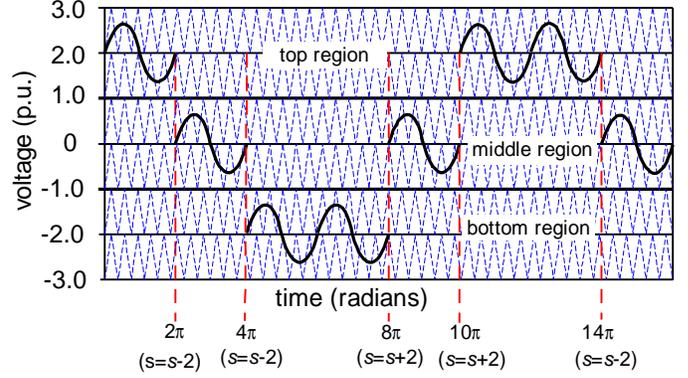
conducted. During one cycle, the reference waveform is centered in the upper 3 carrier bands of the inverter; and during the next cycle, the reference waveform is centered in the lower three carrier bands of the inverter as shown in Fig. 5. This technique enables half of the switches to “rest” every other cycle and not incur any switching losses. With this method, the switching frequency (or carrier frequency f_c in the case of multilevel inverters) can effectively be doubled to $2f_c$, yet the switches will have the same losses as if they were switching at f_c but every cycle.

For the diode-clamped inverter, this method is possible only for 3-wire systems because it has line-line redundancies and no phase redundancies. At the discontinuity where the reference moves from one carrier band set to another, the transition has to be synchronized such that all three phases are moved from one carrier band set to the next set at the same time. In the case of frequency doubling, all three phases add or subtract the following number of states (or levels) every other reference cycle:

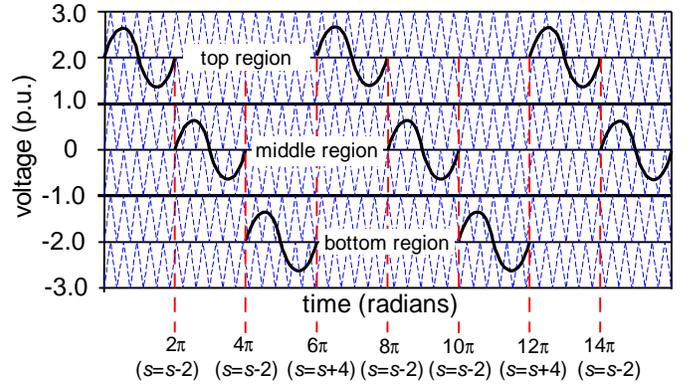
$$S_a(j+1) = S_a(j) + (-1)^j \cdot \frac{\lfloor m-1 \rfloor}{2} \quad (8)$$

This will enable the discontinuity not to show up in the line-line voltage waveform.

At modulation indices closer to zero, the switching frequency can be increased even more. This is possible because the reference waveform can be rotated among different carrier bands for a few cycles before returning to a previous set of switches for use. The switches are allowed to “rest” for a few cycles and thus are able to absorb higher switching losses during the cycle that they are in use. Table III shows the possible increased switching frequencies available at lower modulation indices for multilevel inverters with several different levels.



(a) preferred method



(b) alternate method

Fig. 6. Reference rotation among carrier bands with 3X carrier frequency at very low modulation index ($m = 7$, $m_a = 0.2$, $m_a < 0.333$).

Some additional switching loss is associated with the redundant switchings of the three phases at the end of each reference cycle when rotating among modulation bands. For instance, in Fig. 5 each of the three phases in the seven-level inverter will have three switch pairs change states at the end of every reference cycle. Compared to the switching loss associated with just the normal PWM switchings, however, this redundant switching loss is quite small, typically less than 5% of the total switching loss.

Fig. 6 illustrates two different methods of rotating the reference waveform among three different regions (top, middle, and bottom) for modulation indices less than 0.333 in a seven-level inverter to enable the carrier frequency to be increased by a factor of three. The method shown in Fig. 6(a) is preferred over that shown in Fig. 6(b) because of the reduction in redundant state switching. The method in Fig. 6(a) requires only four redundant state switchings every three reference cycles, whereas the method in Fig. 6(b) requires

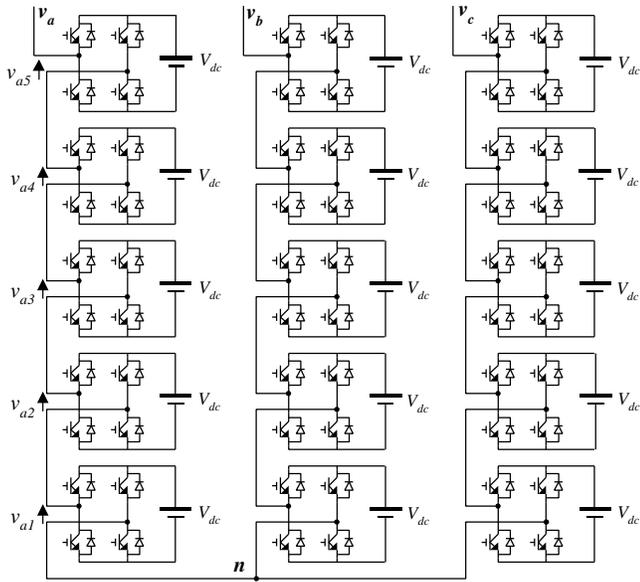


Fig. 7. 11-level wye-configured cascaded inverter.

eight redundant switchings every three reference cycles. In general for any multilevel inverter regardless of the number of levels or number of rotation regions, using the preferred reference rotation method will have $\frac{1}{2}$ of the redundant switching losses that the alternate method would have.

B. Cascaded H-Bridges Inverter

An 11-level three-phase wye-connected cascaded inverter is shown in Fig. 7. In the cascaded H-bridges inverter, each single-phase H-bridge inverter is fed from a separate dc source and can be controlled independently of the other bridges in the inverter. This means that unlike a diode-clamped inverter, a cascade inverter has phase redundancies in addition to line-line redundancies. While the carrier band set rotation techniques shown in the previous section for diode-clamped inverters can also be applied to cascade inverters, making use of the phase redundancies is much more advantageous. Use of phase redundancies does not incur the additional redundant switching losses that occur when line-line redundant switching is used.

When performing multilevel PWM at low modulation indices, this allows rotation of the pulses among the various physical levels (H-bridges) of the cascade inverter. The same pulse rotation technique used for fundamental frequency switching of cascade inverters described in [11, 12] can also be used when a PWM output voltage waveform is desired, which is the case at low modulation indices. The effect is that the output waveform can have a high switching frequency but the individual levels can still switch at a constant switching frequency of 60 Hz if desired.

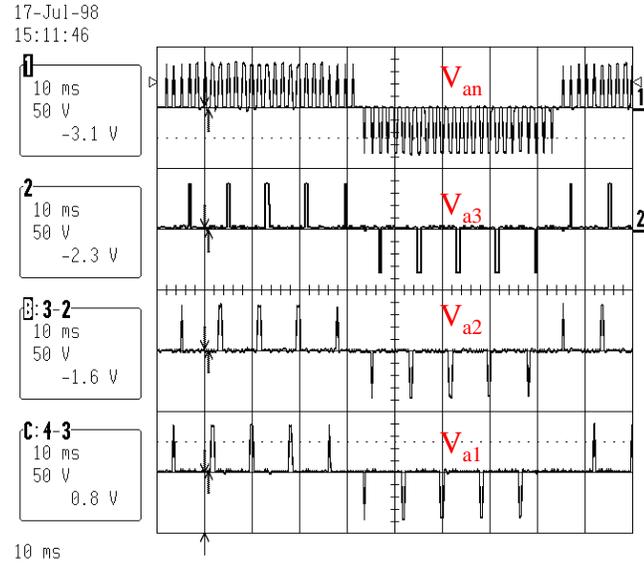


Fig. 8. Pulse rotation in an 11-level prototype cascade inverter.

Example PWM pulses for this type of control are shown in Fig. 8. Pulses (V_{a1} , V_{a2} , and V_{a3}) are shown for three of the five H-bridges that compose the a phase of the inverter. The line-neutral voltage waveform V_{an} is composed of the sum of the pulses from all five H-bridges. While the switching frequency of each individual H-bridge is kept constant at 60Hz, the effective switching frequency of the phase-neutral voltage is 300 Hz. This technique allows a multilevel cascaded inverter to achieve a quality PWM output waveform at low modulation indices without resorting to high frequency switching.

A prototype three-phase 11-level wye-connected cascaded inverter has been built using MOSFETs as the switching devices. A battery bank of 15 separate dc sources (SDCSs) of 36 Vdc each fed the inverter (5 SDCSs per phase). The inverter was used to drive a $\frac{3}{4}$ hp induction motor. The control of the inverter was via a 32-bit digital signal processor. A constant voltage/frequency control technique was applied to the motor drive system. Fig. 9 shows the phase and line-voltage and current waveforms for the driven induction motor. For an amplitude modulation index of 0.2 (to run the motor at 1/5 rated speed), the inverter outputs a 12 Hz fundamental frequency voltage waveform that has three levels line-neutral (V_{an}) and three levels line-line (V_{ab}).

Fig. 10 shows the same waveforms for operating at an amplitude modulation index of 0.3, or reference frequency of 18 Hz. For this operating condition, the inverter's line-line voltage V_{ab} has five levels.

So that all the batteries will be equally discharged (or charged if the cascade inverter operates in a rectification mode), the number of phase-neutral output voltage pulses for

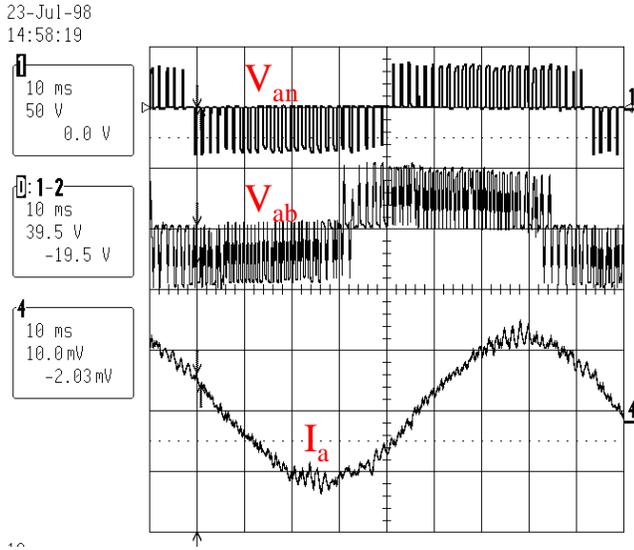


Fig. 9. Cascade inverter waveforms at 12 Hz fundamental frequency operation.

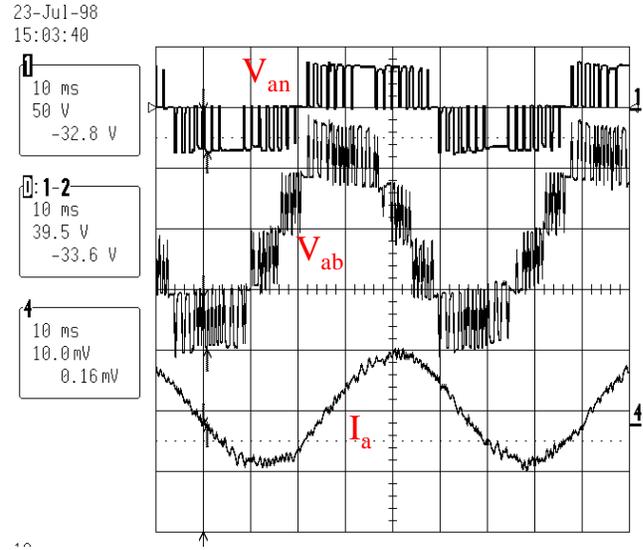


Fig. 10. Cascade inverter waveforms at 18 Hz fundamental frequency operation.

each half cycle of the fundamental frequency waveform should *not* be equal to an integer multiple of the number of H-bridges in one phase of the inverter. Otherwise, each H-bridge would generate the same pulse widths every half cycle, which would lead to different discharge (or charge) rates among the batteries.

VI. CONCLUSIONS

During low modulation index operation of a diode-clamped inverter, rotating the modulation waveform through different bands of carrier waveforms is possible by using line-line redundant voltage states. PWM pulse rotation among the various H-bridges in a cascade inverter takes advantage of phase redundancies to help balance the SDCS voltage states.

These novel carrier-based switching strategies can be used to enable better switch utilization and to achieve an increase in the effective switching frequency without exceeding the thermal limits of the individual active devices. These methods can be used as part of a control system to have minimum distortion in a multilevel inverter's output voltage waveform at low modulation indices.

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