Universal Multilevel DC-DC Converter with Variable Conversion Ratio, High Compactness Factor and Limited Isolation Feature

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***Abstract*- A multilevel dc-dc converter with programmable conversion ratio (CR) is presented in this paper. This converter is a modified version of the MMCCC converter. A universal version of the MMCCC is developed in this paper, and the CR can be easily changed within a wide range. The MMCCC converter is based on capacitor-clamped topology, and the conversion ratio of the circuit depends on the number of active modules. However, like any other capacitor-clamped circuit, the MMCCC circuit requires a large number of transistors and capacitors to attain a high conversion ratio (CR). In this paper, a new circuit module will be introduced that can be connected in a cascade pattern to form the new converter. By using the new modular cell, it is possible to attain very high conversion ratio using a limited number of components, and thus more compactness compared to the predecessor MMCCC circuit can be achieved.**

I. Introduction

Capacitor-clamped dc-dc converters inherently possess several advantageous features such as high efficiency operation, magnetic element-free design construction, low stress per component, and simple operation. There are many reported topologies of capacitor-clamped circuits [1-9], and several of them were investigated in [10]. The key difference between a capacitor-clamped circuit and other genres of dc-dc converters is the distributed stress across the switching elements in the circuit. Thus, the total power handling capability is contributed by multiple transistors and capacitors used in the circuit. This property of capacitor-clamped converters is advantageous over the conventional inductive energy transfer based (IETB) converters such as buck or boost where the entire voltage stress is experienced by a single transistor.

In spite of their advantageous features, most conventional capacitor-clamped converters require a large number of transistors especially when the conversion ratio is high. However, the use of a higher number of transistors can be justified if some capacitor-clamped converters are comparable with the interleaved design of classical IETB converters. In interleaved buck or boost converters, multiple current paths are connected in parallel to reduce the current stress for a single switch. On the other hand, capacitor-clamped converters such as flying capacitor multilevel dc-dc converter (FCMDC) [11] offers stacked-capacitor (multiple capacitors connected in series), and MMCCC [11] offers both stacked-capacitor and cascade configurations to reduce the voltage stress across one single transistor. In addition, the MMCCC circuit can also reduce the current stress by cascading and paralleling current paths inside the circuit [11].

The MMCCC converter construction is based on capacitor-clamped topology. However, the circuit uses a higher number of transistors compared to the FCMDC circuit to offer current path paralleling and modularity in the circuit. For a CR equal to N, the FCMDC circuit requires 2N number of transistors, and the MMCCC requires (3N-2) number of transistors. It was shown in [12] how the MMCCC converter has a better component utilization (CU) compared to the FCMDC converter although the MMCCC requires more transistors for any conversion ratio. In continuation of the improvement phases of the MMCCC converter, a modified version of the MMCCC circuit will be presented in this paper that can offer very high CR without having large number of transistors. It will be shown how the new converter can attain the number of transistors and the CR ratio lower than 2.

II. New Converter Design: Construction

The heart of the universal MMCCC circuit is the 4-transistor 2-capacitor cell shown in Fig. 1. This is slightly different from the unit cell for the MMCCC converter. In each

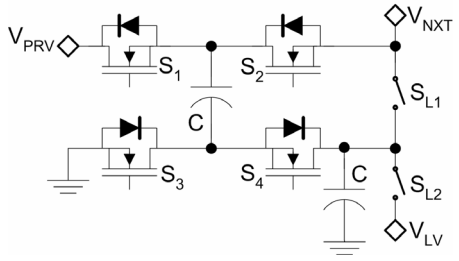

Fig. 1. One module of the new universal MMCCC converter.

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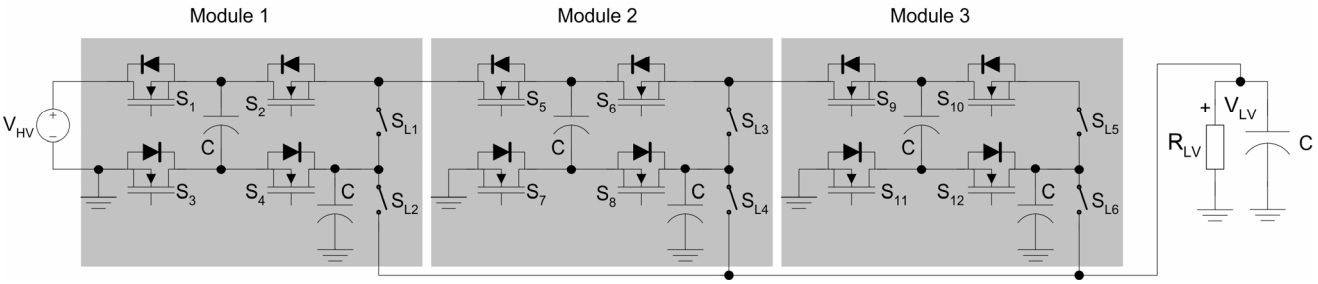


Fig. 2. The schematic of the universal MMCCC circuit with programmable conversion ratio.

cell, 4 transistors are grouped in two bootstrap pairs. Therefore, transistors S_1, S_2 are driven by one bootstrap driver, and S_3, S_4 by another driver. Thus, the gate drive circuit remains almost the same in spite of having one more transistor in the cell. In the original MMCCC cell, there was only one capacitor [11]; however, 2 capacitors are used in the new cell structure. Multiple cells are connected in a cascade pattern to form the converter, and a universal converter having 3 modules is shown in Fig. 2.

Inside each cell, there are two additional selector switches S_{L1} and S_{L2}, and these switches can be used to vary the CR in a wide range. These switches are optional and can be avoided if the converter is operated in one fixed mode. On the other hand, the converter can be interchangeably operated in two different modes using the selector switches. These switches could be transistors or even electromechanical switches depending on the application of the converter. The detailed operating principle of the converter is described in the next section.

III. Circuit Operation

There are two operating modes of the universal MMCCC circuit. By selecting the proper states of S_{L1} and S_{L2}, any module can be configured interchangeably between modes. The operations of these two switches are complementary to each other.

A. Mode 1: Multiplier mode

Inside each module when S_{L1} is closed and S_{L2} is open, the module ends up working as a separate dc-dc converter with a CR equal to 2. This mode can be defined as the multiplier mode. Thus, if S_{L1}, S_{L3} and S_{L5} are closed and S_{L2} and S_{L4} are open in Fig. 2, the CR of the circuit becomes $2\times2\times2 = 8$, and the operational diagram of the circuit is shown in Fig. 3.

B. Mode 2: Normal mode

When S_{L1} is open and S_{L2} is closed inside each module, it works as a regular MMCCC module. When these modules are connected in a cascaded pattern, each module contributes a value of one (1) towards the overall CR of the circuit. Thus when S_{L1}, S_{L3} are open and S_{L2}, S_{L4}, and S_{L6} are closed, the circuit works as a regular MMCCC circuit with a conversion ratio 4 [11]. The operational diagram of the corresponding circuit is shown in Fig. 4. This mode of operation of each module can be defined as the regular or normal mode.

Module 3 or the last module from the left is different from the other two modules because in this module, both the selector switches S_{L5} and S_{L6} are permanently closed for the correct operation of the converter. Thus, module 3 always works in the multiplier mode. The detailed operating principle of the MMCCC converter can be found in [11].

The circuit could be manipulated in many other ways to achieve conversion ratios other than 4 and 8. When module 1 works in the multiplier mode and module 2 works in the regular mode inside a 4-level converter with three modules, the cascade combination of module 1 and 2 creates an MMCCC circuit with a CR of 3. Moreover, module 3 always works in multiplier mode. Thus, when combined with module 3, the overall CR of the circuit becomes $3\times2=6$. When more modules are connected in cascade, more variations in the CR of the circuit can be achieved. In addition, when one of the three modules works in multiplier mode and the other modules are bypassed [12][13], the circuit achieves the minimum CR

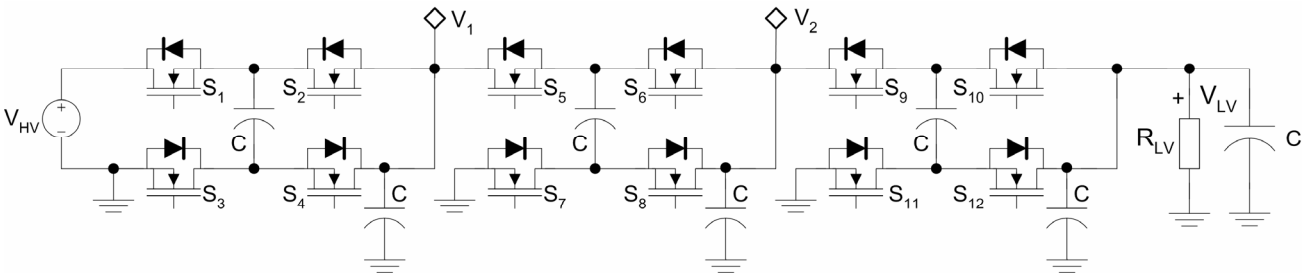


Fig. 3. Schematic of the universal MMCCC for a conversion ratio 8.

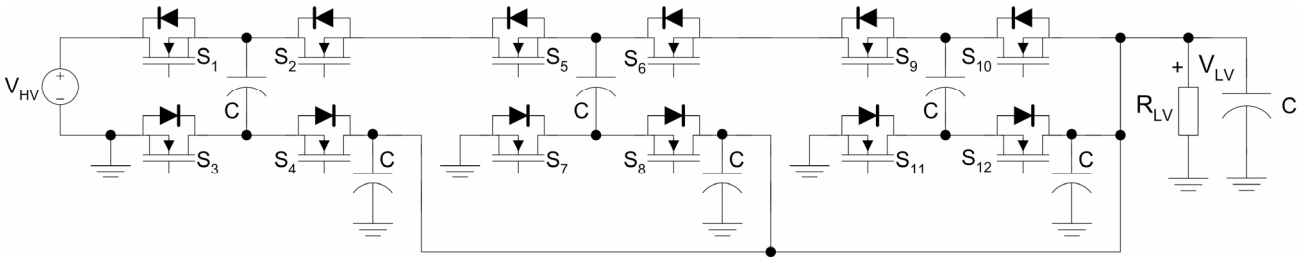


Fig. 4. Schematic of the universal MMCCC for a conversion ratio 4.

TABLE 1
CONVERSION RATIOS OF THE CONVERTER FOR DIFFERENT OPERATING MODES OF THE MODULES.
B = BYPASS, M = MULTIPLIER, R = REGULAR.

CR	Module 1	Module 2	Module 3
2	M	B	B
2	B	M	B
2	B	B	M
3	R	R	B
4	R	R	M
4	M	M	B
6	M	R	M
8	M	M	M

of 2. Thus, the overall CR of the circuit with 3 modules as shown in Fig. 2 can be 2, 3, 4, 6 or 8. Table 1 summarizes the possible CRs of a 3-module converter by assigning different modes for the modules.

IV. ACHIEVING ISOLATION IN THE CIRCUIT

One of the key features of the new universal MMCCC circuit is the limited form of galvanic isolation in the circuit. The input and output of a capacitor-clamped circuit are not usually isolated, and there exists a current path between the high voltage side and the low voltage side of the converter. This phenomenon is observed in FCMDC, MMCCC, series-parallel converter and many other capacitor-clamped converters. When the universal MMCCC is operated in multiplier mode, it can be operated in such a way that the low voltage side can remain isolated from the high voltage side.

Like the original MMCCC circuits, the universal version also has two states of operation; state 1 and state 2. In Fig. 5, S_1, S_4, S_6, S_7, S_9, and S_{12} are operated in state 1, and the remaining six (6) transistors are switched in state 2. However, there is a redundant switching scheme present in the operation of the circuit. In this scheme S_1, S_4, S_5, S_8, S_9, and S_{12} are operated in state 1, and the other transistors are operated in state 2. These schemes are shown in Table 2.

The universal MMCCC circuit performs in the same way using any of these two schemes mentioned above. However, when operating in scheme 1, a limited form of galvanic isolation can be achieved between the high voltage and low voltage side. Fig. 5(a) shows the schematic of a converter with CR equal to 8, and this converter uses switching scheme 1. Fig. 5(b) shows the equivalent charge-flow diagram in state 1, and 5(c) shows the charge-flow diagram in state 2.

In both states, the low voltage side is isolated from the high voltage side. In state 1, the high voltage source is coupled to module 1, and the LV side is coupled with module 2 through module 3. In state 2, the HV side is coupled with module 2 through module 1, and the LV side is coupled with module 3 only. The operating voltage in module 2 is 2 V_{LV} and 1 V_{LV} in module 3. Thus, in worst case, the LV side load experiences a current path through module 2, which is only 2 V_{LV}.

In contrast, the LV side load is powered by a current path that is connected to V_{HV} in the original MMCCC, FCMDC or in a buck converter. Because the LV side shares the same ground with the HV side in the universal MMCCC, this isolation is considered to be limited and not as superior as magnetic isolation.

V. HIGH COMPACTNESS FACTOR

The other attractive feature of the new circuit is the lower component count for a certain CR compared to many other capacitor-clamped circuits especially when the CR is high. In capacitor-clamped or charge pump circuits, the CR is usually a constant integer number [14], and it requires a certain number of transistors to generate that CR. Thus, there exists a ratio of the number of transistors to the CR of the converter, and this ratio indicates the level of compactness of the converter. The lower the ratio, the better is the compactness. In a flying capacitor multilevel dc-dc converter (FCMDC) demonstrated in [3], this compactness factor (CF) is 2. For the original

TABLE 2
DIFFERENT SWITCHING SCHEMES OF THE UNIVERSAL MMCCC AND ACTIVE TRANSISTORS IN STATE 1 AND STATE 2

	Switching Scheme 1		Switching Scheme 2	
	State 1	State 2	State 1	State 2
Active Transistors	S_1	S_2	S_1	S_2
	S_4	S_3	S_4	S_3
	S_6	S_5	S_5	S_6
	S_7	S_8	S_8	S_7
	S_9	S_{10}	S_9	S_{10}
	S_{12}	S_{11}	S_{12}	S_{11}

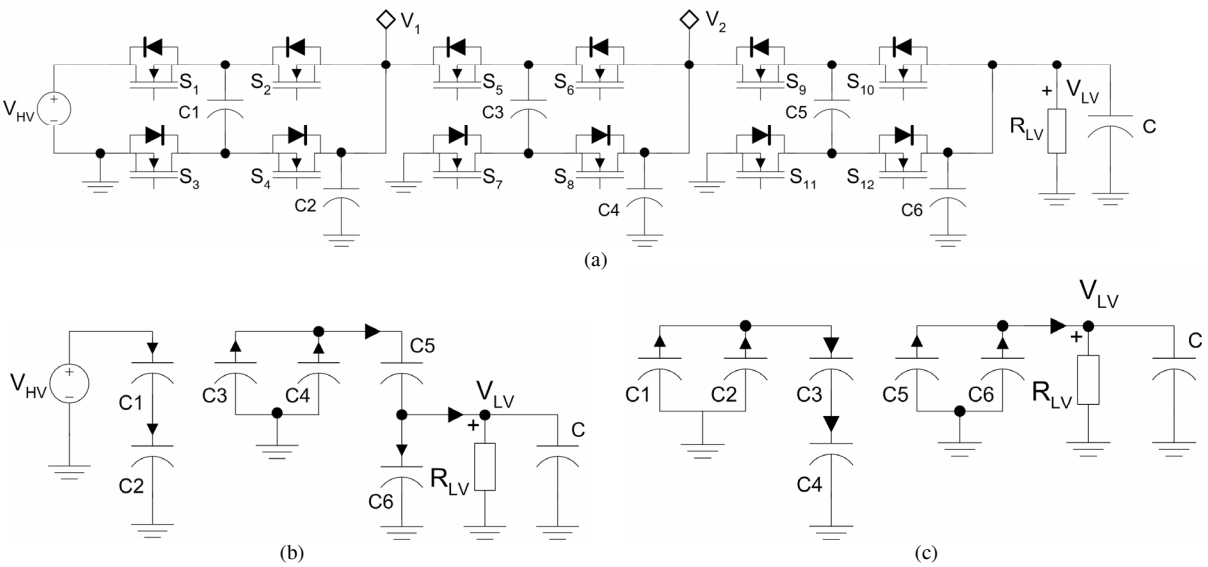


Fig. 5. Charge transfer and balance operation in the 3-module universal MMCCC converter in multiplier mode, and $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C$. (a) circuit schematic, (b) equivalent charge-flow diagram in state 1, (c) equivalent charge-flow diagram in state 2.

MMCCC circuit presented in [11], this factor is (3-2/N) to have features such as modular structure and fault bypass capability. For the series-parallel converter, the CF is the same as the MMCCC circuit [4][5].

The magnetic-less dual voltage dc-dc converter has a modular structure [15]. However, the CF is (N+1); which could be very high when the CR is high. In a switched-capacitor step up dc-dc converter [7], the compactness factor is 3.33. By contrast, the universal MMCCC achieves a conversion ratio (CR) dependent CF, and it could be as low as 1 depending on the CR of the converter. Thus, the new circuit could achieve many desirable features of the MMCCC topology having a smaller number of transistors. The circuit shown in Fig. 2 has 3 modules requiring 12 transistors, and the maximum achievable CR is 8. Thus, CF is 1.5, which is already smaller than the FCMDC circuit. For a 5-level universal MMCCC with 4 modules, the maximum achievable CR is 16, and the required number of transistors becomes 16 also. Thus, the compactness factor is only 1 here. For higher number of modules, this factor drops below 1, and circuit becomes very compact.

For a converter with N modules, the minimum achievable CR would be 2. However, the maximum CR = 2^N.

One module needs four (4) transistors. Thus, the total no. of transistors = 4N.

$$\text{Thus, CF} = \frac{4N}{2^N} = N \bullet 2^{(2-N)} \qquad (1)$$

For N = 4, the CF becomes exactly 1. When more modules are used to achieve higher CR, the CF drops in an exponential manner, and this is shown in Fig. 6.

VI. Moderate Component Utilization

The universal MMCCC circuit has higher component utilization (CU) compared to several flying capacitor converters such as FCMDC. However, the original MMCCC converter performs the best from the CU perspective. The following calculation shows the comparative analysis of CU for four (4) topologies. These calculations are done based on a dc-dc converter where V_{HV} is 40 V, V_{LV} is 5 V, and I_{LV} is 80 A, thus the total output power is 400 W considering the converter is operating in down conversion (buck) mode.

A. Universal MMCCC

To obtain a CR equal to 8, the universal MMCCC needs three (3) modules and twelve (12) transistors, and this is shown in Fig. 2. Each transistor in module 1 experiences a maximum voltage stress of $0.5V_{HV}$, and a maximum current stress if 0.25 I_{LV}. In module 2, the maximum voltage stress is 0.25 V_{HV} and the maximum current stress is 0.5 I_{LV}. In the last module, these stress figures are 0.125 V_{HV} and I_{LV}. Thus the total installed capacity in VA is,

$$(4 \bullet 20 \bullet 20) + (4 \bullet 10 \bullet 40) + (4 \bullet 5 \bullet 80) = 4800VA \qquad (2)$$

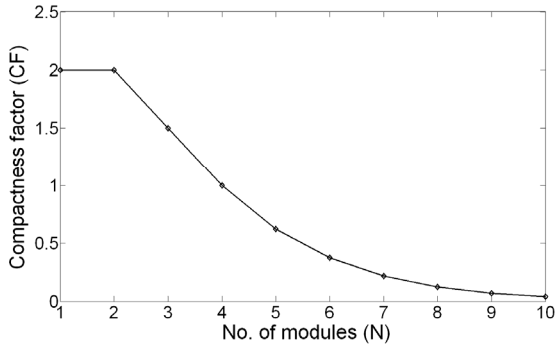


Fig. 6. Correlation of the compactness factor with number of modules. CF drops exponentially with increased number of modules in the circuit.

(With this calculation method – all of the modules cannot be identical (modular) if some have different current ratings or voltage ratings)

B. Original MMCCC

For the original MMCCC, it requires 7 modules and 22 transistors to obtain a CR of 8. There will be four (4) parallel paths to deliver a load current of 80 A. According the method shown in [12], the installed capacity in VA is,

$$(5 \bullet 10 \bullet \frac{80}{4}) + (17 \bullet 5 \bullet \frac{80}{4}) = 2700VA \quad (3)$$

C. FCMDC

For the FCMDC circuit, it takes 16 transistors to produce a CR equal to 8. According to [12], the installed VA of these 16 transistors is,

$$(16 \bullet 5 \bullet 80) = 6400VA \quad (4)$$

D. Buck Converter

For a single transistor classical buck converter, the transistor will experience a maximum voltage stress of 40 V, and a maximum current stress of 160 A considering the converter is operating in critical conduction mode. Thus the installed VA rating would be,

$$(1 \bullet 40 \bullet 160) = 6400VA \quad (5)$$

This analysis shows that the original MMCCC has the best component utilization (CU) among these four (4) topologies. Although the universal MMCCC does not have the best CU, it yields the best compactness factor (CF). Thus, there is a trade off in the design of the universal version that optimizes the CF by sacrificing some CU.

VII. Simulation Results

To verify the concept of the universal MMCCC circuit, a 4-level (3-module) universal MMCCC circuit was simulated in PSIM, and voltages at several nodes were observed. These results are summarized in Fig. 7. The converter was simulated in down conversion (buck) mode, and the universal feature of the converter was observed in two steps. In the first step, all the modules in the converter were configured to work in multiplier mode, and the overall CR was fixed at 8. The HV side voltage was 40 V and a 5 Ω load was connected at the LV side. Some non-idealities such as MOSFET R_{DS}, and capacitor ESR were considered while simulating the circuit. In this mode, the output at the LV side is shown in Fig. 7(a), and the load voltage was 4.85 V. When the converter is simulated in regular mode, the CR becomes 4, and the corresponding output voltage is shown in Fig. 7(b). From simulation, this voltage was found to be 9.9 V. In the last step, the converter was operated in multiplier mode, and the voltages at V_{HV}, V_1, V_2 and V_{LV} were observed simultaneously. This is shown in Fig. 7(c)

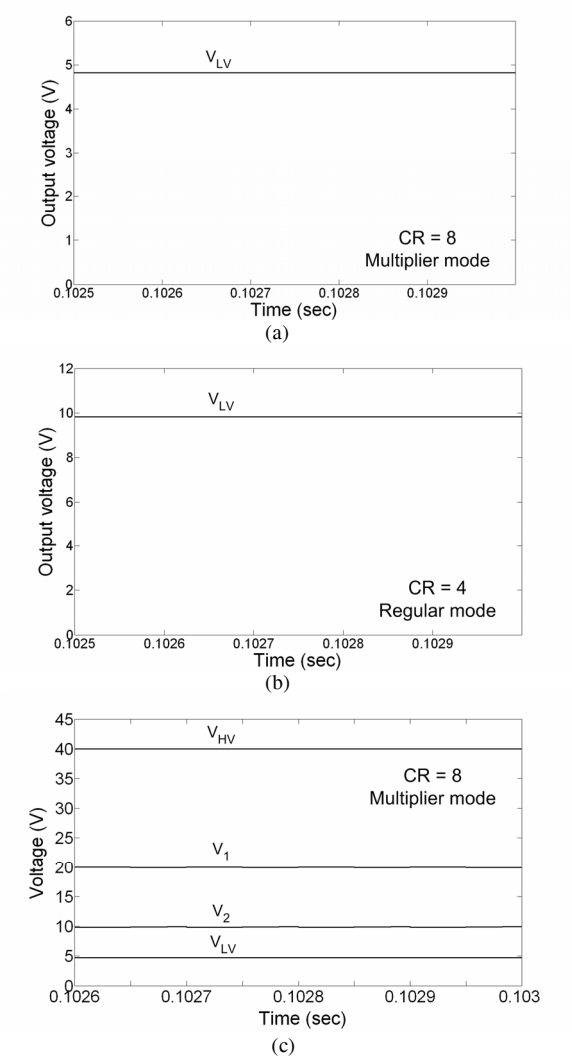


Fig. 7. Simulation results of various node voltages of the universal MMCCC circuit. The input voltage was 40 V, and a 5 Ω load was connected at V_{LV}. a) output voltage V_{LV} for CR = 8, b) output voltage V_{LV} for CR = 4, c) voltages recorded at nodes V_{HV}, V_1, V_2, and V_{LV} with CR = 8.

From Fig. 7(a), it can be seen that the concept of the new topology works, and the circuit can also work as a combination of three individual MMCCC circuits. In addition, Fig. 7(b) demonstrates that this universal converter circuit can also work as a regular MMCCC circuit. Thus, the introduction of the new modular cell presents a unified approach that can create a link between the original MMCCC and the modified MMCCC converter. Finally Fig. 7(c) shows that the overall CR of the converter is the product of CRs of three (3) individual converters. This is why V_1 is approximately two (2) times V_2, and V_2 is about two (2) times V_{LV}.

VIII. Experimental Results

For a complete verification of the concept, a 5-level (4-

module) universal converter was fabricated and tested in both modes. Fig. 8 shows the photograph of the converter. By using appropriate gate signals, three (3) out of these four (4) modules were used to generate the experimental results. Four (4) IRFI540N MOSFETs and two (2) 1000 μF general purpose electrolytic capacitors were used to form one module. Two (2) bootstrap gate drive circuits (IR2110) were used to drive four (4) MOSFETs inside each module.

In the first step, the converter was configured in the multiplier mode and in this mode, the CR was 8. For an input voltage 40 V, the theoretical output voltage should be 5 V at no load condition. With a 5 Ω load at the output, the LV side voltage was recorded and shown in Fig. 9(a), and the measured voltage was 4.77 V.

By configuring the converter in regular mode, the CR became 4, and the corresponding output voltage is shown in Fig. 9(b). This time, the voltage found at the LV side was 9.69V.

In the third step, the converter was operated in multiplier mode, and the voltages V_1, V_2 and V_{LV} in Fig. 3 were recorded, and they are shown in Fig. 9(c). From this experiment, it can be shown that the overall CR of the circuit is a product of the CRs of individual MMCCC circuits. V_1 is the output of module 1, and this is approximately half of V_{HV}. Again, V_1 works as the input of module 2, and V_2 is the output of module 2. Thus, V_2 is close to the half of V_1. And finally, V_2 works as the input to module 3, and it is about two times of V_{LV}.

Therefore, the use of these three (3) modules in the circuit can produce various outputs such as $V_{HV}/2$, $V_{HV}/4$ and $V_{HV}/8$ without changing the mode. Also from [11], the universal MMCCC circuit can generate other dc voltage levels by changing the mode into the regular configuration.

IX. Conclusions and Future Work

A new multilevel capacitor clamped converter has been presented here which is a modified version of the MMCCC converter. This new converter has many desirable features of the MMCCC converter. In addition, the universal configuration of the converter can obtain a very high conversion ratio (CR) using a minimum number of

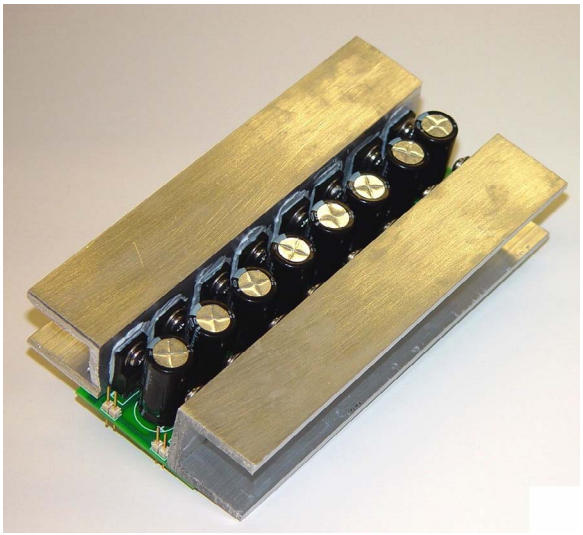
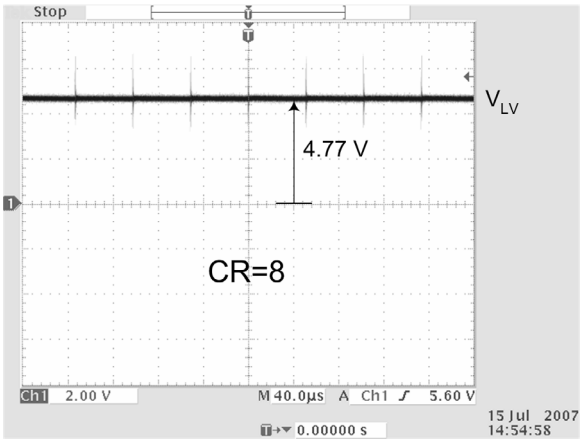
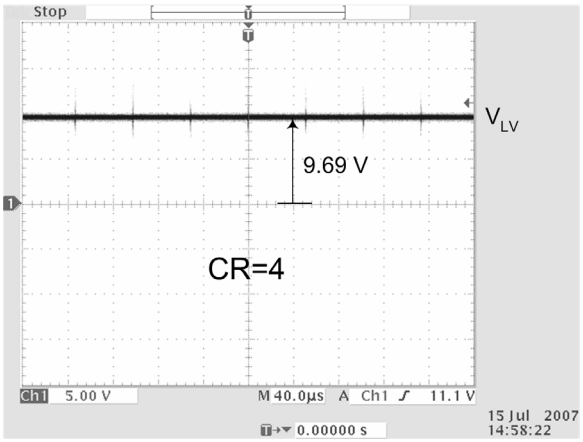


Fig. 8. Photograph of a 100 W prototype of the universal MMCCC converter.



(a)



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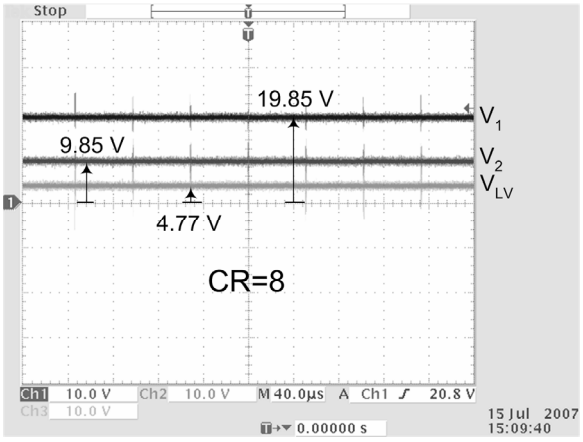

(c)

Fig. 9. The experimental node voltages of the universal MMCCC circuit at nodes V_1, V_2 and V_{LV}. The input voltage was 40 V, and a 5 Ω load was connected at V_{LV}. a) the output voltage for CR = 8, b) output voltage for CR = 4, c) voltages recorded at the output of module 1, 2 and 3 with CR= 8.

components thereby achieving a high compactness factor (CF). As a proof of concept, a 4-module universal MMCCC converter has been constructed, and the experimental results found to be consistent with the simulation results. As a next step, another prototype of the universal converter with high power rating could be constructed, and investigated for multiple load-source integration capabilities. Because of the galvanic isolation, this converter has great potentials to be used in hybrid electric or fuel cell automobiles.

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