SOI-Based Integrated Circuits for High-Temperature Power Electronics Applications

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***Abstract*— The growing demand for hybrid electric vehicles (HEVs) has increased the need for high-temperature electronics that can operate at the extreme temperatures that exist under the hood. This paper presents a high-voltage, high-temperature SOI-based gate driver for SiC FET switches. The gate driver is designed and implemented on a 0.8-micron BCD on SOI process. This gate driver chip is intended to drive SiC power FETs for DC-DC converters and traction drives in HEVs. To this end, the gate driver IC has been successfully tested up to 200ºC. Successful operation of the circuit at this temperature with minimal or no heat sink, and without liquid cooling, will help to achieve higher power-to-volume as well as power-to-weight ratios for the power electronics modules in HEVs.**

I. INTRODUCTION

Previously reported high-temperature automotive electronic requirements are presented in Table I [1]. Much of the under-the-hood cavity operates at an ambient temperature in excess of 150°C. The junction temperature of integrated circuits in this environment can be 25°C higher than ambient. Hence, electronics used in automobiles, especially those in proximity to the engine, must be capable of operating at temperatures at or above 150°C.

The alternative to high-temperature devices and circuits is complicated thermal management systems that add mass and volume, resulting in reduced power-to-volume and power-to-weight ratios. These thermal management approaches also introduce additional overhead in the form of longer wires, extra connectors, and cooling systems that add undesired mass and volume to the system, as well as increased potential for failure [1]. An order of magnitude reduction in the overall mass and volume of power electronic modules can be achieved by reducing the need for long interconnects and thermal management systems.

TABLE I. AUTOMOTIVE TEMPERATURE RANGES [1]

In-transmission	150-200°C
On-engine	150-200°C
On Wheel-ABS sensors	150-250°C
Cylinder pressure	200-300°C
Exhaust sensing	Up to 850°C, ambient 300°C

This work presents a silicon-on-insulator (SOI) based high-temperature, high-voltage integrated gate driver circuit for automotive applications. In all power electronic circuits, a gate driver is an essential component to control the "on" and "off" cycling of power switches. In hybrid vehicles (HEVs), plug-in hybrid vehicles (PHEVs), and fuel cell vehicles (FCVs) power converter modules and drivers must be placed close to the engine in order to optimize performance. Hence, the ambient temperature of the gate driver IC will be 150°C or higher. Earlier prototypes of the gate driver circuit have been successfully tested with a SiC power MOSFET at 20 kHz up to 200°C without any heat sink and cooling mechanism [3]-[5]. Improved versions of the gate driver design with additional functionality and more robust design have been fabricated and tested. These new designs incorporate several new features including a temperature-compensated voltage regulator and protection circuits. Measurement results for the new prototype are presented.

II. HIGH TEMPERATURE GATE DRIVER

In the literature reviewed, several gate driver topologies have been presented for FET-based power switches [6]-[10]. Of these designs, only the circuit reported in [9] is capable of operating at junction temperatures up to 200ºC. However, the circuit in [9] is composed of one commercial gate driver chip and several off-chip components, thus there is no treatment on the high temperature design of a fully integrated driver circuit. In this paper, a gate driver circuit consisting of minimum off-chip components is presented. The design considerations for circuits operating in high-temperature environments are discussed throughout this section. A block level diagram of the most recent gate driver circuit design is shown in Fig. 1.

Two gate driver versions will be discussed in this paper: the 3G gate driver and 4G gate driver. For the purposes of this paper, these designs are principally identical, except for the set of on-chip circuits available. The 4G gate driver

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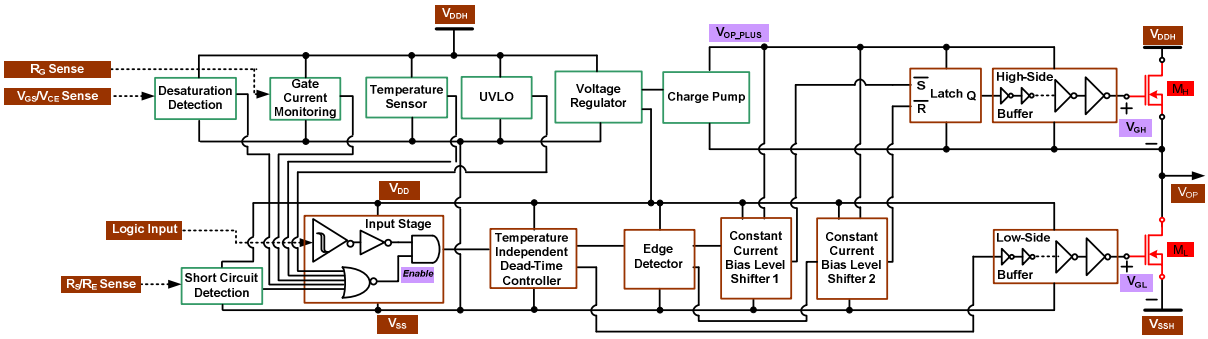

Fig. 1. Core gate driver block diagram.

includes a charge pump, a gate current monitoring circuit, a de-saturation detection circuit, and an enhanced voltage regulator not present on the 3G version. This design discussion will focus primarily on the 4G gate driver. Post-fabrication test data, presented in section IV, was taken on the 3G version of the gate driver design due to its immediate availability.

A. *Core Functionality*

The core functionality of the gate driver is briefly described here but is covered more thoroughly in [3]-[5]. The input stage of this gate driver receives the off-chip, digital control signal. A Schmitt trigger is utilized to create a reliable control signal from the potentially noisy input signal. Feedback signals from the temperature sensor, under-voltage lock out (UVLO), short circuit detection, de-saturation and gate current monitoring circuits provide feedback, in any combination, to a NOR gate which creates a HIGH enable signal. If the enable signal becomes LOW, the output of the gate driver goes LOW, deactivating the power switch.

The dead-time controller circuit block generates two non-overlapping, complementary signals (Inp_H and Inp_L) from the buffered input signal. These signals are then processed to generate appropriate gate signals for the NMOS transistors in the output stage. The Inp_L signal is fed to the buffer for the NMOS switch M_L. Inp_H is input to the edge detector circuit which generates two narrow pulse trains (SET and RESET), one at the rising edge of Inp_H and the other at the falling edge. The level shifter circuits are used to convert the logic-level SET and RESET voltage signals into a current signal. On the high-voltage (VOP_PLUS power rail) side these current signals are converted back into a voltage referenced to the high-side voltage.

Two, large aspect ratio, high-voltage (45-V) NMOS devices (M_L and M_H) constitute the half-bridge output stage of the gate driver circuit. Complementary switching of these two NMOS devices connects the output terminal of the gate driver to one of the two supply rails (V_{DDH} or V_{SSH}). The rail voltages used is determined according to the type of SiC power switch (MOSFET or JFET) being driven by the gate driver. This gate driver is designed to operate on V_{DDH} levels between 10-V to 30-V above V_{SSH}.

The large W/L ratios of the output transistors present a large capacitive load to the control circuitry of the gate driver. Since these output transistors must have fast switching times, multi-stage buffers are employed in the design to mitigate the capacitive loading effects.

B. *Charge Pump*

On the 4G gate driver, a charge pump replaces the bootstrap capacitor and diode used in the 3G gate driver. The bootstrap circuit was used to provide a 5-V floating supply rail to power the high-side circuitry. The high-side circuitry, with its lower rail referenced to V_{OP}, drives the current sourcing NMOS output transistor, M_H. This circuit requires that the gate driver output be turned "off" periodically to allow the bootstrap capacitor to recharge. This effectively limited the lower frequency bound of the 3G gate driver to no less than 1 kHz for reliable operation.

The charge pump (shown in Fig. 2), based on [11], removes the recharge cycle limitation by providing charge independent of the switching state of the gate driver. This independence is accomplished by continually refreshing the charge of capacitor C2, which provides the 5-V rail to the high-side circuitry. The control for the charge pump is provided by a logic signal, V_{SWITCH}, which drives switches S1 and S2. When V_{SWITCH} is high, switches S1 and S2 are "on". S1 allows current to flow through diode D1, charging the boost capacitor C1. S2 pulls the gate voltage of switch S3 down, maintaining it in an "off" state. When switches S1

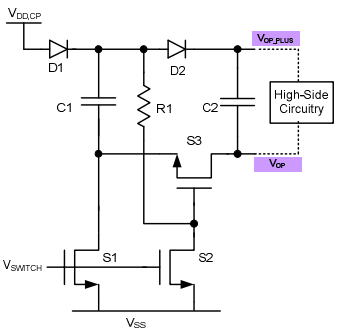

Fig. 2. Basic charge pump topology.

and S2 are turned "off", capacitor C1 begins to charge the gate of switch S3 through resistor R1, which eventually activates switch S3. With S3 "on", capacitor C1 is connected to C2 through S3 and charge is exchanged. When switches S1 and S2 are reactivated, switch S3 is pulled down by S2 and turned "off", while capacitor C1 is again placed in charging mode. With continuous cycling of the logic control signal V_{SWITCH}, charge is maintained on capacitor C2 and power is constantly available to the high-side circuitry of the gate driver. This allows for 100% high-side duty cycle operation.

Signal V_{SWITCH} is generated by a simple 1 MHz on-chip ring oscillator. $V_{DD,CP}$, the power supply used to charge capacitor C1, is supplied by an on-chip voltage regulator designed to provide a temperature-dependent supply voltage of 6.6 V to 6.1 V across 27°C to 200°C. This temperature characteristic approximately offsets the temperature coefficient of diode D1 and D2 and allow for a supply voltage of 5 V to be available to the high side circuitry across the entire temperature range.

C. Voltage Regulator

The 4G gate driver chip requires two, on-chip voltage regulators: the 5-V regulator and the charge-pump (CP) regulator. Both of these regulators are designed using three sub-circuits: a pre-regulator, a voltage reference generator, and an error amplifier [12]. The pre-regulator stage regulates V_{DDH} down to approximately 9.5 V to protect the bipolar devices that are used extensively in the reference generator and the error amplifier stages. This is required because of the relatively low (12-V) collector-emitter breakdown voltage of these devices. The topology utilized by these two regulators, Fig. 3, is based on the LM-723 voltage regulator design [13]. The LM-723 topology utilizes Zener diodes to establish a bias current and a reference voltage. The 5-V regulator is designed to provide a 5-V output voltage with minimum variation over temperature. The charge pump regulator is designed to provide a CTAT (complementary to absolute temperature) output voltage (see Fig. 4).

Several temperature considerations must be made in order to achieve a robust regulator design in extreme environments [14]. The reference generator temperature

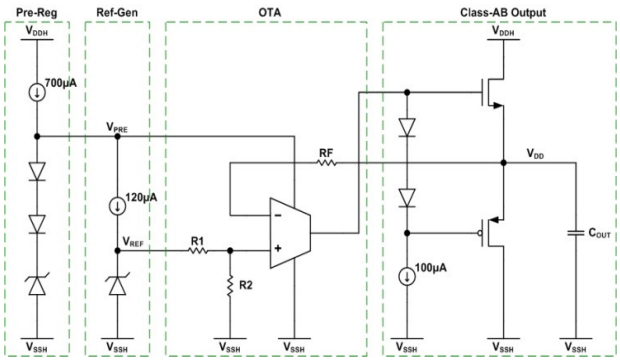

Fig. 3. 5-V and CP voltage regulator topology.

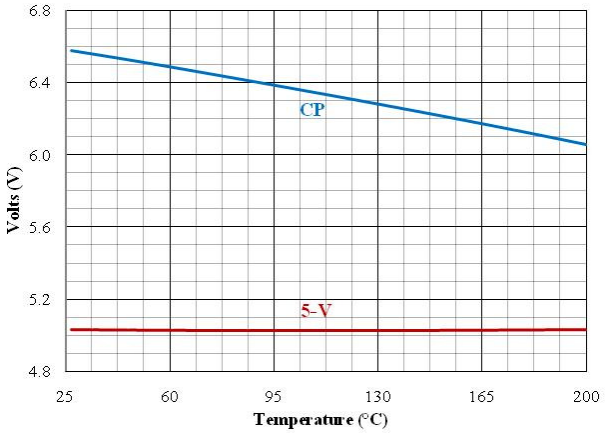

Fig. 4. 5-V and CP voltage regulator temperature characteristic.

compensation scheme used in the 5-V regulator employs a Zener diode and poly resistor to implement temperature coefficient cancelling. This cancellation results in a simulated output voltage variation of less than 5 mV over the 27°C - 200°C temperature range.

The charge-pump regulator modifies the 5-V regulator topology by adding a diode-connected *npn* transistor in series with the reference voltage setting Zener diode. The diode temperature coefficient (-2.8mV/°C) cancels the diode voltage drop of the charge-pump circuit, which yields a "flat" temperature characteristic for the charge-pump circuit [15].

The circuits supplied by these two regulators require large, transient currents (induced by digital switching circuits). The sharp rise time of these load current transients renders the relatively slow feedback path of the regulator's error amplifier ineffectual in regulating the regulator output voltage. The 4G regulators combat this limitation with the use of on-chip output capacitors to supply charge during load current transient events. These capacitors do, however, create a non-dominant pole in the loop transmission of the regulators [16].

To maintain stability, the regulators incorporate a low output impedance, class-AB output stage. The resulting load current transient simulation shows the variation in regulator output voltage during a load current transient of the gate driver (see Fig. 5).

The output voltage of the 5-V regulator is limited to within 95% of the nominal output voltage. This output voltage variation is well within the tolerable range of the gate driver circuits and allows for reliable operation without the requirement of an external capacitor. The charge-pump circuit induces smaller load current transients than the 5-V circuits and, therefore, requires a smaller output capacitor. Both on-chip regulators provide reliable output voltages over wide temperature ranges (−50 °C to 200 °C), varying supply voltages (10 V to 30 V), and many different load conditions (DC loads from 0 mA to 200 mA; load transients up to 200 mA).

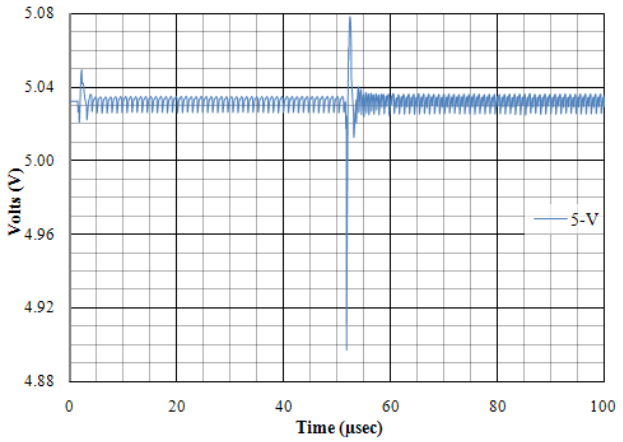

Fig. 5. 5-V voltage regulator load transient behavior.

III. PROTECTION CIRCUITRY

This gate driver contains several protection circuits that will send a fault signal to the gate driver logic if operational boundaries are exceeded. These circuits include an under-voltage lock-out circuit, a short circuit protection circuit, and a gate current monitoring circuit. There is also a novel temperature sensor design employed on both the 3G and 4G gate drivers. It is discussed in depth in [5] and [17].

A. *Under-Voltage Lock Out*

The gate driver circuit utilizes an under-voltage lock out circuit to monitor the power supply voltage and provide an enable signal when a usable voltage is available [18]. The UVLO topology, Fig. 6, implements a current-sourced Zener diode as a reference voltage for power supply comparison. This reference voltage is compared to a resistively-divided (V_{DDH} – V_{SSH}) voltage, where the on-chip resistors, R_1 and R_2 are set according to the value of V_{DDH} – V_{SSH} (via external jumpers).

The incorporation of hysteresis into the design of the UVLO comparator circuit (Fig. 7) stabilizes the UVLO enable signal, which prevents rapid state switching when the resistively-divided V_{DDH} – V_{SSH} is near the UVLO reference voltage [19]. The clamping circuit within the comparator prevents the output voltage from reaching voltages that could damage other gate driver circuits.

Fig. 8 shows the simulated results for the UVLO circuit for the three possible V_{DDH} values. The comparator

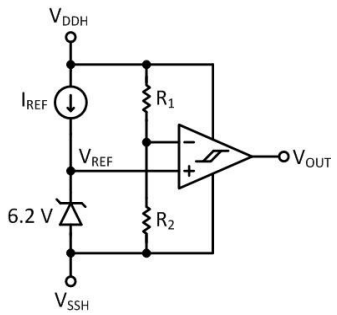

Fig. 6. UVLO topology.

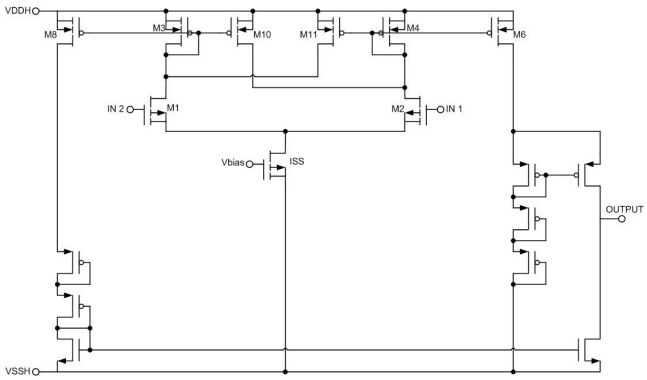

Fig. 7. UVLO comparator.

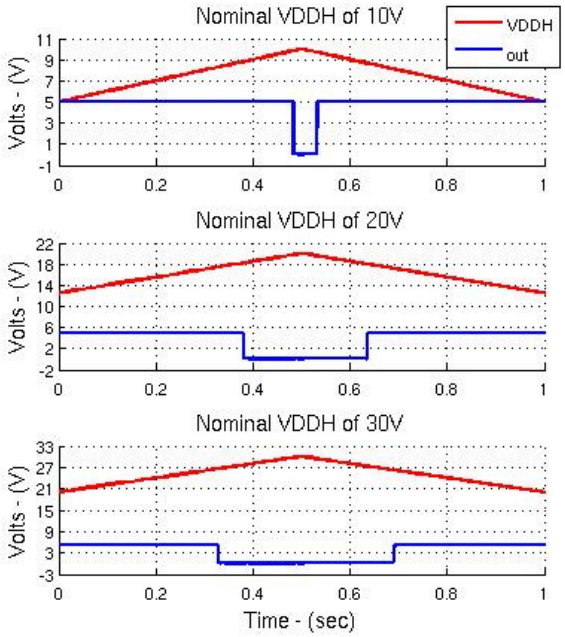

Fig. 8. UVLO simulations.

threshold voltage, V_{REF}, remains constant for each V_{DDH} voltage, while the compared voltage, resistively-divided (V_{DDH} – V_{SSH}) voltage, varies according to V_{DDH}. Therefore, the hysteresis incorporated into the UVLO is proportional to V_{DDH}. This allows the comparator switching points to accommodate wider (V_{DDH} – V_{SSH}) ranges for higher values of V_{DDH}. Table II summarizes the switching thresholds for the UVLO, where V_{TH}^+ is the positive threshold voltage (for rising supply voltage) and V_{TH}^- is the negative threshold voltage (for falling supply voltage).

B. *Short Circuit Protection*

The maximum operating current in SiC power switches is restricted by the deficiencies in the material quality [20].

TABLE II. UVLO THRESHOLD VOLTAGES

V_{DDH} – V_{SSH}	V_{TH}^+	V_{TH}^-
10 V	9.8 V	9.7 V
20 V	18.2V	17.9 V
30 V	26.6 V	26.2 V

Excess current density will place extreme electrical stress on the devices. Therefore, SiC power switches are normally operated at only tens of amperes. A short circuit protection scheme is necessary to prevent the power switch from exceeding its maximum current ratings.

Short circuit faults fall into two, general categories: fault under load (FUL) and hard switch fault (HSF) [21]. The FUL results from a short circuit at the load during the device's "on" state operation. When turning "on", the drain voltage is increased rapidly. This large dV/dt induces a transient current, i_{dg}, through the parasitic Miller capacitance, C_{DG}. As i_{dg} flows back to the driver circuit through the gate resistor Rg, the gate voltage is pulled up immediately. Inevitably, the fault current is increased to an undesired value since the gate voltage is increased.

Hard switch fault, on the other hand, stems from the short circuit formed at the load as the power switch turns "on". A large dV/dt is not induced upon switching, since the voltage across the device is constant. However, due to the large drain voltage, the load current (and resultant device power dissipation) is beyond its limit during the "on" state.

Two short circuit protection (SCP) schemes, resistor sensing protection and de-saturation protection, have been implemented on-chip to protect the power switches working at high temperatures.

The first protection scheme is a technique that uses a sense resistor connected in series to the source of the SiC switch. The block diagram, shown in Fig. 9, consists of a voltage reference, a rail-to-rail comparator, an output buffer, and an off-chip resistor. The off-chip resistor is to convert the fault current into a voltage. This resistor is implemented off-chip since its value is selected based on the fault current of a specific power switch. Moreover, this resistor is typically exposed to a high current, which is unrealistic to implement on chip. The on-chip block of the short circuit protection employs a rail-to-rail comparator to detect the input voltage if it is larger than the reference voltage. This comparator is capable of discriminating mV-level signals and is designed with hysteresis for rejecting small variations at the input [12]. The output buffer is powered by a 5-V digital supply and is used to output digital fault signals.

The circuit works as follows: once the current through the power switch exceeds a certain fault level, (i.e. providing 400 mV across the sense resistor), the comparator will quickly detect a fault and send a 5-V digital signal to the output buffer. The buffer with built-in delay network is able to distinguish the fault signal from any nuisance current. Typically, current surges less than several microseconds will be filtered by the R-C delay in the buffer. If the current surge remains for more than several microseconds, a short circuit fault is identified by the output buffer. A fault signal is then triggered. Thus, the gate driver will turn the power switch "off" to protect it from further damage.

The other short circuit protection scheme, "de-saturation protection," is first proposed in [21] and is widely used in protection circuits for power switches. This SCP scheme utilizes a sense diode to detect any undesired voltage at the drain terminal. This undesired drain voltage is typically caused by a short circuit fault, as discussed previously. The detailed circuit block is shown in Fig. 10.

Under normal circumstances, the power switch is turned on by the gate driver, and diodes D1 and D2 become forward biased. The node voltage V_b and V_a can be expressed as in Eq. (1) and (2),

$$V_b = V_{ds} + V_{diode} \tag{1}$$

$$V_a = V_{ds} + V_{diode} \tag{2}$$

where V_{diode} is the anode-to-cathode, forward-bias voltage for diodes D1 and D2, and V_{ds} is the voltage drop across the power switch. Thus, we can derive Eq. (3) and (4):

$$V_{c1} = \frac{120k\Omega}{120k\Omega+380k\Omega} \cdot (V_b - V_{ds}) \tag{3}$$

$$V_{c2} = \frac{120k\Omega}{120k\Omega+780k\Omega} \cdot (V_a - V_{ds}) \tag{4}$$

In normal working condition, V_{c1} and V_{c2} are guaranteed to be less than V_{ref}, thus no fault signal will be sent to the gate driver. However, in the event of an overcurrent, V_b increases with V_{ds}. As a result, capacitor C1 is charged to a higher voltage. As soon as V_{c1} reaches V_{ref}, a fault is triggered to shut down the gate driver circuit. The power switch will remain "off" until the load current returns to normal. This overcurrent fault does not cause permanent damage to the power switch and is mostly caused by an

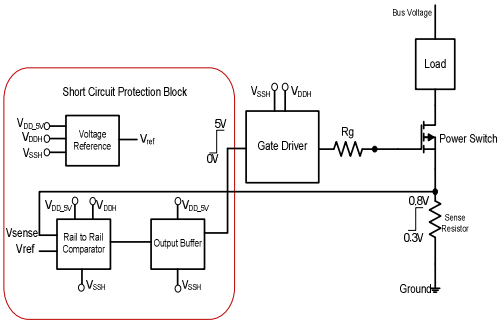

Fig. 9. Resistor sensing short circuit protection circuit.

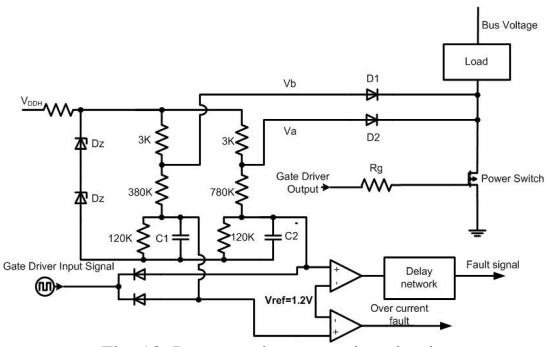

Fig. 10. De-saturation protection circuit.

unstable working environment, such as overshoot of the system power supply or an unstable gate driver output voltage.

On the other hand, when a short circuit occurs, i.e. the load current becomes much larger than the overcurrent threshold and lasts more than several microseconds, V_{ds} increases to an even a higher level. The top comparator is triggered by V_{C2}, and a short circuit fault signal is triggered. Under this scenario, the high load current will impose mechanical and thermal stress on the power switch, severely degrading its reliability and lifetime. Therefore, the power switch will be shut "off" until the fault is removed externally.

Both the resistor sensing protection and the de-saturation protection have been widely used. However, it is not practical to implement one de-saturation protection circuit for both normally "on" and normally "off" power devices without additional power supplies. This is because this circuit always requires one positive power supply, i.e. more than 10 V, to maintain the sense diode in the forward bias region and detect different fault drain voltages when the power switch is "on".

C. *Gate Current Monitoring*

In general, there are two types of gate current faults [22]: (1) a gate short circuit condition and (2) a gate dielectric wear-out condition. A gate short circuit condition is usually caused by a faulty electrical connection or a damaged power device; this condition will result in large, continuous current flowing through the gate of the power device from the drain or to the source. Gate wear-out conditions mostly stem from gate dielectric degradation. This degradation will increase the time required for the driver circuit to charge and discharge the gate of the power switch.

A gate current monitoring circuit (Fig. 11) is used to detect these fault conditions by monitoring the transient current flowing through the sense resistor (R_{sense1} and R_{sense2} in Fig. 11) during the switching operation of the power switch.

The gate current induced voltage across the sense resistor is fed to a differential amplifier with near unity gain.

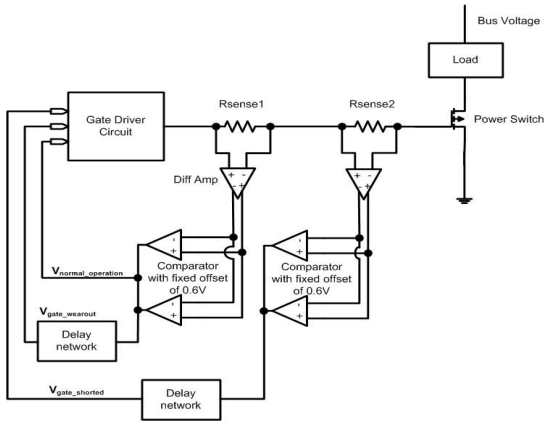

Fig. 11. Gate current monitoring circuit.

This buffer converts the sensed differential signal, superimposed upon a rapidly changing common mode signal (gate signal), into a V_{SS}-referenced signal. The V_{SS}-referenced signal is input to a comparator having 0.6-V offset. Thus, the comparator will detect any fault signals larger than 0.6 V. Two comparators are required since the gate current is bidirectional.

Two similar circuits are implemented here because gate wear-out and gate shorted conditions have different fault current levels, thus different sense resistor values are needed to accommodate the different triggering current levels.

IV. Measurement Results

Several measurement results are presented for the core (3G) gate driver. For the first measurement, an on-chip current limiting resistor, R_G, was connected in series with an external 10-nF capacitive load to model the load presented by a power switch. Fig. 12 shows the 30-V_{p-p} (−15 V to +15 V), 20-kHz gate pulse signal generated by the chip at an ambient temperature of 200°C with a nominal R_G value of 3.4 Ω. At 200°C, the peak sourcing and sinking currents were measured to be 2.5 A and 2.2 A, respectively.

A SiC power MOSFET (1200-V, 10-A) prototype device was also tested with the 3G gate driver, Fig. 13. The SiC MOSFET was arranged in a common-source configuration with an 80-Ω, 250-W load resistor in series with the drain terminal. The drain voltage of the MOSFET was set at 560 V using a 600-V, 16-A DC power supply. A 20-V_{p-p} (+15 V to −5 V) drive signal was applied to the gate terminal of the SiC MOSFET through the 3.4-Ω, on-chip current-limiting resistor (R_G). The switching frequency was 20 kHz with a

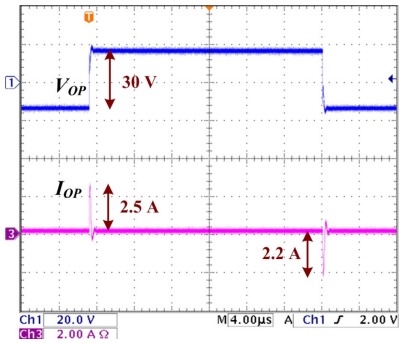

Fig. 12. R-C load test results at 200°C with R_G =3.4 Ω and CLoad =10 nF.

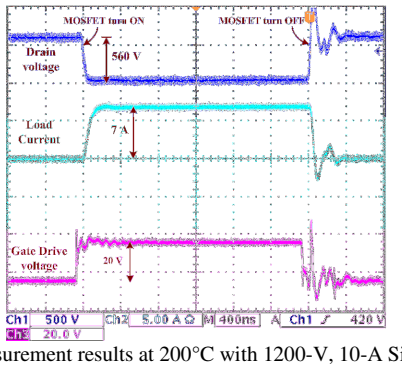

Fig. 13. Measurement results at 200°C with 1200-V, 10-A SiC MOSFET.

duty cycle of 5%. The chip was tested from room temperature up to 200ºC ambient.

The gate driver IC was also tested with a normally-"on" SiC JFET (1200-V, 50-A) power module. The gate driver circuit was biased to generate an 8-V_{p-p} (−5 V to 3 V) gate signal to control the JFET module that was connected to a 560-V rail voltage through an 80-Ω load resistor. Fig. 14 shows the test result at 200°C ambient temperature with a 1 kHz switching frequency.

The 3G gate driver featured a 5-V regulator similar to the 4G 5-V regulator; however, the 3G 5-V regulator requires an external output capacitor to provide a stable output voltage for gate driver circuits. Fig. 15 shows the 3G regulator temperature characteristic test data.

The low temperature dependence of the 3G 5-V regulator is maintained in the 4G 5-V regulator design, while allowing the 4G 5-V regulator to make substantial design improvements. The 70-mV offset voltage (due to input bias current) of the 3G 5-V regulator is reduced in the 4G 5-V regulator design by reducing the resistance in the base of the differential input pair of the error amplifier. The 4G 5-V regulator implements a class-AB output stage as opposed to the class-A output stage of the 3G 5-V regulator. This modification reduces the output impedance of the regulator and allows the regulator to sink and source current effectively.

The resistor sensing short circuit protection circuit has been tested with the gate driver core circuitry with a gate resistor of 3.4 Ω and load capacitor of 10 nF. Fig. 16 and Fig. 17 show the transient response of the circuit at both room temperature and at 200˚C ambient with a power supply range from −15 V to +15 V. The gate driver has been

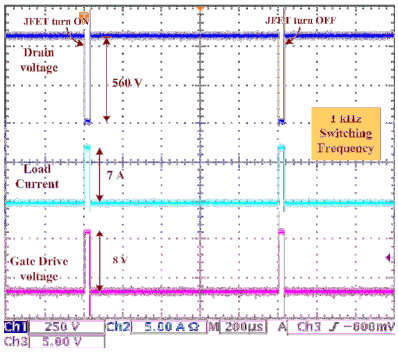

Fig. 14. SiC normally ON JFET module (1200 V, 50 A) test results at 200°C driving and 1 kHz switching frequency.

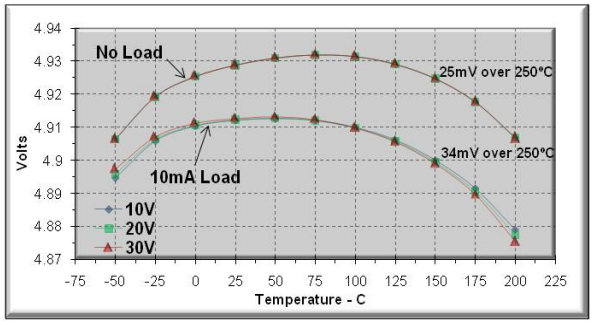

Fig. 15. 3G 5-V Regulator temperature characteristic.

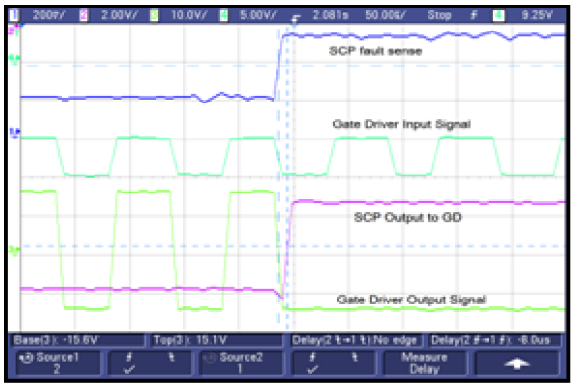

Fig. 16. SCP tested with gate driver circuit and 10 nF load capacitor (room temperature).

Fig. 17. SCP tested with gate driver circuit and 10 nF load capacitor (200˚C).

successfully turned "off" within 8 microseconds of fault current detection. Other power supply arrangements (V_{SSH} = −15 V, V_{DDH} = 5 V and V_{SSH} = −3 V, V_{DDH} = 7 V) have been successfully tested to verify the protection circuitry functionality for normally "on" and normally "off" power devices.

V. Conclusions

In this paper, a high-temperature, high-voltage SOI-based gate driver has been presented. A prototype gate driver has been successfully tested up to 200°C ambient temperature without any active or passive cooling mechanisms. This prototype has successfully generated a 30-V_{p-p} gate drive voltage with sourcing and sinking currents > 2.2 A at 200˚C. The gate driver has also been demonstrated driving SiC MOSFETs and JETs at 200˚C ambient temperature. Although this gate driver has been designed for automotive applications, it could easily be applied to numerous harsh environment applications, in which conventional bulk silicon-based devices could not deliver an efficient, cost-effective solution. For integration of wide-bandgap, power devices into power electronic modules, SOI-based integrated circuits capable of working above 150°C ambient temperature are needed to interface them with control circuitry. The high-temperature, high-voltage gate driver integrated circuit presented in this paper is part of an on-

going research effort to design an integrated smart-power module.

REFERENCES

[1] R. W. Johnson, J. L. Evans, P. Jacobsen, and R. Thompson, "High-temperature automotive electronics," in *Proc. Int. Conf. Advanced Packaging and Systems,* Reno, NV, 10-13 March, 2002, pp. 77-87.

[2] C. M. Carlin and J. K. Ray, "The requirement for high-temperature electronics in a future high speed civil transport (HSCT)," in *Proc. 2nd Int. High-Temperature Electronics Conf.,* Charlotte, NC, June 1994, pp. I19-I.26.

[3] M. Huque, R. Vijayaraghavan, M. Zhang, B. Blalock, L. Tolbert and S. Islam, "An SOI-based high-voltage, high-temperature gate-driver for SiC FET," *Proceedings of the 38th IEEE Power Electronics Specialist Conference (PESC 07)*, Orlando, Florida, USA, 17-21 June 2007, pp. 1491-1495.

[4] M. A Huque, B. J. Blalock, C. Su, R. Vijayaraghavan, S. K. Islam, and L. M. Tolbert, "SOI based integrated circuits for high-temperature applications," in *Proc. of International Conference and Exhibition on High Electronics* (HiTEC 2008), Albuquerque, New Mexico, USA, May 13 - 15, 2008.

[5] M. A. Huque, L. M. Tolbert, B. J. Blalock, and S. K. Islam, "A high-temperature, high-voltage SOI gate driver IC with high output current and on-chip low-power temperature sensor," *42nd International Symposium on Microelectronics* (IMAPS 2009), San Jose, CA, Nov. 1-5.

[6] K. Mino, S. Herold, and J. W. Kolar, "A gate drive circuit for Silicon Carbide JFET," *Proceedings of the 29th Annual Conference of the IEEE Industrial Electronics Society*, Roanoke (VA), USA, 2-6 November 2003, pp. 1162-1166.

[7] M. L. Heldwein and J. W. Kolar, "A novel SiC JFET gate drive circuit for sparse matrix converter applications," *IEEE Applied Power Electronics Conference and Exposition*, 2004, pp. 116-121.

[8] A. Melkonyan, I. Hofsajer, S. Round, and J. Kolar, "A simple, low cost gate drive method for practical use of SiC JFETs in SMPS," *Proceedings of the 11th European Conference on Power Electronics and Applications*, Dresden, Germany, 12-14 September 2005, pp. P1-P6.

[9] S. Round, J. Kolar, I. Hofsajer, and P. Friedrichs, "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter," *IEEE Industry Applications Conference*, 2-6 October 2005, pp. 410 – 416.

[10] F. Li, D. Giannopoulos, and I. Wacyk, "A low loss high-frequency half-bridge driver with integrated power devices using EZ-HV SOI technology," *IEEE Applied Power Electronics Conference and Exposition*, 10-14 March 2002, pp. 1127 – 1132.

[11] S. Park and T. M. Jahns, "A self-boost charge pump topology for a gate drive high-side power supply," *IEEE Transactions on Power Electronics*, vol. 20, no. 2, March 2005, pp. 300-307.

[12] R. Jacob. Baker, "*CMOS: Circuit Design, Layout, and Simulation, Revised Second Edition*," Wiley-IEEE, 2008, pp. 812-819, 910.

[13] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits 4th Edition*, John Wiley & Sons, Inc., 2001.

[14] F. Shoucair, "Design considerations in high-temperature analog CMOS integrated circuits," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 9, no. 3, Sept. 1986.

[15] P. Songmalai, T. Phetchakul, W. Pengchan, E. Ratanaudomphisut and J. Supadech, "Study on temperature effect on p-n and Zener junction for PTAT temperature sensor," *International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, ECTI-CON 2008. 5th, May 2008.

[16] M. U. Abbasi, T. A. Abbasi, M. S. Abbasi, and A. Hasan, "An improved fast transient response low drop-out voltage regulator," *IEEE International Symposium on Circuits and Systems,* May 2009, pp. 808-811.

[17] M. A. Huque, S. K. Islam, B. J. Blalock, and L. M. Tolbert, "Diode leakage current based low power, on-chip high temperature sensor circuit*," Proc. of 18th Annual Symposium on Micro- and Nano-technologies for Electronics, Photonics, Biosensors, and Alternate Energy Sources* (CMOC 2009), Yale University, New Haven, Connecticut, March 11, 2009, pp. 57-58.

[18] M. R. Hoque and S. S. Ang, "A CMOS under-voltage lockout circuit," *World Congress and Computer Science*, 2008.

[19] Z. Fanglan, F. Quanyuan, and G. Kunlin, "An under-voltage lockout of hysteretic threshold of zero temperature coefficients," *Microwave Conference Proceedings*, vol. 2, no. 3, pp. 4 – 7, Dec 2005.

[20] P.G. Neudeck, "SiC Technology," *The VLSI Handbook*, pp. 5.1-5.34.

[21] R.S. Chokhawala, J. Catt, L. Kiraly, "A discussion on IGBT short-circuit behavior and fault protection schemes," *IEEE Transactions on Industry Applications*, vol. 31, Issue. 2, 1995, pp. 256 – 263.

[22] C. Lihua, F. Z. Peng, and C. Dong, "A smart gate drive with self-diagnosis for power MOSFETs and IGBTs," *IEEE Applied Power Electronics Conference and Exposition*, Feb. 2008, pp.1602-1607.