Temperature Dependent Pspice Model of Silicon Carbide Power MOSFET

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Abstract— **This paper provides a behavioral model in Pspice for a silicon carbide (SiC) power MOSFET rated at 1200 V / 30 A for a wide temperature range. The Pspice model was built using device parameters extracted through experiment. The static and dynamic behavior of the SiC power MOSFET is simulated and compared to the measured data to show the accuracy of the Pspice model. The temperature dependent behavior was simulated and analyzed. Also, the effect of the parasitics of the circuit on switching behavior was simulated and discussed.**

I. INTRODUCTION

Silicon (Si) power MOSFETs have been widely used in high frequency power converters because of their fast switching capability [1]. However, because of material properties, Si MOSFETs are limited to relatively low power applications. SiC power MOSFETs have become competitive because of its superior material properties. SiC power MOSFETs have higher blocking voltage, higher operational temperature and even higher switching frequency, and will compete with Si IGBTs in applications that can take full advantage of its inherent superior properties [2-4].

Device modeling is necessary to fully estimate the behavior of the device in power converters, like the transient switching times, overshoot current and voltage values, and switching losses. Different MOSFET models have been developed to estimate their performance in power converters [5-8]. Because of less application knowledge of SiC power MOSFETs, accurate modeling is even more significant to help people estimate their performance and further properly design power converters to take full advantage of SiC power MOSFETs.

This paper presents a temperature dependent behavioral Pspice model of a SiC power MOSFET rated at 1200 V / 30 A. The modeling procedure is discussed and the comparisons between experiments and simulations for the static and dynamic characteristics are presented. Then, the temperature influence on switching transients has been analyzed in both experiment and simulation. Finally, the effect of different parasitics in the circuit is shown in simulation.

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II. STATIC CHARACTERISTIC AND MODELING

A. MOSFET Modeling Method

Fig. 1 shows the equivalent circuit of a power MOSFET used in this paper. It includes an ideal MOSFET which is described as a voltage controlled current source, three junction capacitors that vary with voltage, a reverse body diode and other parasitics.

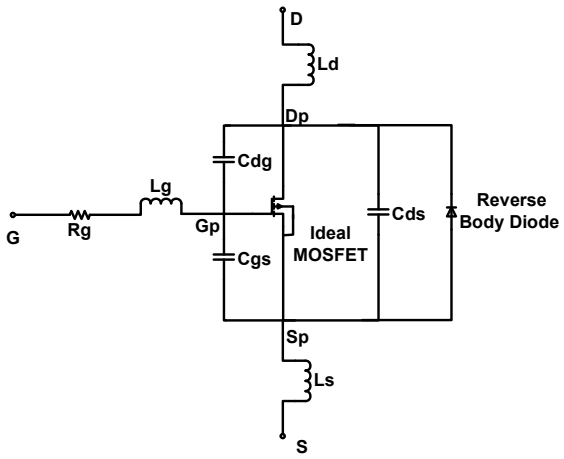

Fig. 1. Equivalent circuit model of MOSFET.

Normally, the following equations can be used to represent the MOSFET model. In these equations, C_{OX} is the capacitance of the oxide layer. μ_n is the charge-carrier effective mobility, λ is the channel-length modulation parameter, W is the gate width, and L is the gate length. Eq. (2) is the current in the linear region where $V_{DS} < V_{DSsat}$ and (3) is the saturation current where $V_{DS} \geq V_{DSsat}$.

$$V_{DSsat} = V_{GS} - V_{th} \quad (1)$$

$$I_D = \mu_n C_{OX} \frac{W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right) \quad (2)$$

$$I_D = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda(V_{DS} - V_{DSsat})) \quad (3)$$

Based on this method, the transfer characteristics have been simulated and compared to the measured data shown in Fig. 2. However, the differences between simulation and experiment are not negligible. Therefore, the n-th power law

MOSFET model proposed in [9] was implemented in modeling this SiC power MOSFET. This model offers more accuracy and flexibility in defining the saturation voltage. This method does not require any additional experiment and parameter extraction. The following discussion is based on this model.

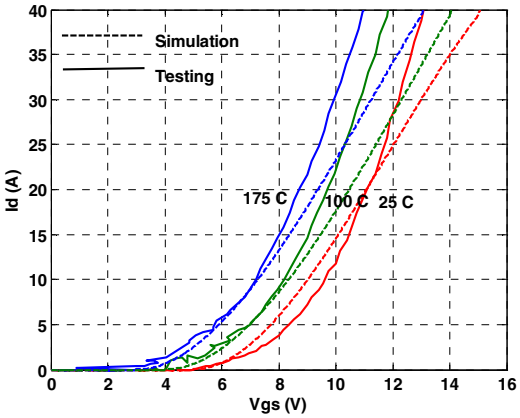

Fig. 2. Transfer characteristic comparison between experiment and simulation with model using eqs. (1)-(3).

The following equations are used to describe the voltage controlled current source in this model [5, 9]. I_{Dsat} and V_{DSsat} are the saturation current and voltage. Eq. (6) describes the linear current, and (7) is for the saturation current.

$$V_{DSsat} = K(V_{GS} - V_{th})^m \quad (4)$$

$$I_{Dsat} = B(V_{GS} - V_{th})^n \quad (5)$$

$$I_D = I_{Dsat}(1 + \lambda V_{DS})\left(2 - \frac{V_{DS}}{V_{DSsat}}\right)\frac{V_{DS}}{V_{DSsat}} \quad (6)$$

$$I_D = I_{Dsat}(1 + \lambda V_{DS}) \quad (7)$$

The value of threshold voltage V_{th} was directly from measured transfer data. The values of *B, K, m, n* and λ in the model were calculated from the measured forward curves of the MOSFET [9]. All the parameters are temperature dependent in this model. Because of difference in value of these parameters at lower and higher gate voltage, a piece-wise linear function was implemented to describe them over gate voltage to improve the accuracy of this model.

B. Static Characteristic Comparison

Based on the MOSFET model developed with the method discussed above, the forward and transfer characteristics have been simulated in Pspice and compared to the measured data at multiple temperatures. Also, the on-state resistance and threshold voltage have been calculated in simulation and experiment correspondingly and compared with each other.

Figs. 3-5 are the forward characteristic comparison at different temperatures and different gate voltages (curves from top to bottom, V_{gs} equals to 20 V, 18 V and 16 V, respectively). The conduction current is up to 40 A in the comparison considering overshoot during switching transient. As shown in the figures, the simulation results have good agreement with the experimental results at different operating conditions.

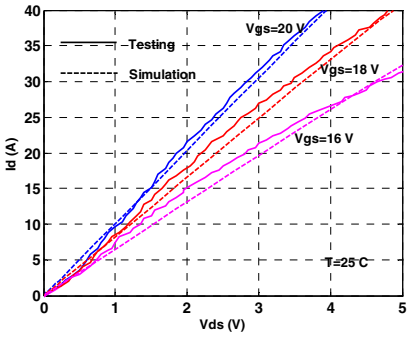

Fig. 3. Forward characteristic comparison between simulation and experiment of 1200 V / 30 A SiC MOSFET at 25 °C .

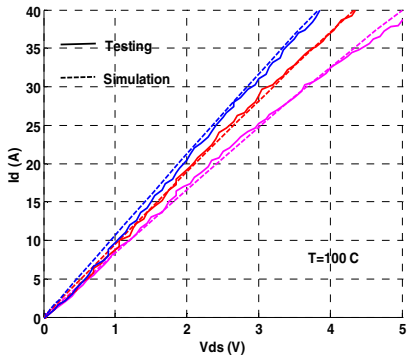

Fig. 4. Forward characteristic comparison between simulation and experiment of 1200 V / 30 A SiC MOSFET at 100 °C.

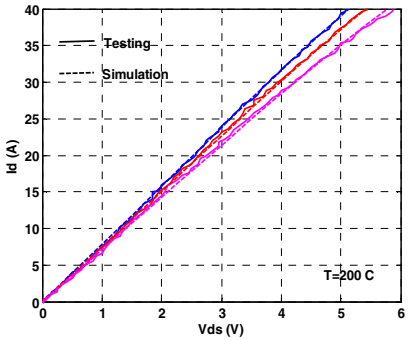

Fig. 5. Forward characteristic comparison between simulation and experiment of 1200 V / 30 A SiC MOSFET at 200 °C.

The on-state resistance can be calculated from the forward curves. Fig. 6 is the comparison between simulated and measured results. The on-state resistance was calculated when the current was 10 A to ensure the MOSFET was in linear region for both simulation and experiment. As shown in Fig. 6, around 50 °C, the on-state resistance from the experiment showed a negative temperature coefficient. This can be explained as follows. The resistance of a power MOSFET mainly comes from three parts: channel resistance R_{CH}, JFET region resistance R_{JFET}, and drift layer resistance R_{DRIFT} [10]. R_{CH} has a negative temperature coefficient, while the other two components have a positive temperature coefficient. Around 50°C, the change of R_{CH} is dominant which makes the whole resistance decrease with temperature increasing. At higher temperature, R_{JFET} and R_{DRIFT} change faster than R_{CH} which leads to positive temperature coefficient [10-12].

However, the simulation did not show much of this effect because the coefficients in the modeling equations were calculated at individual temperature points and later modeled as a continuous function by curve fitting, during which the values around 50°C lost some characteristics to fit the whole curve.

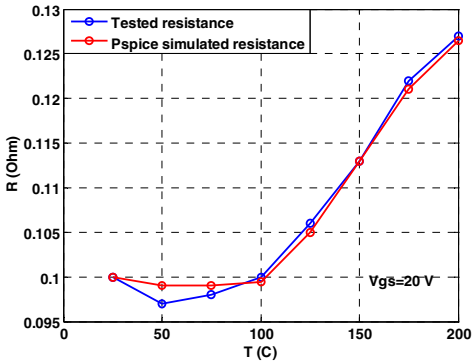

Fig. 6. On-state resistance comparison between simulation and experiment of 1200 V / 30 A SiC MOSFET.

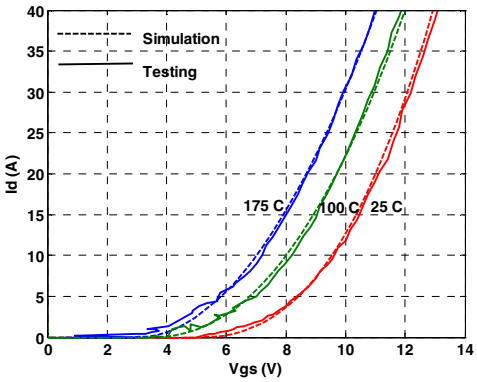

Fig. 7. Transfer characteristic comparison between simulation and experiment of a 1200 V / 30 A SiC MOSFET.

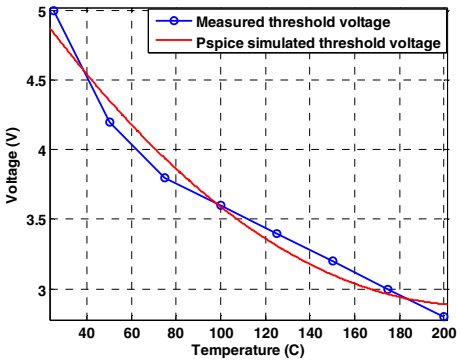

Fig. 8. Threshold voltage comparison between simulation and experiment of 1200 V / 30 A SiC MOSFET.

Simulated transfer curves have also been compared to experimental results at different temperatures in Fig. 7. Clearly, this model gives more satisfactory results compared to the model built with (1) to (3) shown in Fig. 2. The transconductance can be calculated from the transfer curve, which increases with temperature, from 7 S at 25°C to 9 S at 200°C. All of the values were calculated under the same condition. Fig. 8 is the comparison of threshold voltage which decreases with increasing temperature.

III. Dynamic Characteristic and Modeling

A. Junction Capacitance Extraction

Junction capacitances govern the switching behavior of the MOSFET during transients; therefore, accurate extraction is necessary for a good match of transient behavior between simulation and experiment. Three junction capacitances have been extracted using an impedance analyzer. Schematic of the fixture and extraction method can be found in [11,13].

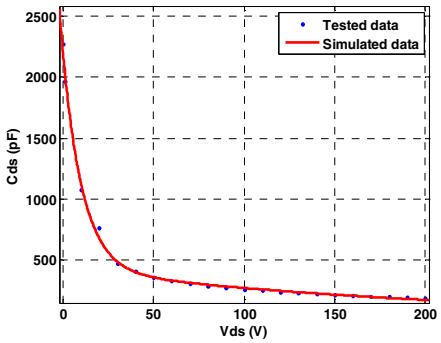

Fig. 9. C_{ds} versus V_{ds} for 1200 V / 30 A SiC MOSFET.

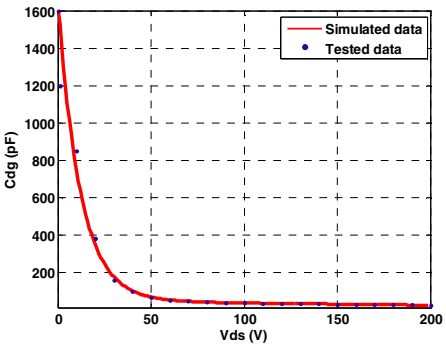

Fig. 10. C_{dg} versus V_{ds} for 1200 V / 30 A SiC MOSFET.

Figs. 9 and 10 are the comparison between the modeled and measured drain to source and drain to gate capacitances with V_{ds} varying from 0 V to 200 V. The curves were obtained by curve fitting the measured capacitances over voltages. The gate to source capacitance was also extracted, and the value changed from 2.16 nF to 3.3 nF when V_{gs} changed from 0 V to 5 V and kept at 3.3 nF at higher gate voltage.

B. Dynamic Characteristics Comparison

Dynamic characteristics of the SiC power MOSFET were tested in a double pulse tester (DPT) with the schematic of the test circuit shown in Fig. 11. The parasitics included during simulation were also indicated in Fig. 11. Fig. 12 is the experimental setup for the double pulse testing. The free-wheeling diode was a SiC junction barrier Schottky (JBS) diode rated at 600 V / 50 A whose junction capacitance was extracted using the impedance analyzer. An IXDD 414 chip was used as the gate driver. The gate resistors R_{g1} and R_{g2}

were 15 Ω and 3 Ω, respectively, and the gate capacitor C_1 was 30 nF. The combination of R_{g2} and C_1 was used to reduce transient time and increase switching speed. The gate voltage swing was 0 V to 20 V. V_{ds} was measured by a TEK differential probe P5205 with 100 MHz, and I_d was measured by a Pearson current probe with 2877 MHZ range bandwidth.

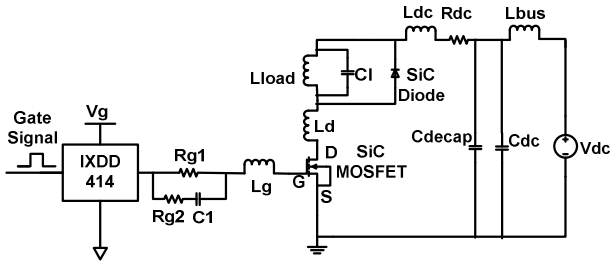

Fig. 11. Schematic of double pulse tester with parasitics.

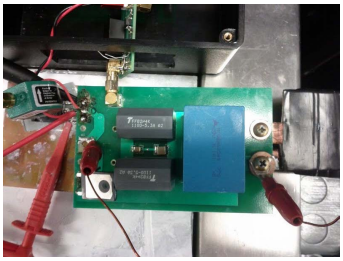

Fig. 12. Experiment setup of DPT for 1200 V / 30 A.

A similar circuit has been built in Pspice using the same diode model. The gate driver was not included in Pspice to simplify the simulation. Instead, an ideal voltage source with 20 ns transient time was connected to the gate of the MOSFET through the same parallel structure of resistors and capacitor shown in Fig. 11. The parasitic capacitance associated with the load inductor was extracted with value of 201 pF. The internal gate resistance is 4.7 Ω obtained through extraction.

L_{bus} is the inductance coming from the wire connected to the power supply, and its influence could be compensated by the decoupling capacitors shown in Fig. 11. L_{dc} is the inductance introduced to the circuit after the decoupling capacitors, and R_{dc} is the parasitic resistance. In the Pspice simulation, R_{dc} was also used for damping oscillation. L_d is the external drain inductance between the MOSFET drain and the free-wheeling diode, which came from both the circuit board and the wire used to measure the drain current. L_g is the external parasitic gate inductance in series with the gate resistors. In simulation, the values of the parasitics used were as follows: L_{dc} was 100 nH, external drain inductance L_d was 100 nH, external gate inductance L_g was 10 nH, and parasitic resistance R_{dc} was 9 Ω. R_{dc} was much larger than the actual value in the circuit, which is mainly for oscillation damping. The small time step was used for convergence purpose in Pspice, but it created unrealistic oscillations, especially for the current. It has been proved by simulation that this resistance value did not affect transient time.

The test circuit was not optimized to keep the effect of parasitics to a minimum. This was done intentionally to introduce parasitics for modeling purpose.

The comparison between simulation and experiment was performed at 400 V and 15 A under room temperature. Figs. 13 and 14 are the gate voltage comparison. Experimental turn on gate voltage had more oscillation compared to simulation waveform. Simulated turn off waveforms matched better with the experimental waveform. Figs. 15 and 16 are comparison of the turn on and turn off drain current and drain to source voltage between experiment and simulation. As seen from these figures, the simulation gives fairly accurate results.

However, turn on transient voltage has some mismatch between testing and simulation. This is because the gate voltage of experiment was not as stable as the simulation.

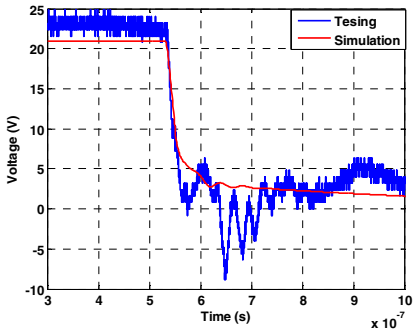

Fig. 13. Gate voltage comparison during turn off between simulation and experiment of 1200 V / 30 A SiC MOSFET.

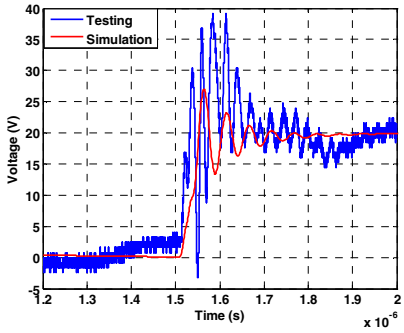

Fig. 14. Gate voltage comparison during turn on between simulation and experiment of 1200 V / 30 A SiC MOSFET.

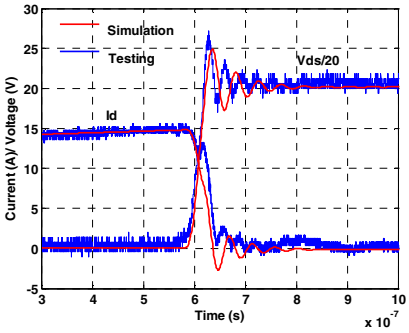

Fig. 15. Comparison of turn off waveforms between simulation and experiment of 1200 V / 30 A SiC MOSFET.

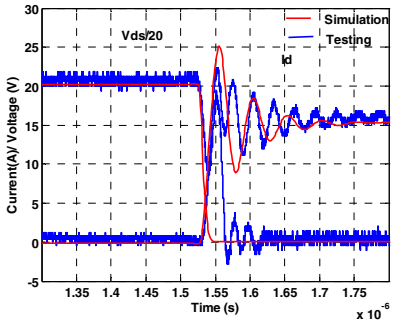

Fig. 16. Comparison of turn on waveforms between simulation and experiment of 1200 V / 30 A SiC MOSFET.

C. *Temperature Dependency Analysis*

Switching behavior of the SiC MOSFET was tested over temperature to show the temperature dependency. Transient comparisons between experiment and simulation were presented at 25°C and 175°C. To observe more clearly the changes associated with temperature, experiment and simulation waveforms are shown in different figures as follows.

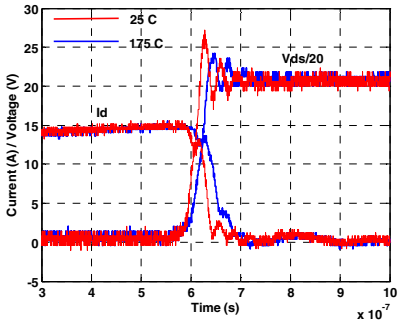

Fig. 17. Tested turn off waveforms at 25°C and 175°C of 1200 V / 30 A SiC MOSFET.

Shown in Fig. 17, the current turn off speed was slower at higher temperature. This explains the reduction of turn off voltage overshoot as the overshoot comes from the voltage across the loop parasitic inductance which is a function of the current slope. In simulation, similar phenomenon appears as shown in Fig. 18. Turn-on waveforms are almost unchanged except for a slight delay of the point when current started to increase at 25°C, which is because the threshold voltage is larger in both simulation and experiment as shown in Figs. 19 and 20.

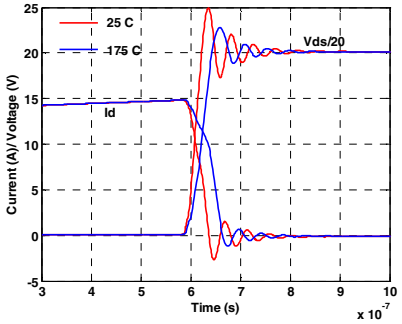

Fig. 18. Simulated turn off waveforms at 25 °C and 175 °C of 1200 V / 30 A SiC MOSFET.

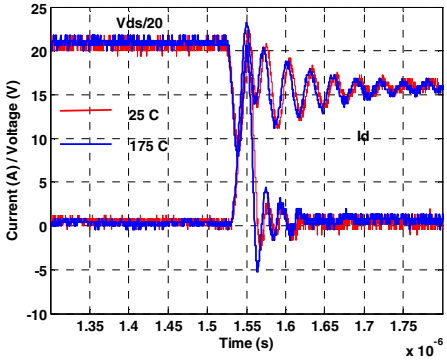

Fig. 19. Tested turn on waveforms at 25°C and 175°C of 1200 V / 30 A SiC MOSFET.

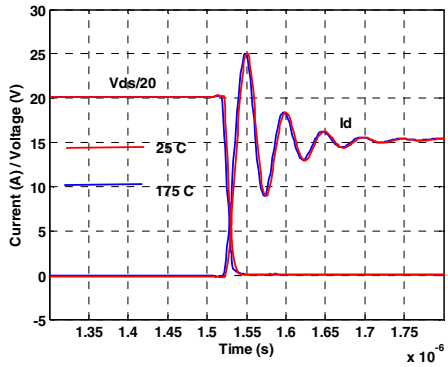

Fig. 20. Simulated turn on waveforms at 25°C and 175°C of 1200 V / 30 A SiC MOSFET.

IV. Analysis of Parasitics in Circuit

The parasitics, like DC loop inductance and resistance, though undesirable, cannot be eliminated completely from the circuit and will affect the performance of the device and the converter. The influence of the parasitics on the switching behavior has been studied in [14-16]. Based on the MOSFET model and the DPT circuit in Pspice, the impacts of some parasitics shown in Fig. 11 have been studied and analyzed in this section.

A. *DC Loop Inductance*

The DC loop inductance is the sum of L_{dc} and L_d in Fig. 11. Figs. 21 and 22 show the influence of this inductance on the MOSFET's turn on and turn off behavior. All the other elements in the circuit were kept the same except for the parasitic inductance and the simulated values were shown in Figs. 21 and 22. The value of the parasitic inductance greatly affects the overshoot value of voltage during turn off. This is because during turn off, the MOSFET not only withstands the DC voltage, but also the voltage drop across the inductor. Furthermore, because the SiC power MOSFET is widely used for high switching frequency application, the parasitic loop inductance becomes more critical. When all the DC loop inductance is eliminated, the voltage does not experience overshoot during turn off, the current rise time becomes much smaller during turn on, and oscillation in current and voltage disappears. As expected, the value of the loop inductance would also affect the current and voltage oscillation frequency.

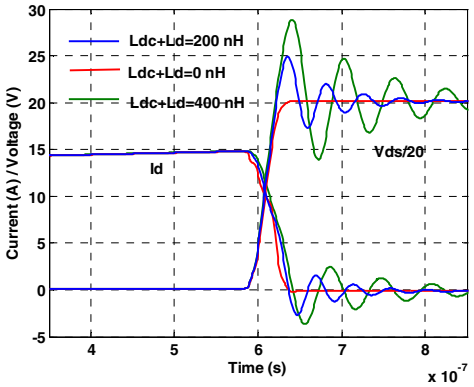

Fig. 21. Simulation comparison of different loop inductance during turn off of 1200 V / 30 A SiC MOSFET.

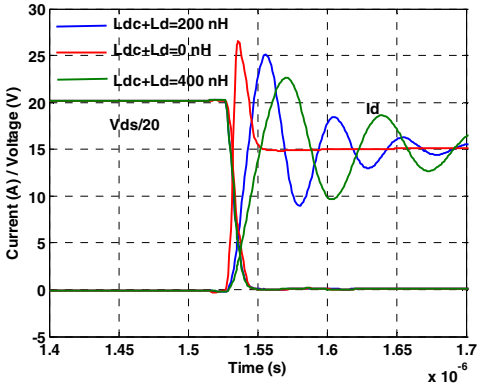

Fig. 22. Simulation comparison of different loop inductance during turn on of 1200 V / 30 A SiC MOSFET.

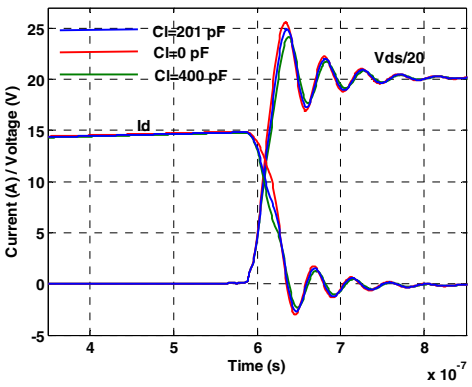

Fig. 23. Simulation comparison of parasitic capacitance during turn off of 1200 V / 30 A SiC MOSFET.

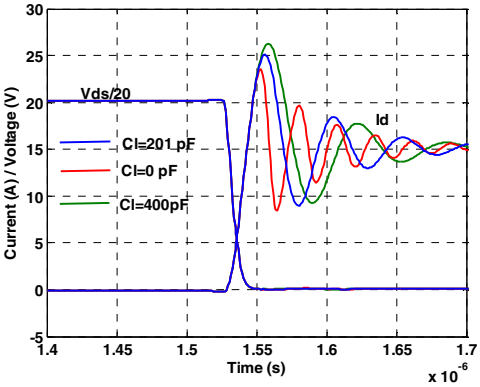

Fig. 24. Simulation comparison of parasitic capacitance during turn on of 1200 V / 30 A SiC MOSFET.

B. Inductor Parasitic Capacitance

Figs. 23 and 24 are the comparison of turn on and turn off transients with different values of parasitic capacitance associated with the load inductor. This parasitic capacitance is in parallel with the free-wheeling diode junction capacitance; therefore, during every turn-on and turn-off transient, it will be charged and discharged like the diode junction capacitor.

During turn off, the voltage overshoot value reduces when parasitic capacitance becomes larger as the current becomes slower. During the MOSFET turn on process, this parasitic capacitance is also commutated with the MOSFET. This explains why the larger this capacitance is, the larger the overshoot current is. The turn on voltage is almost unaffected by the parasitic capacitor. Turn on current oscillation frequency changes when the capacitor value changes as expected.

The parasitic capacitance has less impact on the turn off transient than turn on transient, which is because of the diode junction capacitance C_j. The value of C_j increases as the reverse voltage applied across the diode decreases. The parasitic capacitance is much smaller compared to C_j during turn off transient as the voltage across the diode drops to zero, while during turn on transient, the value of these two capacitors are comparable and the change of the parasitic capacitance would be more significant as shown in Fig. 26.

V. CONCLUSION

In this paper, a 1200 V / 30 A SiC power MOSFET has been tested and modeled. The static characteristics, such as the forward and transfer curves, the on-state resistance, threshold voltage, and transconductance, have been extracted and calculated under different temperatures. The temperature dependency of them has also been analyzed. The comparison of static characteristic between Pspice model and measured data show good agreement with each other.

The switching characteristics have been tested on a double pulse tester under multiple conditions. The junction capacitances of the SiC MOSFET and the SiC diode have been extracted using an impedance analyzer. A similar double pulse test circuit with parasitics in consideration has been simulated in Pspice with the MOSFET model, which gave satisfactory results. With both static and switching comparison, the Pspice model has been proved to be valid for predicting the MOSFET performance in power converters. The temperature dependency has also been analyzed and similar phenomenon shown in both experiment and simulation. Furthermore, the influence of the loop inductance and the parasitic capacitance associated with the load inductor has been simulated and studied in Pspice.

ACKNOWLEDGEMENT

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