SiC Based Current Source Rectifier Paralleling and Circulating Current Suppression

Fan Xu, Ben Guo, Zhuxian Xu, Leon M. Tolbert, Fred Wang, Ben J. Blalock
Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT)
Department of Electrical Engineering and Computer Science
The University of Tennessee
Knoxville, TN 37996-2250, USA
fxu6@utk.edu

***Abstract*— This paper develops a liquid cooled high efficiency three-phase current source rectifier (CSR) for data center power supplies based on 400 V_{dc} architecture, using SiC MOSFETs and Schottky diodes. The 98.54% efficiency is achieved at full load. The rectifiers are paralleled to achieve high power ratings and system redundancy. The current balance and hot-swap of paralleled CSRs are realized in simulation using master-slave control. Moreover, an improved modulation scheme through adjustment of the freewheeling state is proposed and verified to effectively suppress the circulating current.**

I. INTRODUCTION

The data and telecommunication centers are major energy consumers, with energy consumption estimated at 40 TWh in 2005 in U. S. alone and 120 TWh worldwide [1], due to the widespread use of information and communication technology equipment. The total electricity bill for operating those servers and associated infrastructure in 2005 was about 2.7 billion dollars and 7.3 billion dollars for the U. S. and the world, respectively [1]. In a typical data center, however, less than half of the power is delivered to the computing load, and the rest of the power is lost in power conversion, distribution, and cooling [2]. Therefore, reduction in electricity consumption in the telecommunication and information industry is an important issue. In recent studies, the 400 V_{dc} power distribution architecture for data center and telecommunication power supply systems, shown in Fig. 1, has been presented to have superior efficiency and reliability compared with the traditional AC distribution architecture [2]-[3].

The three-phase current source rectifier (CSR) with 400 V_{dc} output is well-suited as the front-end rectifier for such a power distribution system, because a boost type rectifier output is too high when connected to the 480 V_{rms} line-to-line grid. Compared to traditional Si devices [4], Silicon Carbide (SiC) power semiconductors have low on-state resistance, fast switching, and provide new opportunities to implement ultra-high efficiency power converters [5]-[6]. A 5 kW three-phase CSR based on SiC Schottky diodes and Si MOSFETs is presented in [5], and the full load efficiency of 98.8% was achieved.

The paralleling connection of converters is widely used in power supply systems to achieve high power ratings, system redundancy, and easy implementation of converter power management. The existing techniques of current distribution and hot-swap for paralleled converters in power supplies are all based on voltage source converters [7]-[12].

In direct connected paralleling converter systems, circulating current (I_C) will be generated that will increase power loss, saturate inductors, overstress or even damage power devices [13]. The active control method is preferred to reduce circulating current without using passive components and has been proposed for paralleled three-phase voltage source converters [13]-[14]. For current source converters, some publications develop multiple space vector controls to solve DC current unbalance caused by circulating current [15]-[16]. The circulating current has been reduced by improving the modulation scheme for interleaved CSRs without freewheeling diodes in [17]-[18], which have different modulation than the CSRs with freewheeling diodes that are presented in this paper.

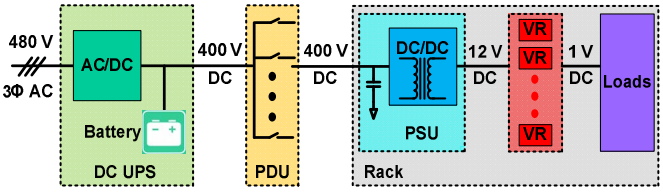


Fig. 1. 400 V_{dc} power delivery architecture for data center power supply systems [2].

This paper presents a high efficiency three-phase current source rectifier using SiC MOSFETs and Schottky diodes for 400 V_{dc} data center power supplies. The test results demonstrate good performance and high efficiency. The rectifiers are paralleled to achieve high output power. The current balance and hot-swap of paralleled CSRs are simulated. Moreover, an improved modulation scheme based on switching loss optimized (SLO) modulation is proposed that effectively suppresses the circulating current in a paralleled CSRs system.

II. SiC Based Hihg Efficiency Current Source Rectifier

A. Converter Topology and Specifications

The three-phase CSR, developed as the front-end rectifier of data center power supplies, operates at a normal power rating of 7.5 kW with a three-phase 480 V_{rms} line-to-line input voltage and 400 V_{dc} output voltage, which are dictated by the architecture of the power delivery system in Fig. 1.

Fig. 2 shows the topology of three-phase CSR with input and output filters. Table I lists specifications of this converter. The front-end rectifier needs to provide sinusoidal input current and high input power factor.

TABLE I. THREE-PHASE BUCK RECTIFIER SPECIFICATIONS

Power Rating	7.5 kW
Input Voltage	Three-phase line-to-line 480 $V_{ac,rms}$
Input Voltage Range	± 10%
Input Current	9 A_{rms}
Output Voltage	400 V_{dc}
Output Current	18.75 A
Input Power Factor	> 0.99
Input Current Total Harmonic Distortion	< 5%
Ambient Temperature	50 ºC

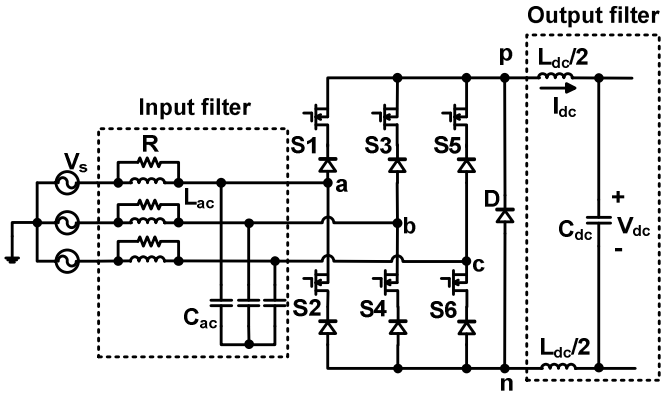


Fig. 2. Three-phase current source rectifier topology.

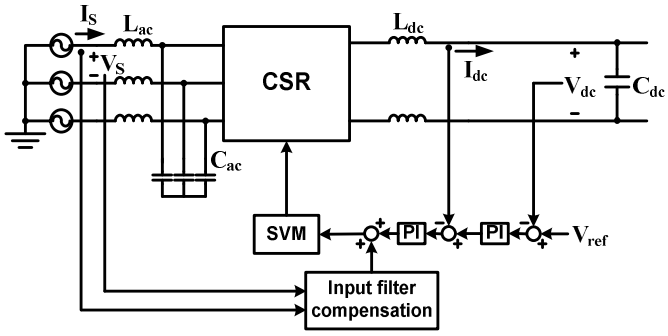
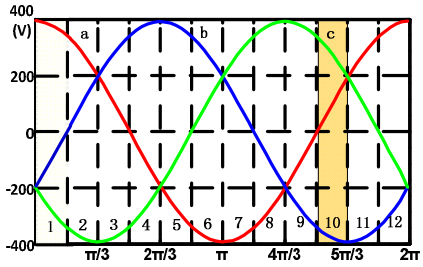


Fig. 3. Three-phase current source rectifier control algorithm.

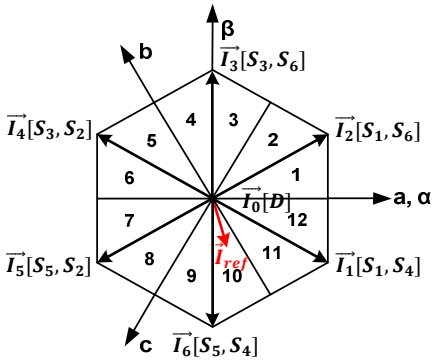
B. Control and Modulation Scheme

The control algorithm of CSR is shown in Fig. 3. The main control loop includes the outer DC voltage control loop and inner DC current control loop [19].

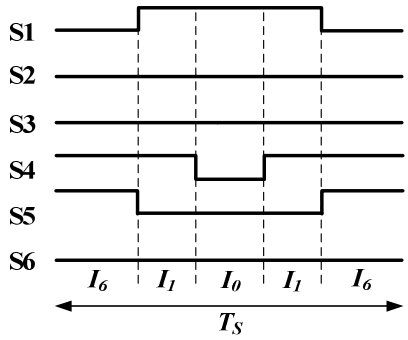
In the DC current control loop, the DC current (I_{dc}) in the output DC inductor is fed back to the current compensator to generate D_d, the duty cycle on the d axis. In the outer DC voltage control loop, the DC voltage (V_{dc}) on the DC capacitor is fed back to generate the DC current reference for the inner DC current control loop. To compensate the displacement power factor caused by the input filter, an input filter current compensation unit is introduced to generate the compensation duty cycles of d axis and q axis, which would be added to D_d and D_{qref} (the duty cycle reference on the q axis which is 0 in the unity power factor rectifier) respectively.



(a) Input phase voltage waveforms with 12 sectors



(b) Space vectors for three-phase CSR



(c) Sequence of switching state vectors in sector 10

Fig. 4. Switching loss optimized modulation scheme for three-phase CSR.

To reduce devices' switching loss, the switching loss optimized (SLO) modulation scheme is used for the three-phase CSR. This modulation has been proved to be able to obtain the lowest power loss and increase three-phase current source converters' efficiency [20]-[21].

The SLO modulation is a symmetric space vector pulse width modulation (SVPWM) with 12 sectors, as shown in

Fig. 4(a) and (b). The space vectors are arranged so that the average switching voltage is lowest in symmetric modulation schemes. In sector 10, for example, the vector, commutating with zero vector (I_0), is I_1 not I_6, because the absolute value of line-to-line voltage V_{ab} is lower than V_{bc}, i.e. $|V_{ab}| < |V_{bc}|$ in sector 10, as shown in Fig. 4(a). Fig. 4(c) shows the gate signals of six active devices in CSR in one switching period (T_S) in sector 10. The zero vectors are realized by conducting the freewheeling diode D instead of a phase-leg, to reduce conduction loss and avoid switching of active switches as well.

From Fig. 4(c), S4 and S5 are ON to form current vector I_6. When I_6 commutates to I_1, the DC current commutates from S5 to S1. To realize I_0, only S4 is turned off and S1 is still ON, to avoid switching loss on S1. S1 keeps ON during zero vector because V_a has lower absolute value than V_b and V_c in sector 10.

C. Converter Design

The active switch used in the three-phase CSR is 1200 V SiC MOSFETs, CMF20120D, from Cree. Both series diode in phase-leg and freewheeling diode are 1200 V SiC Schottky diodes, SDP60S120D, from SemiSouth. Their static characteristics are measured, and switching performance is evaluated based on current source topology in [22].

In order to reduce the power losses and obtain high efficiency, power devices are paralleled. The conduction loss of paralleled MOSFETs and diodes are given in (1) and (2) respectively, combining with average and rms current values of active switch, series diode, and freewheeling diode, presented in [5]. The switching energy of paralleled SiC MOSFETs is calculated from the sum of all MOSFETs' switching energies, obtained from the switching tests in [22], in a line period. The switching loss of paralleled MOSFETs is given in (3),

$$P_{MOS,con} = I_{MOS,rms}^2 \cdot \frac{R_{MOS}}{n_{MOS}} \quad (1)$$

$$P_{D,con} = I_{D,avg} \cdot V_{th} + I_{D,rms}^2 \cdot \frac{R_D}{n_D} \quad (2)$$

$$P_{MOS,sw} = f \cdot n_{MOS} \cdot \sum_n (E_{on}(v_{ds}, \frac{i_{ds}}{n_{MOS}}) + E_{off}(v_{ds}, \frac{i_{ds}}{n_{MOS}})) \quad (3)$$

where n_{MOS} is the paralleling number of MOSFET, n_D is the paralleling number of diode, f is the input voltage line frequency, and n is the number of switching instants of the MOSFET in a line period. Current balance for paralleled MOSFETs is assumed. Considering converter efficiency and cost, four paralleled MOSFETs and two paralleled SiC Schottky diodes for both series diode and freewheeling diode are used to build this CSR.

The input and output filters are designed in [23], with 10.57 W and 8.38 W loss respectively. Input filter consists of 6 µF capacitor, 100 µH inductor, and 180 Ω damping resistor in each phase. Output filter consists of 150 µF capacitor and 1.9 mH inductor. The switching frequency is 28 kHz to achieve low total loss of the rectifier [23].

D. Converter Test

Fig. 5 shows the prototype of this liquid cooled SiC based three-phase CSR. The main board hosts power devices, gate drivers, sensors, AC/DC capacitors, and device overvoltage protection circuit. The interface board is used to realize sensor signal processing, PWM signal processing, and auxiliary power supply.

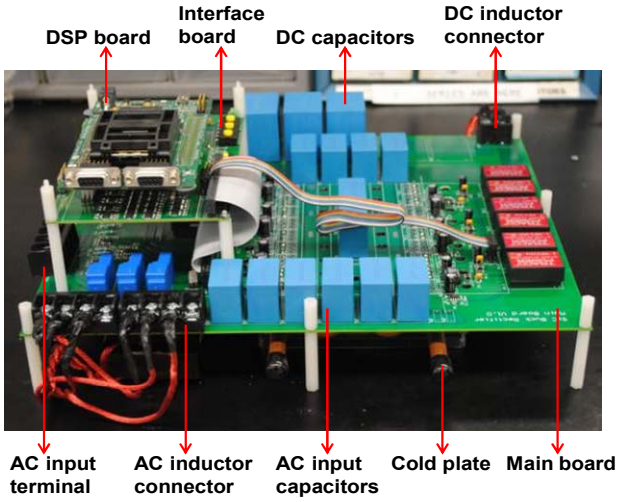


Fig. 5. SiC based three-phase CSR prototype.

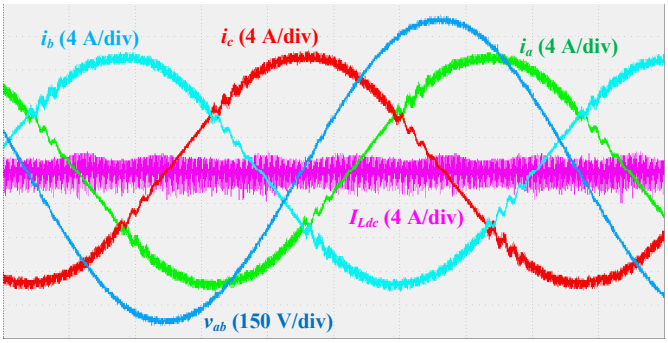


Fig. 6. Full load waveforms of SiC based three-phase CSR.

In the test, the converter is cooled via 50 °C liquid with 50% ethylene glycol and 50% water, provided by a chiller. The liquid flow rate is 5.68 liter per minute (LPM). The load is resistor load. Fig. 6 shows the full load waveforms of the converter. The measured input power factor is 0.9996 and the input current total harmonic distortion (THD) is 2.9%, which meet the requirement in Table I.

The power of the converter is measured and calculated using the PZ4000 power analyzer. Input power P_{in} is calculated by (4) and output power P_{out} is calculated by (5). The 12 W auxiliary circuit loss P_{aux} is included in the efficiency calculation. The efficiency η of the converter can be calculated by (6).

$$P_{in} = I_a \times V_{ac} + I_b \times V_{bc} \quad (4)$$

$$P_{out} = I_{dc} \times V_{dc} \tag{5}$$

$$\eta = \frac{P_{out}}{P_{in} + P_{aux}} \times 100\% \tag{6}$$

Fig. 7 shows the CSR efficiency curve. The peak efficiency of 98.55% appears at 6.4 kW output power and the converter full load efficiency is 98.54%.

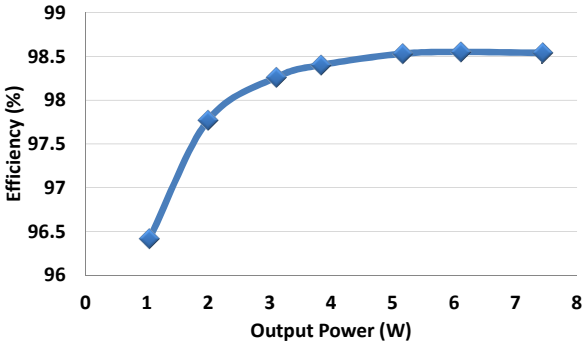


Fig. 7. SiC based three-phase CSR efficiency curve.

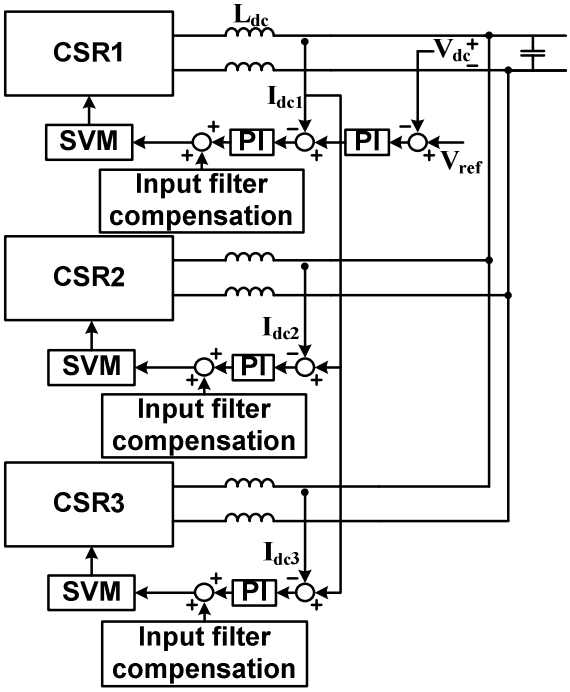
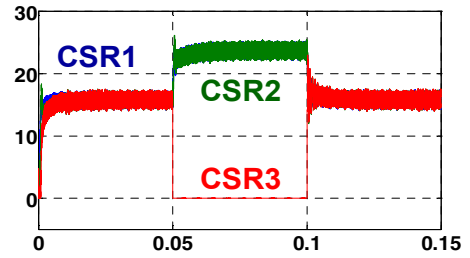


Fig. 8. Master-slave control for paralleled CSRs.

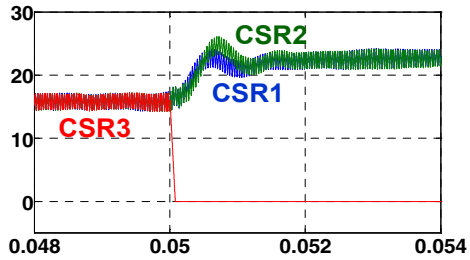
III. Paralleled Current Source Rectifiers

Converter paralleling has been a popular choice to achieve high power ratings and system redundancy which are necessary for power supply systems. The proper current distribution strategies among rectifier modules are necessary to achieve reliable parallel operation. Furthermore, the hot swapping and flexibility in paralleling any number of the converter modules are expected.

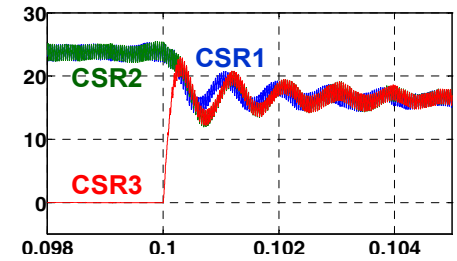
The master-slave control (MSC) is simple and stable control and has been widely used for paralleled voltage source inverters in uninterruptible power supply (UPS) systems. The master module specifies the parallel output voltage and provides the output current reference for each module. The slave modules are designed to be current followers to achieve fast dynamic response and good current distribution [7].



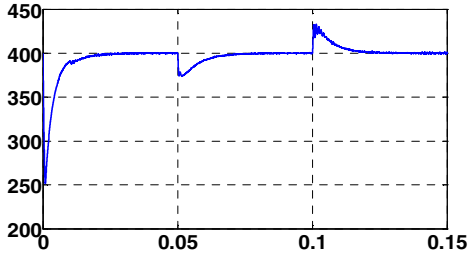
(a) Output currents I_{dc}



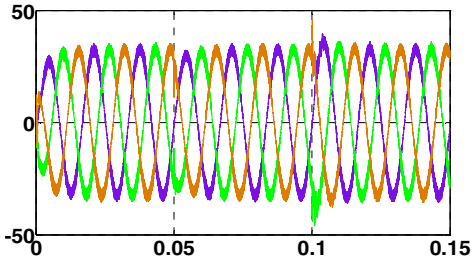
(b) Output currents at t = 0.05 s



(c) Output currents at t = 0.1 s



(d) Output voltage V_{dc}



(e) Output currents I_{ac}

Fig. 9. Simulation waveforms of three paralleled CSRs.

Fig. 8 shows the proposed MSC for paralleled three-phase CSRs, based on the single CSR control algorithm shown in Fig. 3. Take three paralleled CSRs as an example. Only CSR1, the master rectifier, has the outer control loop, V_{dc} loop, to provide reference for its inner loop. The slave rectifiers, CSR2 and CSR3, have only I_{dc} loop and their DC currents follow the DC current of CSR1. Each rectifier module has a compensator to compensate the displacement power factor caused by the input filter.

Fig. 9 shows the simulation results of three paralleled CSRs with 480 V_{rms} line-to-line input voltage, 400 V_{dc} output voltage, and rated output current of 47.5 A. At the beginning, t = 0 s, three CSRs work together. At t = 0.05 s, CSR3 is removed from the system. The master rectifier increases its output and CSR2 follows it, shown in Fig. 9(b), to support the full load. At t = 0.1 s, CSR3 is added to the system. The master rectifier decreases its output and slaves follow it, shown in Fig. 9(c). Fig. 9(d) and (e) show the fast dynamic response of V_{dc} and I_{ac} during these two transients.

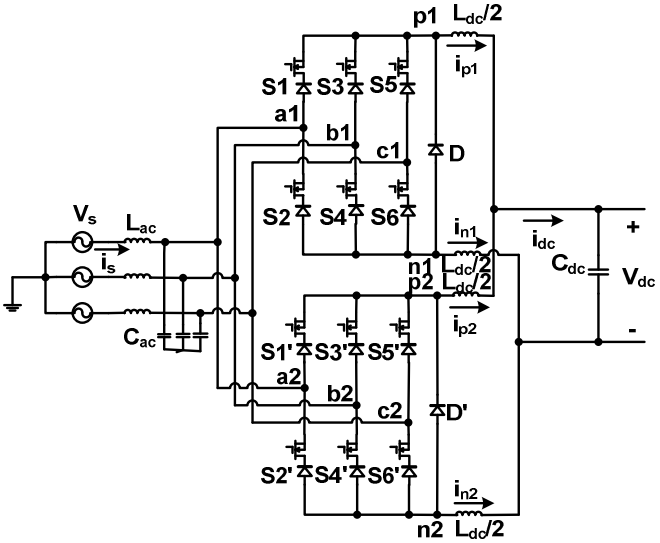
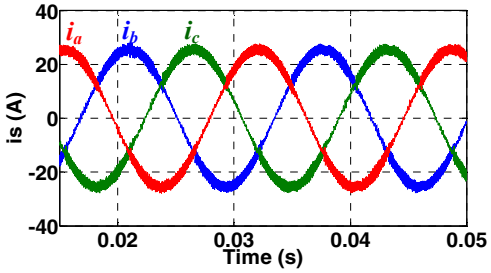


Fig. 10. Paralleled three-phase current source rectifiers.

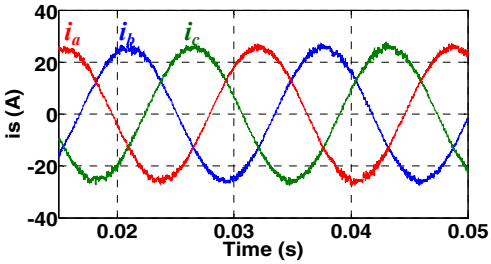
IV. Circulating Current Suppression

Interleaving can further improve the benefits of converter paralleling. By phase-shifting the PWM switching cycles of an individual CSR by an appropriate angle, the current ripple in the DC side and AC line harmonic current can be reduced [24]-[25]. As a result, smaller values of passive components or lower switching frequency can be used to meet current harmonics and ripple requirements. Both of them can help to reduce the loss of paralleled converter system. In this work, symmetric interleaving is used where the interleaving angle is π for two-paralleled converter system.

Fig. 10 shows a system of two paralleled CSRs which shares a common *L*-*C* input filter and DC capacitor. Each converter is the three-phase CSR designed above. The rated power of the paralleled CSR system is 15 kW. The input voltage is 480 V_{rms} line-to-line voltage. The rated DC voltage is 400 V_{dc} and DC current is 37.5 A. The passive component values are the same as the single CSR.

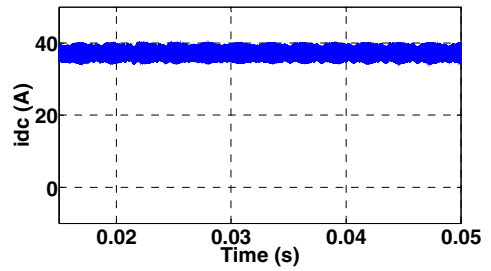


(a) AC current without interleaving

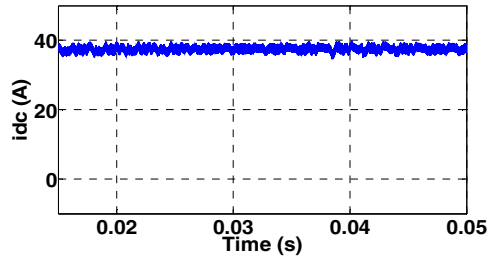


(b) AC current with interleaving

Fig. 11 AC side currents comparison in simulation.



(a) DC current without interleaving



(b) DC current with interleaving

Fig. 12. DC side currents comparison in simulation.

The currents of the AC input side and DC output side are compared in simulation with the interleaving angles of 0 (no interleaving) and π, in Fig. 11 and Fig. 12 respectively, using 28 kHz switching frequency. From Fig. 11, the AC current harmonics with the same filtering efforts are reduced by interleaving; the THD of input current reduces from 6.5% to 3.0%. From Fig. 12, the DC inductor current ripple reduces from 7.5 A to 5 A after interleaving, using the same DC inductor value.

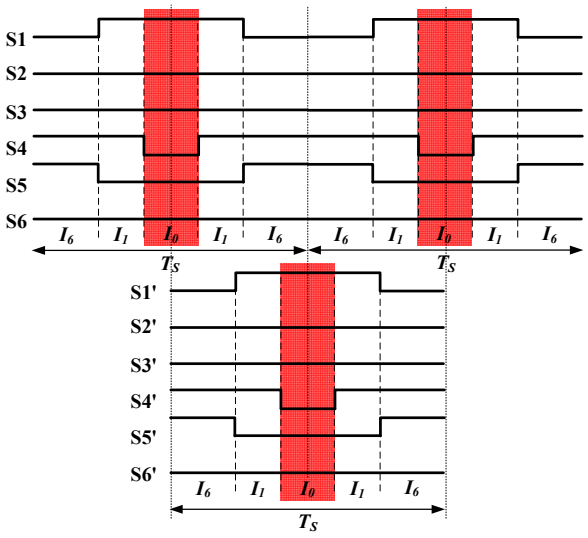
Paralleling three-phase current source rectifiers directly without using an isolation transformer will result in circulating currents i_C,

$$i_C = \frac{i_{p1} + i_{n1}}{2} = -\frac{i_{p2} + i_{n2}}{2} \tag{7}$$

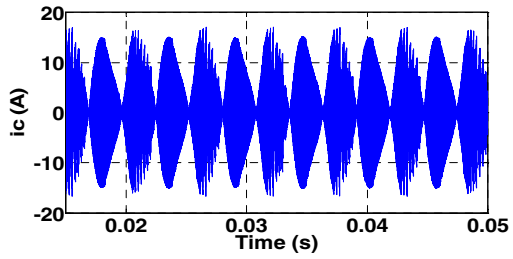
caused by the difference of their common-mode voltages (CMV) ΔV_{CM},

$$\Delta V_{CM} = \frac{(v_{p1} + v_{n1}) - (v_{p2} + v_{n2})}{2} \tag{8}$$

The circulating currents are superimposed to DC link currents but do not contribute to the output current. For a single converter, CMV does not induce any current because physically there is no such current path [17]. The CMV magnitude is increased by the freewheeling states and induces higher circulating current [26]. The circulating current will increase power loss, saturate inductors, overstress or even damage power devices, so it must be suppressed.



(a) Sequence of switching state vectors in sector 10 for two symmetric interleaved CSRs



(b) Circulating Current

Fig. 13. Interleaved CSRs with SLO modulation.

Fig. 13 (a) shows the gate signals of active switches in sector with SLO modulation introduced above, when paralleling two CSRs with symmetric interleaving. From Fig. 13(a), the two converters do not take the freewheeling state at the same time. In sector 10, the second CSR takes the freewheeling state by conducting D' and $v_{p2} = v_{n2} = v_a$. At this time, however, the first CSR is taking the vector I_6 and $v_{p1} = v_c$, $v_{n1} = v_b$. Then the CMV is

$$\Delta V_{CM} = \frac{2v_a - v_b - v_c}{2} \tag{9}$$

As a result, large circulating current appears, shown in Fig. 13(b). The CMV has a larger value during the zero vector than the non-zero vectors.

To suppress the circulating current, two CSRs should take the freewheeling state at the same time. As shown in Fig. 14, both the duration of I_0 in the center and edge of a switching cycle are $T_0/2$, where T_0 is the duration of I_0 in a switching cycle. During zero vector, voltages of v_{p1}, v_{n1}, v_{p2}, and v_{n2} are all v_a, so CMV is 0.

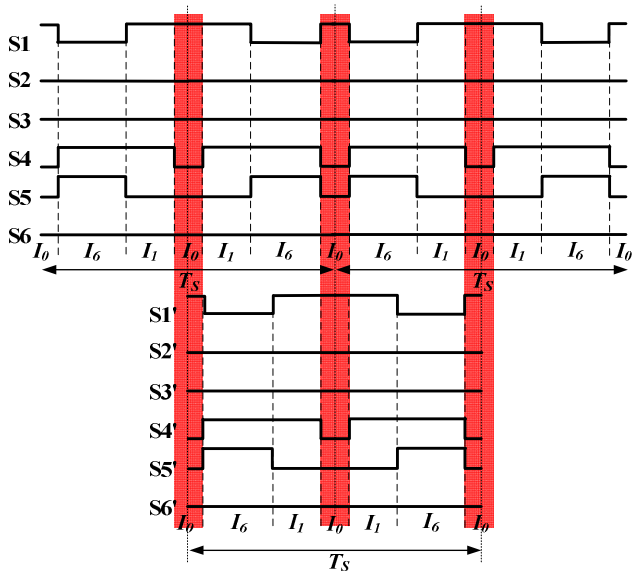


Fig. 14. Sequence of switching state vectors in sector 10 for two symmetric interleaved CSRs taking freewheeling state at the same time.

To avoid excessive switching actions, the modulation scheme in Fig. 14 is improved and shown in Fig. 15(a). The freewheeling state on the edge of the switching cycle is realized by keeping S5/S5' ON, not S4/S4', because $|V_{ac}| < |V_{ab}|$ in sector 10. With the modulation scheme in Fig. 15(a), the CMV during freewheeling state will be

$$\Delta V_{CM} = v_a - v_c \tag{10}$$

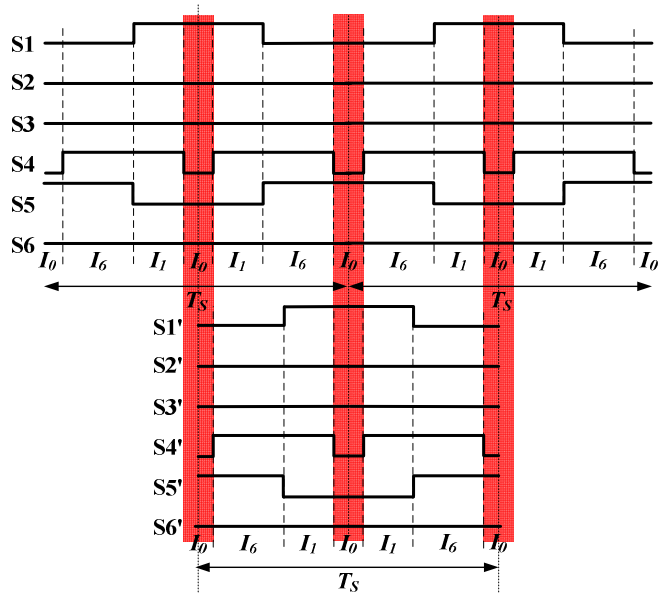
Because the value of v_b is from -340 V to -392 V in sector 10, the value of CMV in (10) is much smaller than in (9). During the non-zero states, if one CSR takes current vector I_1 and another CSR takes I_6, the CMV will be

$$\Delta V_{CM} = \frac{v_a - v_c}{2} \tag{11}$$

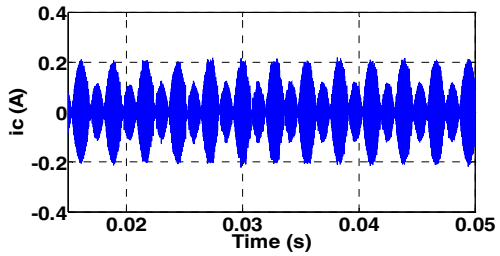
As a result, the circulating current for two interleaved CSRs are reduced according to (10) and (11), shown in Fig. 15(b), since (v_a - v_c) is from 340 V to 0 V in sector 10.

The drawback of the modulation scheme shown in Fig. 15(a) is two more switching actions of S4/S4' in a switching period. However, with the symmetric interleaving where the interleaving angle is π, the real switching frequency of two paralleled CSRs can be reduced to half of the original switching frequency to keep the same current harmonics and ripples. So the total loss of the paralleled CSRs system will not be increased. Fig. 16 compares the total loss of two paralleled CSRs at two different cases. Case I is two

paralleled CSRs with f_{SW} = 28 kHz using SLO modulation without interleaving. Case II is symmetric interleaved CSRs with improved modulation scheme in Fig. 15(a), to suppress circulating current. The switching frequency for each CSR is 14 kHz. From Fig. 16, the total loss of 15 kW paralleled CSRs is 174 W in Case I and 163 W in Case II, which shows the loss reduction by using the improved modulation scheme.



(a) Sequence of switching state vectors in sector 10 for two symmetric interleaved CSRs



(b) Circulating Current

Fig. 15. Interleaved CSRs with improved modulation scheme.

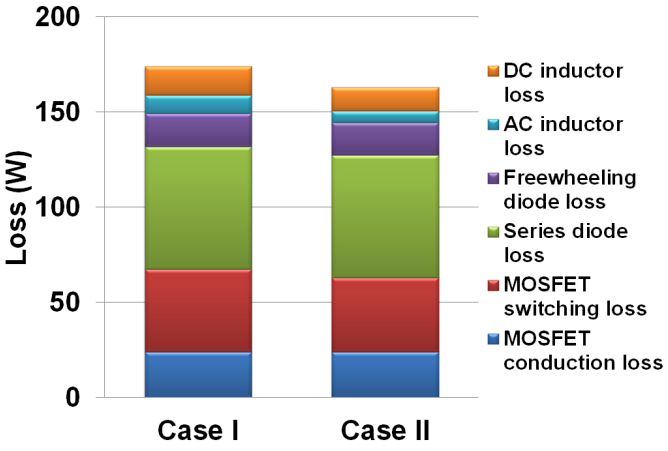


Fig. 16. Loss comparison of two different cases.

V. Conclusions

This paper presents a 7.5 kW, liquid cooled high efficiency three-phase current source rectifier, using SiC MOSFETs and Schottky diodes, for 400 V_{dc} architecture based data center power supplies. The good performance of the rectifier is verified and 98.54% full load efficiency is obtained in experiments. The master-slave control for paralleled three-phase CSRs is developed to achieve current distribution control and hot-swap. Moreover, the improvement of switching loss optimized modulation scheme is proposed to reduce the circulating current effectively. The total loss of paralleled rectifier system is reduced by converter interleaving and using improved modulation scheme by loss calculation and comparison.

Acknowledgment

This work made use of Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and DOE under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

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