A Novel Gate Assist Circuit for Cross Talk Mitigation of SiC Power Devices in a Phase-leg Configuration

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Abstract—Silicon Carbide (SiC) power devices have inherent capability for fast switching. However, in a phase-leg configuration, high $dv/dt$ will worsen the interference between the two devices during a switching transient (i.e., cross talk), leading to slower switching speed, excessive switching losses, and overstress of power devices. Unfortunately, due to intrinsic properties, such as low threshold voltage, low maximum allowable negative gate voltage, and large internal gate resistance, SiC power devices are easily affected by cross talk. This paper proposes a novel gate assist circuit using an auxiliary transistor in series with a capacitor to mitigate cross talk. Based on CMF20120D SiC MOSFETs, the experimental results show that the new gate assist circuit is capable of reducing the turn-on switching loss up to 19.3%, and suppress the negative spurious gate voltage within the maximum allowable negative gate voltage without the penalty of further decreasing the device switching speed. Moreover, in comparison to a conventional gate drive with -2 V turn-off gate voltage, this gate assist circuit without negative isolated power supply is more effective in improving the switching behavior of power devices in a phase-leg. The proposed gate assist circuit is a cost-effective solution for cross talk mitigation.

I. INTRODUCTION

To achieve higher performance power conversion, wide band-gap semiconductor devices such as silicon carbide (SiC) have become a promising alternative to silicon, offering increased junction operating temperature, low specific on-resistance, and high switching-speed capability. Among these benefits, the fast switching performance plays a key role in reducing switching losses, shortening dead time for a phase-leg, and increasing switching frequency. All of these are beneficial to high power efficiency, quality and density [1-3]. However, in the actual converter composed of a phase-leg configuration, high $dv/dt$ during fast switching transient of one device will affect the operating behavior of its complementary device [4-11]. This interaction between the two switches is cross talk [11]. Specifically, during the turn-on transient of one device, due to the induced positive spurious gate voltage, its complementary device might be partially turned on. As a result, a shoot-through current is generated, leading to excessive switching loss in both switches or even shoot-through failure. In addition, due to the self-regulating mechanism of power devices, this shoot-through current will limit $dv/dt$ as well, and then decrease the switching speed of power devices [11].

During turn-off transient of one device, the negative spurious voltage induced at the gate terminal of its complementary device will overstress the power device if its magnitude exceeds the maximum allowable negative gate voltage acceptable to the semiconductor device. Therefore, in a phase-leg configuration, to guarantee the reliability of the power converter and fully utilize the potential advantages of fast switching-speed performance and low switching loss of SiC power devices, cross talk must be suppressed.

Prior reported work has proposed several methods for cross talk mitigation [2, 12-16]. It can be roughly divided into three categories. First, decrease the switching speed to reduce $dv/dt$. Generally, it is implemented by adding an external capacitor between the gate-to-source terminals of power devices or increasing resistance in the gate loop [12-15]. This solution improves the reliability of power devices with the penalty of slower switching speed and more switching losses.

Second, use a negative biased turn-off gate voltage [12-15]. This method suppresses the impact of cross talk during turn-on transient, but it will worsen the overstress of power devices due to the higher negative spurious gate voltage induced during turn-off transient, especially for the SiC power device when considering its lower maximum allowable negative gate voltage compared with the silicon-based power device (see Table I). Additionally, this method is less cost-effective due to the additional negative isolated power supply that is required.

Third, use active Miller clamping [15, 16]. The operation principle of this method is to monitor the gate voltage of the power devices, and based on this measured gate voltage, identify the existence of cross talk [15]. However, due to the fairly large internal gate resistance of SiC power devices, as shown in Table I, the measured gate voltage is less than that of the internal gate-to-source
TABLE I. CHARACTERISTICS OF SEVERAL COMPARABLE Si/SiC POWER DEVICES [19-23]

<table>
<thead>
<tr>
<th>Type</th>
<th>Manufacturer</th>
<th>Model</th>
<th>$V_{th}$ / $I_D$ (100 °C)</th>
<th>$V_{gs(th)}$ (25 °C)</th>
<th>Negative $V_{gs(max)}$</th>
<th>$R_{gate}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TFS Si IGBT</td>
<td>Fairchild</td>
<td>FGA20N120FTD</td>
<td>1200 V / 20 A</td>
<td>5.9 V</td>
<td>-25 V</td>
<td>N/A</td>
</tr>
<tr>
<td>NPT Si IGBT</td>
<td>IR</td>
<td>IRGP20H120U</td>
<td>1200 V / 20 A</td>
<td>3.1 V</td>
<td>-20 V</td>
<td>N/A</td>
</tr>
<tr>
<td>Si MOSFET</td>
<td>Microsemi</td>
<td>APT34M120J</td>
<td>1200 V / 22 A</td>
<td>4.0 V</td>
<td>-30 V</td>
<td>N/A</td>
</tr>
<tr>
<td>SiC MOSFET</td>
<td>CREE</td>
<td>CMF20120D</td>
<td>1200V / 17 A</td>
<td>2.5 V</td>
<td>-5 V</td>
<td>5 Ω</td>
</tr>
<tr>
<td>Normally-off SiC JFET</td>
<td>Semisouth</td>
<td>SJEP120R100</td>
<td>1200V / 17A</td>
<td>1.0 V</td>
<td>-15 V</td>
<td>6 Ω</td>
</tr>
</tbody>
</table>

The proposed gate assist circuit to mitigate cross talk for SiC power devices is shown in Fig. 1. Compared with the conventional gate drive circuit, only one auxiliary transistor ($S_{3,H}$ or $S_{3,L}$) in series with one capacitor ($C_H$ or $C_L$) is added between the gate-to-source terminals of each device. Fig. 2 displays the logic signals of its corresponding transistors.

The operation principle of the proposed gate assist circuit is described below, as shown in Fig. 3.

Subinterval 1 $[t_0 - t_1]$: Auxiliary capacitor pre-charge. Before main power devices start to operate, the auxiliary capacitor $C_L$ and $C_H$ need to be pre-charged. Via the body diode of auxiliary transistors $S_{2,L}$, $S_{3,H}$ and gate resistor $R_g$, $V_{gs(H)}$ voltage across $C_L$ and $C_H$ is established to the negative gate voltage $V_2$ at the end of $t_1$. Duration of this subinterval is determined by the time constant $R_gC$.

Subinterval 2 $[t_1 - t_2]$: Initialization completion. Auxiliary transistors $S_{3,H}$, $S_{3,L}$ remain off to wait for the operation of the main power devices. At the end of $t_2$, the upper switch starts to turn on.

Subinterval 3 $[t_2 - t_3]$: Turn-on transient of the upper switch. $S_{1,H}$ turns on, and both $S_{2,H}$ and auxiliary transistor $S_{2,H}$ turn off. At this moment, the gate-to-source terminals of the upper switch are equivalently connected with the output capacitor of $S_{1,H}$ in series with $C_{IN}$. Since the output capacitance of the auxiliary transistor is usually an order of magnitude smaller than the input capacitance of the main power device, this auxiliary circuit has no impact on the turn-on switching behavior of the upper switch. Meanwhile, $S_{1,L}$ turns off, and both $S_{2,L}$
and auxiliary transistor $S_{3,L}$ turn on. $C_L$ directly connects with the gate-to-source terminals of the lower switch. This large external capacitance offers a low impedance loop to $C_{dv/dt}$ induced current during the turn-on transient of the upper switch, that is, the gate loop impedance of the lower switch is largely decreased. Therefore, the positive spurious gate voltage would be minimized, and then the cross talk during turn-on transient is suppressed. At the end of $t_3$, the turn-on transient of the upper switch is completed.

Subinterval 4 $[t_3 - t_4]$: Fully turn-on the upper switch. Switching status of all transistors remain the same as that during subinterval 3. The negative power supply $V_{2,L}$ starts to discharge $C_L$ and $C_{gs,L}$ through $R_{g,L}$ until voltages across $C_L$ and $C_{gs,L}$ return to $V_{2,L}$. At the end of $t_4$, the upper switch starts to turn off.

Subinterval 5 $[t_4 - t_5]$: Turn-off transient of the upper switch. $S_{1,H}$ turns off, $S_{2,H}$ turns on, and auxiliary transistor $S_{3,H}$ remains off. Just as in subinterval 3, this auxiliary circuit does not affect the turn-off switching performance of the upper switch. Meanwhile, auxiliary transistor $S_{3,L}$ remains on. The gate loop impedance of the lower switch is decreased due to the low impedance $C_L$. Also, the negative spurious gate voltage is minimized. At the end of $t_5$, the turn-off transient of the upper switch is finished.

Fig. 3. Operation principle of the proposed gate assist circuit: (a) Subinterval 1 $[t_0 - t_1]$; (b) Subinterval 2 $[t_1 - t_2]$; (c) Subinterval 3 $[t_2 - t_3]$; (d) Subinterval 4 $[t_3 - t_4]$; (e) Subinterval 5 $[t_4 - t_5]$; and (f) Subinterval 6 $[t_5 - t_6]$.
Subinterval 6 \([t_5 - t_6]\): Fully turn-off the upper switch. Auxiliary transistor \(S_{3, L}\) turns off. \(C_L\) is disconnected from the lower switch for the upcoming switching transient of the lower switch. The negative power supply \(V_{2, L}\) starts to charge \(C_{gs, L}\) through \(R_{g, L}\) until \(V_{gs, L}\) returns to \(V_{2, L}\). At the end of \(t_6\), the lower switch starts to turn on.

Based on the circuit structure symmetry, subintervals 7-10 are similar to subintervals 3-6.

According to the operation principle, the logic signals of auxiliary transistors are almost the same as that of their complementary main power devices, except that the auxiliary transistors will remain on until the end of turn-off transient of the complementary main power devices, as shown in Fig. 2 (shaded area). Consequently, logic signals of auxiliary transistors can be easily synthesized based on the logic signals of main power devices, and this feedforward control scheme is suitable for the SiC power devices with fast switching capability.

III. PRIMARY PARAMETERS DESIGN

To avoid cross talk during both turn-on and turn-off transient, the spurious gate voltage must be limited within the range from the maximum allowable negative gate voltage \(V_{gs, max(-)}\) to the threshold voltage \(V_{th}\). Thus, a key issue for cross talk suppression is to obtain and control the positive and negative peak value of spurious gate voltage with the gate assist circuit during turn-on and turn-off switching transient. Assume the lower switch is the device under interference, Fig. 4 shows the simplified equivalent circuit of the lower switch during the switching transient of the upper one. The corresponding waveforms of spurious gate voltage and auxiliary capacitor voltage are shown in Fig. 5.

During the turn-on transient of the upper switch (i.e., subinterval 3), the positive peak value of the spurious gate voltage \(V_{gs(+)}\) is expressed as

\[
V_{gs(+)} = V_{2, L} + \Delta V_+ = V_{2, L} + \frac{C_{gs, L} V_{dc}}{A} + \frac{C_{gd, L} V_{dc} \alpha_{ON}}{A} \left(1 - e^{-\alpha_{ON} \frac{V_{dc}}{C_{gs, L} V_{dc}}}\right)
\]

(1)

where \(C_{iss, L}\) refers to the input capacitance of the lower switch, the sum of Miller capacitance \(C_{gd, L}\) and gate-to-source capacitance \(C_{gs, L}\). \(A\) is the sum of \(C_{L}\) and \(C_{iss, L}\). \(R_{g, L}\) is internal gate resistance of the lower switch. \(V_{dc}\) is the dc bus voltage, \(V_{2, L}\) is the negative gate voltage of the lower switch, and \(a_{ON}\) is the slew rate of drain-to-source voltage of the lower switch during the turn-on transient of the upper device, as shown in Fig. 4.

During the turn-off transient of the upper switch (i.e., subinterval 5), the negative peak value of the spurious gate voltage \(V_{gs(-)}\) is given by

\[
V_{gs(-)} = V_{2, L} - \Delta V_- = V_{2, L} - \frac{C_{gd, L} V_{dc}}{A} - \frac{C_{gs, L} V_{dc} \alpha_{OFF}}{A} \left(1 - e^{-\alpha_{OFF} \frac{V_{dc}}{C_{gs, L} V_{dc}}}\right)
\]

(2)

where \(a_{OFF}\) is the slew rate of drain-to-source voltage of the lower switch during the turn-off transient of the upper device, as shown in Fig. 4.

According to the aforementioned analysis, to avoid cross talk, the following requirement must be satisfied

\[
\Delta V_+ + \Delta V_- \leq V_{th} - V_{gs, max(-)}
\]

(3)

\[
V_{gs, max(-)} + \Delta V_- \leq V_2 \leq V_{th} - \Delta V_+
\]

(4)

Fig. 4. Simplified equivalent circuit of the lower switch during the switching transient of the upper switch.

Fig. 5. Spurious gate voltage (blue curve) and auxiliary capacitor voltage (green curve) during switching transient.

Fig. 6. Primary parameters design: (a) Selection ranges of \(C\); and (b) Selection ranges of \(V_2\).
TABLE II. PARAMETERS OF CMF20120D AND SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gd}$</td>
<td>13 pF</td>
</tr>
<tr>
<td>$C_{gs}$</td>
<td>1900 pF</td>
</tr>
<tr>
<td>$V_{th}$</td>
<td>2.5 V</td>
</tr>
<tr>
<td>$V_{gs, max}$</td>
<td>-5 V</td>
</tr>
<tr>
<td>$V_{d}$</td>
<td>800 V</td>
</tr>
<tr>
<td>$a_{on}$</td>
<td>27 V/ns</td>
</tr>
<tr>
<td>$R_{gs, on}$</td>
<td>5 Ω</td>
</tr>
<tr>
<td>$a_{off}$</td>
<td>23 V/ns</td>
</tr>
</tbody>
</table>

* determined according to test results.

Substituting (1) and (2) into (3), the range of the auxiliary capacitance $C$ is determined. The negative biased turn-off gate voltage $V_2$ can be selected based on (4). Taking the CREE SiC MOSFET CMF20120D as an example, based on the parameters and specifications listed in Table II, the value ranges of $C$ and $V_2$ are shown in Fig. 6. The proper auxiliary capacitance is around 10 nF to 1 µF, and the proper negative biased turn-off voltage is around -3 V to 0 V.

IV. EXPERIMENTAL VERIFICATION

Double pulse tester board with CMF20120D SiC MOSFETs is shown in Fig. 7. Fig. 8 displays the gate driver board with the proposed gate assist circuit, which consists of a Si7308DN Si MOSFET with 100 nF ceramic capacitor.

To evaluate the effectiveness of the proposed gate assist circuit for cross talk mitigation, the comparison experiments are conducted under four different groups according to with or without gate assist circuit as well as with or without negative biased turn-off gate voltage, listed in Table III. For each group, 12 cases with gate resistances of 10/4.7 Ω, operating voltages of 800/600 V, and operating currents of 5/10/20 A are tested.

TABLE III. FOUR DIFFERENT GROUPS

<table>
<thead>
<tr>
<th>Group</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st</td>
<td>w/o gate assist circuit with $V_{gs}$ of 20/0 V</td>
</tr>
<tr>
<td>2nd</td>
<td>w/ gate assist circuit with $V_{gs}$ of 20/0 V</td>
</tr>
<tr>
<td>3rd</td>
<td>w/o gate assist circuit with $V_{gs}$ of 20/-2 V</td>
</tr>
<tr>
<td>4th</td>
<td>w/ gate assist circuit with $V_{gs}$ of 20/-2 V</td>
</tr>
</tbody>
</table>

Fig. 9 shows the comparison waveforms under four different groups with the operating condition of 800-V/10-A with 10 Ω gate resistance. In Fig. 9(a) and Fig. 9(b), it shows that during turn-on transient of the lower switch, with the same $V_{gs}$, the turn-on energy losses of the lower switch with gate assist circuit are less than that without gate assist circuit. Meanwhile, without further reducing the switching speed, this gate assist circuit improves the slew rate of the drain-to-source voltage.

Also, the excessive switching losses of the upper switch created by the cross talk induced shoot-through current are decreased once the gate assist circuit is adopted. Moreover, during the turn-off transient of the upper switch, by using the gate assist circuit, the spurious negative gate voltages of the lower switch is largely suppressed, as shown in Fig. 9(c). For example, under $V_{gs}$ of 20/0 V, with gate assist circuit, the turn-on energy loss of the lower switch and shoot-through energy loss of the
upper switch are reduced by 42.8 µJ and 39.3 µJ, respectively, enabling total turn-on energy loss saving of approximately 19.3%. In the meantime, $\frac{dv}{dt}$ increases from 22.7 V/ns to 24.4 V/ns. Also, the negative peak value of the spurious gate voltage is minimized from -6.60 V which exceeds -5 V, the maximum rating of negative gate voltage of the CMF20120D, listed in Table I, to -0.83 V.

Furthermore, in the comparison with the -2 V turn-off gate voltage in the conventional gate circuit (3rd Group), the gate assist circuit with 0 V turn-off gate voltage (2nd Group) still has better performance with turn-on energy losses reduced by 14.9 µJ during turn-on transient of the lower switch, and the spurious negative gate voltage of the lower switch minimized from -8.66 V to -0.83 V during turn-off transient of the upper switch.

**TABLE IV.** $E_{ON}$ & $dv/dt$ vs. $I_L$ UNDER 1st GROUP WITH $V_D$ OF 800V & $R_g$ OF 10 Ω

<table>
<thead>
<tr>
<th>$I_L$ (A)</th>
<th>5</th>
<th>10</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{ON}$ (µJ)</td>
<td>381.3</td>
<td>519.0</td>
<td>852.6</td>
</tr>
<tr>
<td>$dv/dt$ (V/ns)</td>
<td>23.5</td>
<td>22.7</td>
<td>21.1</td>
</tr>
</tbody>
</table>

**Fig. 10.** Comparison test results dependence on load current: (a) Normalized turn-on energy losses during the turn-on transient of the lower switch; (b) Normalized $\frac{dv}{dt}$ during the turn-on transient of the lower switch; and (c) Negative peak value of spurious gate voltage during the turn-off transient of the upper switch.

**Fig. 11.** Comparison test results dependence on dc bus voltage and gate resistance: (a) Normalized turn-on energy losses during the turn-on transient of the lower switch; (b) Normalized $\frac{dv}{dt}$ during the turn-on transient of the lower switch; and (c) Negative peak value of spurious gate voltage during the turn-off transient of the upper switch.
Fig. 10 displays the comparison test results dependence on the load current under the dc bus voltage of 800 V with 10 Ω gate resistance. In order to clearly demonstrate the effectiveness of the proposed gate assist circuit, the turn-on energy loss and \( dv/dt \) under 2\(^{nd}\), 3\(^{rd}\), and 4\(^{th}\) group are normalized based on that under 1\(^{st}\) group, which are listed in Table IV. It shows that under different load current, the turn-on energy losses with gate assist circuit are always less than that without gate assist circuit and \( dv/dt \) is higher under the same \( V_{gs} \). Furthermore, the turn-on switching performance by using the gate assist circuit with 0 V turn-off gate voltage (2\(^{nd}\) group) is better than that with negative turn-off gate voltage in the conventional gate circuit (3\(^{rd}\) group). Note also that the gate assist circuit has the capability of limiting the negative peak value of spurious gate voltages within its required range. Fig. 11 presents the comparison test results dependence on dc bus voltage and gate resistance under the load current of 10 A. According to the conditions under the 1\(^{st}\) group listed in Table V, turn-on energy loss and \( dv/dt \) under the 2\(^{nd}\), 3\(^{rd}\), and 4\(^{th}\) group are managed the same as that in Fig. 10. The experimental results show that under different dc bus voltage with varied gate resistance, the proposed gate assist circuit, even without negative biased turn-off voltage, is more effective to improve the switching behavior of power devices in a phase-leg configuration.

V. CONCLUSIONS

Considering the intrinsic characteristics of SiC power devices, a novel gate assist circuit is proposed for cross talk mitigation in a phase-leg configuration. The test results of the double pulse tester with CMF20120D SiC MOSFETs verify that in comparison with the conventional gate drive, the proposed gate assist circuit improves the switching performance under different operating conditions: turn-on transient becomes fast, turn-on switching loss is reduced, and spurious negative gate voltage is always suppressed within its required range. Additionally, compared with the conventional gate driver with -2 V turn-off gate voltage, this new gate assist circuit without negative isolated power supply is more effective to mitigate cross talk. The proposed gate assist circuit offers a simple, efficient, and cost-effective solution for cross talk mitigation.

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| Table V. \( V_{gs} \) & \( dv/dt \) vs. \( V_{gs} \) & \( R_{g} \) Under 1\(^{st}\) Group with IL of 10A |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| \( V_{gs} (V) \) | \( 600/4.7 \) | \( 600/10 \) | \( 800/4.7 \) | \( 800/10 \) |
| \( E_{on} (\mu J) \) | 263.8 | 332.0 | 416.3 | 519.0 |
| \( dv/dt (V/ns) \) | 29.7 | 19.7 | 33.1 | 22.7 |