A Reconfiguration Technique for Multilevel Inverters Incorporating a Diagnostic System Based on Neural Network

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***Abstract*— A reconfiguration technique for multilevel inverters incorporating a diagnostic system based on neural network is proposed in this paper. It is difficult to diagnose a multilevel-inverter drive (MLID) system using a mathematical model because MLID systems consist of many switching devices and their system complexity has a nonlinear factor. Therefore, a neural network (NN) classification is applied to the fault diagnosis of a MLID system. Multilayer perceptron networks are used to identify the type and location of occurring faults. The principal component analysis (PCA) is utilized in the feature extraction process to reduce the NN input size. A lower dimensional input space will also usually reduce the time necessary to train a NN, and the reduced noise may improve the mapping performance. The output phase voltage of a MLID can be used to diagnose the faults and their locations. The reconfiguration technique is also proposed. The effects of using the proposed reconfiguration technique at high modulation index are addressed. The proposed system is validated with experimental results. The experimental results show that the proposed system performs satisfactorily to detect the fault type, fault location, and reconfiguration.**

***Index Terms*— Diagnostic system, fault diagnosis, multilevel inverter, neural network, reconfiguration technique.**

I. INTRODUCTION

INDUSTRY has begun to demand higher power ratings, and multilevel inverter drives have become a solution for high power applications in recent years. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Two topologies of multilevel inverters for electric drive application have been discussed in [1]. The cascaded MLID is a general fit for large automotive all-electric drives because of the high VA rating possible and because it uses several level dc voltage sources which would be available from batteries or fuel cells [1].

A possible structure of a three-phase cascaded multilevel inverter drive for electric vehicle is illustrated in Fig. 1. The series of H-bridges makes for modularized layout and packaging; as a result, this will enable the manufacturing process to be done more quickly and cheaply. Also, the reliability analysis reported in [2] indicates that the fault-tolerance of cascaded MLID had the best life cycle cost.

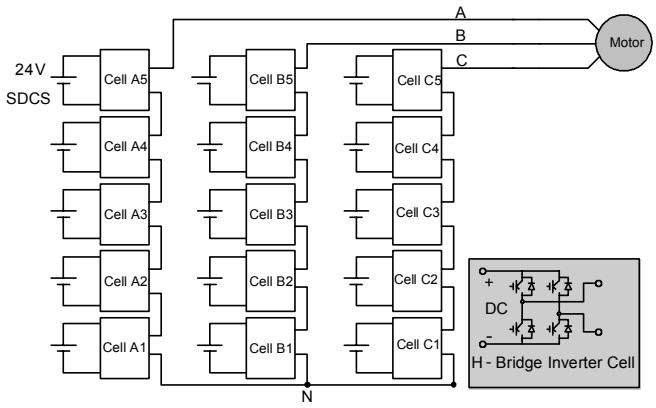


Fig. 1. Three-phase wye-connection structure for electric vehicle motor drive.

However, if a fault (open or short circuit) occurs at a semiconductor power switch in a cell, it will cause an unbalanced output voltage and current, while the traction motor is operating. The unbalanced voltage and current may result in vital damage to the traction motor if the traction motor is run in this state for a long time.

Generally, the conventional protection systems are passive devices such as fuses, overload relays, and circuit breakers to protect the inverter systems and traction motors. The protection devices will disconnect the power sources from the multilevel inverter system whenever a fault occurs, stopping the operated process. Despite a cascaded MLID has the ability to tolerate a fault for some cycles, it would be better if we can detect the fault and its location; then, switching patterns and the modulation index of other active cells of the MLID can be adjusted to maintain the operation under balanced load condition. Of course, the MLID can not be operated at full rated power. The amount of reduction in capacity that can be tolerated depends upon the application; however, in most cases a reduction in capacity is more preferable than a complete shutdown.

A study on fault diagnosis in drives begins with a conventional PWM voltage source inverter (VSI) system. The various fault modes for an induction motor are investigated in [3]. Then, the integration of a fault diagnosis system into VSI

drives is described in [4]. This integration system introduced remedial control strategies soon after failure occurrences; therefore, system reliability and fault tolerant capability are improved. A noninvasive technique for diagnosing VSI drive failures based on the identification of unique signature patterns corresponding to the motor supply current Park's Vector is proposed in [5].

Then, artificial intelligent (AI) techniques such as fuzzy-logic (FL) and neural network (NN) have been applied in condition monitoring and diagnosis. A study of a machine fault diagnosis system by using FFT and neural networks is clearly explained in [6]. Also, a fault diagnosis system for rotary machines based on fuzzy neural networks is developed in [7]. The possibilities offered by a neural network for fault diagnosis and system identification are investigated in [8].

Furthermore, a new topology with fault-tolerant ability that improves the reliability of multilevel converters is proposed in [9]. A method for operating cascaded multilevel inverters when one or more power H-bridge cells are damaged has been proposed in [2,10]. The method is based on the use of additional magnetic contactors in each power H-bridge cell to bypass the faulty cell. One can see from the literature survey that the knowledge and information of fault behaviors in the system is important to improve system design, protection, and fault tolerant control. Thus far, limited research has focused on MLID fault diagnosis and reconfiguration. Therefore, a MLID fault diagnosis system is proposed in this paper that only requires measurement of the MLID's voltage waveforms.

II. Diagnostic Signals

It is possible that AI-based techniques can be applied in condition monitoring and diagnosis. AI-based condition monitoring and diagnosis have several advantages; for instance, AI-based techniques do not require any mathematical models, therefore the engineering time and development time could be significantly reduced [11]. AI-based techniques utilize the data sets of the system or make full utilization of expert knowledge. In MLID applications, the output phase voltage can convey valuable information to diagnose the faults and their locations. For example, output voltage signals of open circuit faults in each location of two 12 V separate dc source (SDCS) MLID as shown in Fig. 2 with multilevel carrier-based sinusoidal PWM gate drive signals are shown in Fig. 3 and Fig. 4. Obviously, all output voltage signals are related to the fault locations. Additionally, the output voltages

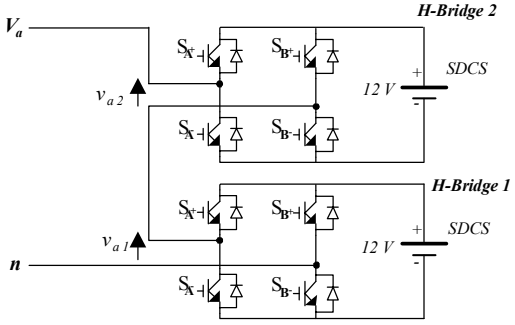
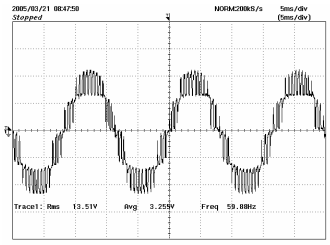
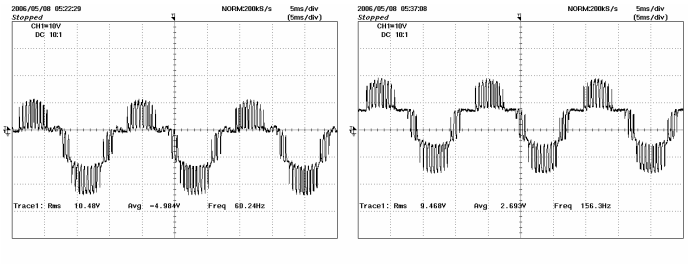


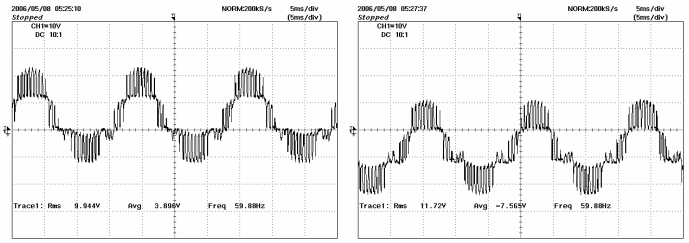
Fig. 2. Single-phase multilevel-inverter system.



(a)

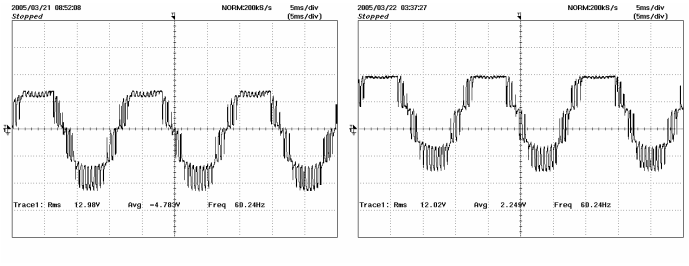


(b) (c)

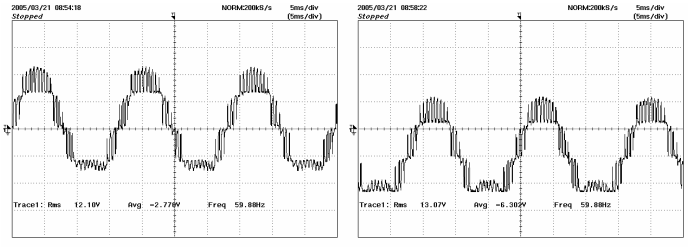


(d) (e)

Fig. 3. Experiment of fault features at (a) normal, (b) S_{A+} fault, (c) S_{A-} fault, (d) S_{B+} fault, and (e) S_{B-} fault of H-bridge 1 with modulation index = 0.8 out of 1.0.



(a) (b)



(c) (d)

Fig. 4. Experiment of fault features at (a) S_{A+} fault, (b) S_{A-} fault, (c) S_{B+} fault, and (d) S_{B-} fault of H-bridge 2 with modulation index = 0.8 out of 1.0.

of a MLID can also be used to diagnose the fault types (open and short circuit) as depicted in Fig. 5.

We can see that all fault features can be visually distinguished in both fault types and fault locations; however, the computation unit cannot directly visualize as a human does. A neural network is one suitable AI-based technique which can be applied to classify the fault features. Besides, a classification technique using a neural network offers an extra degree of freedom to solve a nonlinear problem: the failure of a single neuron will only partially degrade performance. If an input neuron fails, the network can still make a decision by using the remaining neurons. In contrast, if only a single input, for instance the dc offset of signals, is used as the input data to classify the faults, the diagnosis system may not perform classification when the input data has drifted or the single sensor has failed. Furthermore, a neural network also permits parallel configuration and seasonal changes. Additional H-bridges and fault features (short circuit) can be conveniently extended into the system with more training data and parallel configuration.

Therefore, we will attempt to diagnose the fault location in a MLID from its output voltage waveform. The proposed neural network utilizes output voltage signals of the MLID to train the neural networks. The acquired data is transformed by using the Fast Fourier Transform technique (FFT) to rate a signal value as an important characteristic [12]. Then, the PCA is performed to reduce the input neural size [13].

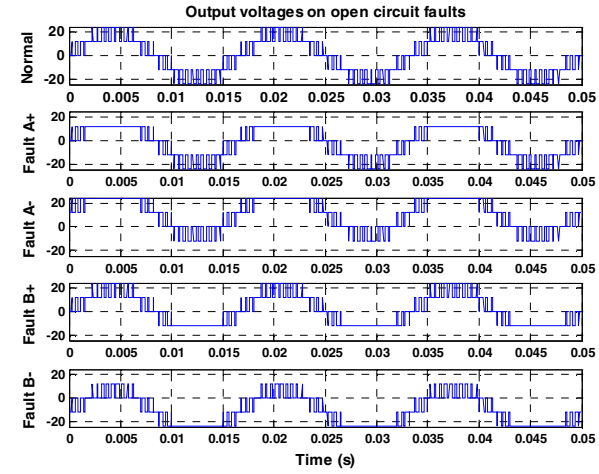
III. Fault Diagnosis Methodology

A. *Structure of Fault Diagnosis System*

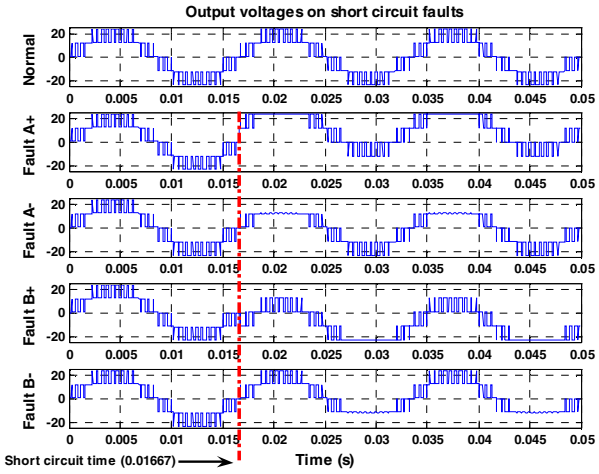
The structure for a fault diagnosis system is illustrated in Fig. 6. The system is composed of four major states: feature extraction, neural network classification, fault diagnosis, and switching pattern calculation with gate signal output. The feature extraction performs the voltage input signal transformation, with rated signal values as important features, and the output of the transformed signal is transferred to the neural network classification. The networks are trained with normal data, all fault feature data, and corresponding output assigned as binary code; thus, the output of this network is nearly 0 and 1 as binary code. The binary code is sent to the fault diagnosis to decode the fault type and its location. Then, the switching pattern is calculated to reconfigure the MLID to bypass and compensate the failed cell.

B. *Feature Extraction System and Principal Component Neural Network*

Simulated and experimental output voltages of a MLID are illustrated in Fig. 3, 4, and 5. As can be seen, the signals are difficult to rate as an important characteristic for classifying a fault hypothesis, and they have high correlation with each other; hence, a signal transformation technique is needed. The comparison of signal transformation suitable to training a neural network for fault diagnosis tools is elucidated in [12]. The fault diagnosis system for a MLID using FFT and neural network are proposed in [14]. The proposed technique has a good classification performance to classify normal and



(a)



(b)

Fig. 5. Simulation of output voltages signals (a) open circuit faults (b) short circuit faults showing fault features at S_{A+}, S_{A-}, S_{B+}, and S_{B-} of H-bridge 2 with modulation index = 0.8 out of 1.0.

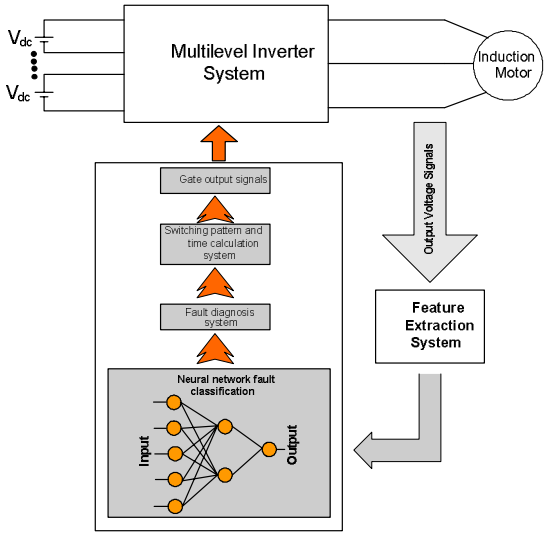


Fig. 6. Structure of fault diagnosis system.

abnormal features. However, many neurons are used to train the network (i.e. one neuron for each harmonic); therefore, PCA can be used to reduce the number of input neurons as illustrated in Fig. 7. PCA is a method used to reduce the dimensionality of an input space without losing a significant amount of information (variability) [15]. The method also makes the transformed vectors orthogonal and uncorrelated. A lower dimensional input space will also usually reduce the time necessary to train a neural network, and the reduced noise (by keeping only valuable PCs) may improve the mapping performance. The comparison in classification performance between the network proposed in [14] and the principal component neural network (PC-NN) is discussed in [16]. The results show that the PC-NN has a better overall classification performance by 5 % points; consequently, the PC-NN is utilized to perform the fault classification in this research.

C. Principal Component Analysis (PCA)

The discussion of PCA presented in this section is brief, providing only indispensable equations to clarify the fundamental PCA approach applied to a fault diagnosis system in a MLID. A distinguished introduction and application of PCA has been provided by [13]. The process of neural network design and the use of principal component analysis for fault diagnosis in a MLID are clearly explained in [14, 16]. Also, PCA technique is possible to implement on floating point DSP for real-time applications as proposed in [17].

The fundamental PCA used in a linear transformation is illustrated in (1). The original data matrix, $\boldsymbol{X}$ of n variables (harmonic orders from FFT) and m observations (different modulation indices of output voltage of a MLID) is transformed to a new set of orthogonal principal components (PC), $\boldsymbol{T}$, of equivalent dimension ($m \times k$) as represented in (2). The transformation is performed such that the direction of first PC is identified to capture the maximum variation of the original data set. The subsequent PCs are associated with the variance of original data set in order; for instance, second PC indicates the second highest variance of the original data set, and likewise.

$$T = XP \tag{1}$$

where:

$\boldsymbol{T}$ is the $m \times k$ score matrix (transformed data)
m = the number of observations
k = dimensionality of the PC space
$\boldsymbol{X}$ is the $m \times n$ data matrix.
m = the number of observations
n = dimensionality of original space
$\boldsymbol{P}$ is the $n \times k$ loadings matrix (PC coordinates)
n = dimensionality of original space
k = number of the PCs kept in the model

Selecting a reduced subset (PCs kept in the model) of PC space results in a reduced dimension structure with respect to the important information available as shown in (3). The objective of PC selection is not only to reduce the dimension structure, but also to keep the valuable components. Normally,

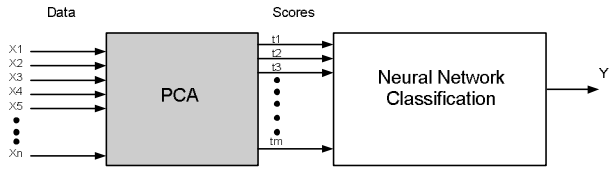


Fig. 7. Principle Component Neural Network.

$$\underset{(m\times k)}{\begin{bmatrix} t_{11} & t_{12} & \cdots & t_{1k} \\ t_{21} & t_{22} & \cdots & t_{2k} \\ \vdots & \vdots & \vdots & \vdots \\ t_{m1} & t_{m2} & \cdots & t_{mk} \end{bmatrix}} = \underset{(m\times n)}{\begin{bmatrix} x_{11} & x_{12} & \cdots & x_{1n} \\ x_{21} & x_{22} & \cdots & x_{2n} \\ \vdots & \vdots & \vdots & \vdots \\ x_{m1} & x_{m2} & \cdots & x_{mn} \end{bmatrix}} * \underset{(n\times k)}{\begin{bmatrix} p_{11} & p_{12} & \cdots & p_{1k} \\ p_{21} & p_{22} & \cdots & p_{2k} \\ \vdots & \vdots & \vdots & \vdots \\ p_{n1} & p_{n2} & \cdots & p_{nk} \end{bmatrix}} \tag{2}$$

$$\underset{(1\times k)}{\begin{bmatrix} t_1 & t_2 & \cdots & t_k \end{bmatrix}} = \underset{(1\times n)}{\begin{bmatrix} x_1 & x_2 & \cdots & x_n \end{bmatrix}} * \underset{(n\times k)}{\begin{bmatrix} p_{11} & p_{12} & \cdots & p_{1k} \\ p_{21} & p_{22} & \cdots & p_{2k} \\ \vdots & \vdots & \vdots & \vdots \\ p_{n1} & p_{n2} & \cdots & p_{nk} \end{bmatrix}} \tag{3}$$

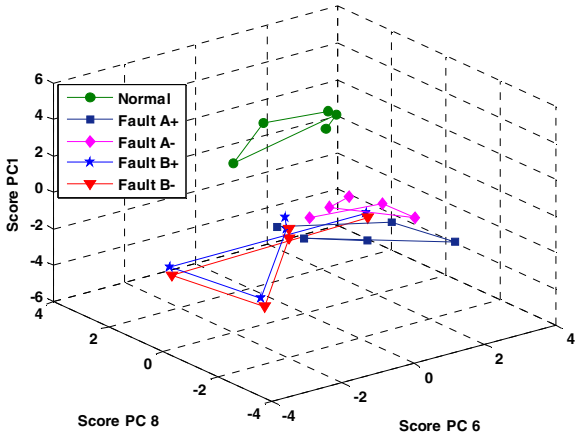
high variance components could contain related information, whereas small variance components that are not retained are expected to contain unrelated information; for instance, measurement noise. It should be noted that the high variance components may not contain the useful information for a classification problem.

PCA can be performed by using MATLAB statistic toolbox as explained in [16]. The example of signal transformation using PCA is shown in Fig. 8. These 3-D plots of PC scores are transformed with training data set used in [16]. We can see that the classification between normal and faults could be a linear problem, whereas the classification among faults is a nonlinear problem. That is why the neural network is applied to solve this problem. By using PCA, the size of input neurons can be reduced from 40 nodes to 5 nodes (i.e. 5 harmonics instead of 40 harmonic components) [16].

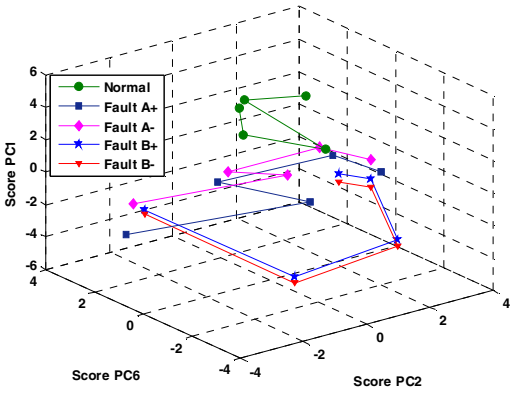
D. Reconfiguration method

The reconfiguration diagram for 11-level MLID with 5 SDCS is illustrated in Fig. 9. It should be noted that multilevel carrier-based sinusoidal PWM is used as shown in Fig. 10. The basic principal of reconfiguration method is to use other cells (H-bridge) to compensate the faulty cell. We know that the turn-on intervals of each cell are not equal with multilevel carrier-based sinusoidal PWM: cell 1 has the longest turn-on interval, then the turn-on interval decreases from cell 2 to cell 5 as staircase PWM waveform. The desired output voltage of a MLID can be achieved by controlling modulation index (m_a).

For instance, if cell 2 has an open circuit fault at S_1 while the MLID operates at m_a = 0.8/1.0 (MLID is operated with four cells (cell 1-4)). We can see from Fig. 9 (b) that S_3 and S_4 need to be turned on, then the gate signal of cell 2 will be shifted up to control cell 3, then the gate signal of cell 3 will shift to cell 4, and the gate signal of cell 4 will shift to cell 5 respectively. This reconfiguration also applies to other phases of MLID in order to maintain balanced output voltage. By using this method, the operation of MLID from 0.0 to 0.8 (out of 1) can



(a)



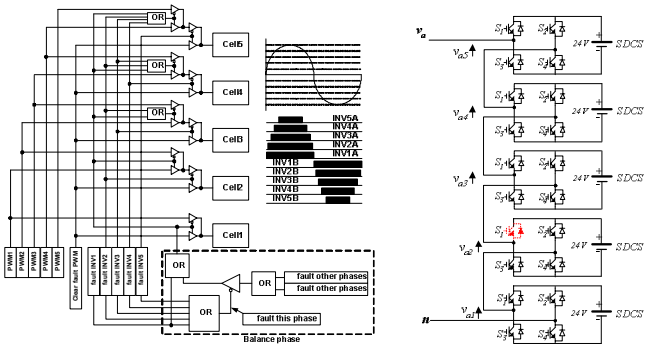
(b)

Fig. 8. The 3-D plots of PC scores; (a) score on PC 6, 8, 1, (b) score on PC 2, 6, 1.

be compensated such that the inverter will continue to function like normal operation; however, if MLID operates at $m_a > 0.9$, the lower order harmonic will occur since the MLID will operate at over modulation region in order to try to continue to output the full requested voltage as illustrated in Fig. 10. To solve this problem, space vector, and third harmonic injection PWM schemes may be used. Also, a redundant cell can be added into the MLID, but the additional part count should be considered. Therefore, if the fault types and location can be detected, the continuous operation can be achieved.

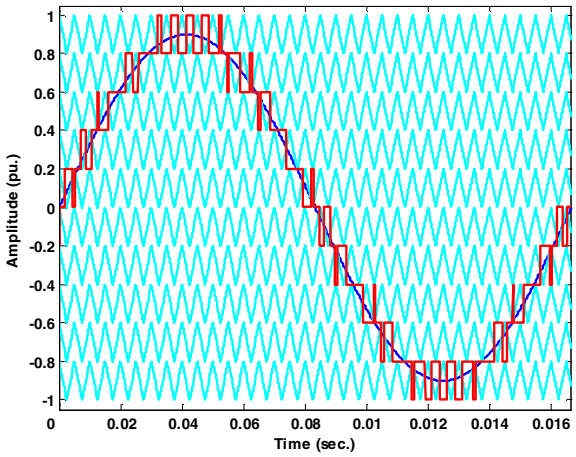
IV. Reconfiguration Effects and Limitations

The proposed reconfiguration technique is very simple to implement because the proposed technique is based on digital logic gate: a simple AND gate and OR gate can be implemented to this reconfiguration method. Unfortunately, the configuration method has a limitation. Table I represents the maximum output phase voltage available of a MLID with 5 SDCS of 24 V/cell. As can be seen, the MLID can only operate at 50% of maximum m_a (1.0) if the MLID has two faulty cells. This means that MLID can drive the traction motor only at half load condition, although the MLID operates

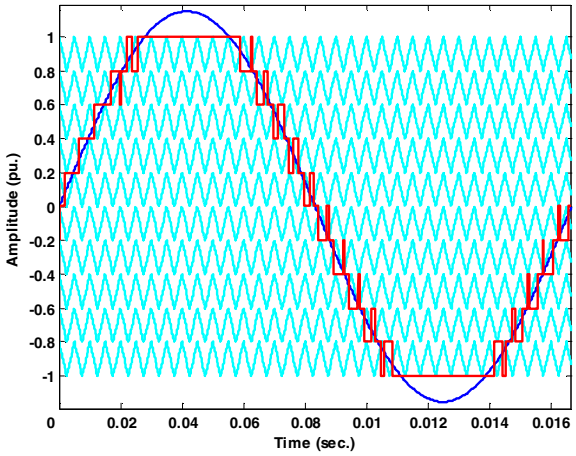


(a) (b)

Fig. 9. (a) Reconfiguration diagram, (b) H-Bridge 2 Switch S_1 open circuit fault at second level of single-phase multilevel-inverter with 5SDCS.



(a)



(b)

Fig. 10. Multilevel carrier-based sinusoidal PWM with 2 kHz switching frequency for 5 SDCS MLID showing carrier bands, modulation waveform, and inverter output waveform (a) $m_a = 0.9/1.0$, (b) $m_a = 1.2/1.0$

in staircase mode. Nevertheless, the MLID can drive at full load condition at staircase mode if MLID has only one faulty cell. The amount of reduction in capacity that can be tolerated depends upon the application; however, in most cases a

TABLE I
MAXIMUM OUTPUT PHASE VOLTAGE AVAILABLE OF A MLID WITH 5 SDCS OF 24V/CELL

Number of faulty cells	*Maximum m_a can be compensated*	Fundamental component of Output phase voltage available, $V_{an,1}$ *(rms)*
1	1.0144	85.98 V
2	0.7624	64.42 V
3	0.5062	42.92 V
4	0.2525	21.40 V

TABLE II
COMPARISON BETWEEN NORMAL AND FAULTY OPERATION OF A MLID WITH 5 SDCS OF 24 V/CELL

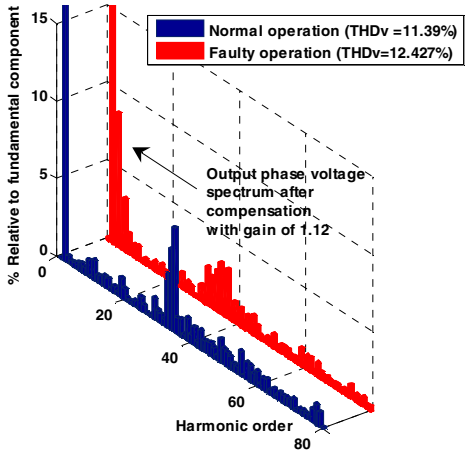
Modulation index at an operating point	*Operating condition*	*Fundamental component of output phase voltage, $V_{an,1}$ (rms)*	*Compensated gain*	*THD_V (%)*
0.9/1.0	Normal	76.28 V	1	11.39%
	One faulty cell	76.28 V	1.12	12.43%
1.0/1.0	Normal	84.88 V	1	9.26%
	One faulty cell	84.88 V	2.47	31.97%

reduction in capacity is more preferable than a complete shutdown.

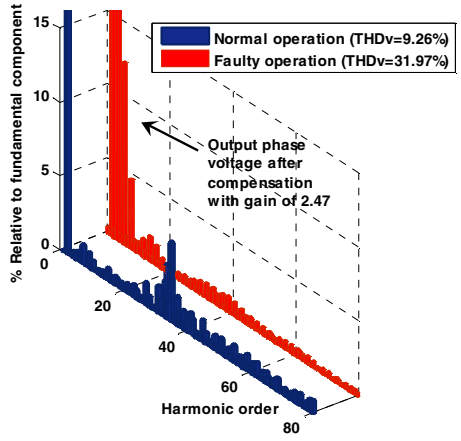
In the case of one faulty cell, the proposed reconfiguration can compensate at m_a from 0.0 to 0.8 (out of 1) such that the inverter will continue to function like normal operation. However, if the MLID operates at $m_a > 0.9$, the output voltage harmonic distortion (THD_V) is higher because of additional lower harmonics when the converter is operated in overmodulation after reconfiguration. The MLID will operate at over modulation region or staircase mode because the compensated gain is needed to keep the full requested output voltage. Table II shows the comparison between normal and faulty operation of the MLID. We can see that the THD_V increases more than 4 times of normal operation at $m_a = 1.0$, whereas the THD_V slightly increases (about 1%) when MLID operates at $m_a = 0.9$. The reconfiguration effects on THD_V are also shown in Fig. 11. A study suggests that space vector and third harmonic injection PWM schemes may be used because those PWM schemes can operate at higher m_a (1.15) before overmodulation. Additionally, a redundant cell can be added into the MLID; however, the tradeoff between reconfiguration effects and the additional part count should be considered.

V. EXPERIMENTAL VALIDATION

The experiment setup is represented in Fig. 12. A three-phase wye-connected cascaded multilevel inverter using 100 V, 70 A MOSFETs as the switching devices is used to produce the output voltage signals. The MLID supplies an induction motor (1/3 hp) coupled with a dc generator (1/3 hp) as a load of the induction motor. The Opal RT-Lab system is utilized to generate gate drive signals and interfaces with the gate drive board. The switching angles are calculated by using Simulink based on multilevel carrier-based sinusoidal PWM.



(a)



(b)

Fig. 11. Reconfiguration effects at over modulation index (a) normal operation $m_a = 0.9/1.0$, (b) normal operation $m_a = 1.0/1.0$

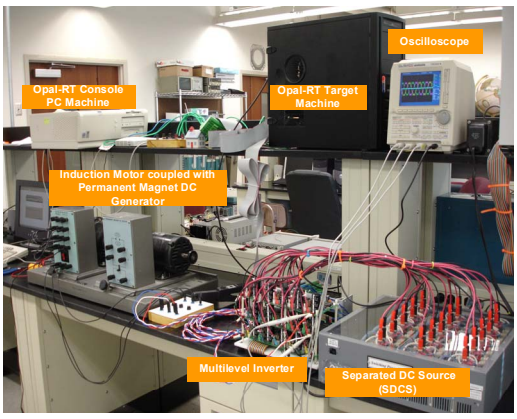
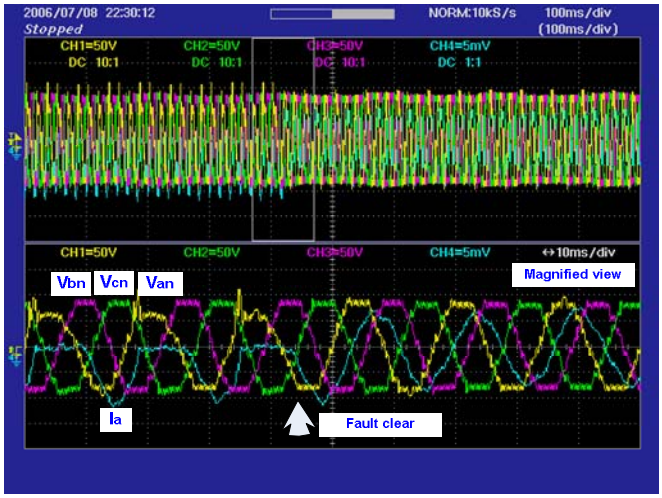


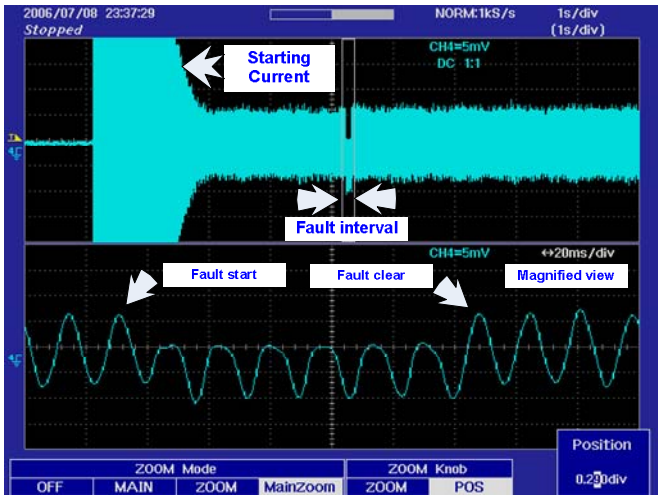
Fig. 12. Experiment set-up.

A separate individual 24-volt SDCS is supplied to each cell of the MLID, consisting of 5 cells per phase as shown in Fig. 9(b).

The experimental results of the open circuit fault at S_1 in cell 2 on phase *a*, while the MLID is operated at $m_a = 0.8/1.0$ are represented in Fig. 13. Fault occurrence is created by



(a)



(b)

Fig. 13. Experiment results of the open circuit fault at S_1 ,cell 2 of the MLID during operated at m_a = 0.8/1.0 (a) Output phase voltages and line current (I_a), (b) line current (I_a) showing starting current, fault interval, and fault clear.

physically removing the switch in the desired position. We can see that the output voltage (V_{an}) of the MLID is unbalanced during the fault interval. Fig. 13 (b) shows that the proposed system utilizes about 6 cycles to clear the fault. The clearing time can be shorter than this if the proposed system is implemented as a single chip using an FPGA or DSP. The Opal-RT system needs a few cycles to load the output voltage signals from the target machine to console PC machine via Ethernet. In addition, the window of FFT function requires at least a cycle to perform signal transformation. However, the cascaded MLID can tolerate a few cycles of faults, the proposed system can detect the fault and can correctly reconfigure the MLID; therefore, the results are satisfactory.

VI. Conclusion

The fault diagnosis and reconfiguration system in a MLID using a principal component neural network have been proposed. The output phase voltage of a MLID can be used to diagnose the faults and their locations. A neural network and a principal component analysis can be applied as diagnostic techniques in a MLID. The proposed reconfiguration technique is very simple to implement because the proposed technique is based on a basic digital logic gate. The limitations and effects of the proposed reconfiguration method have also been addressed. The proposed system utilizes about 6 cycles to clear the fault. The experimental results show that the proposed diagnosis and reconfiguration system performs satisfactorily to detect the fault type, fault location, and reconfiguration.

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