

Characterization of a High Temperature Multichip SiC JFET-Based Module

Fan Xu, Dong Jiang, Jing Wang, Fred Wang, Leon M. Tolbert
Department of Electrical Engineering and Computer Science
The University of Tennessee
Knoxville, TN 37996-2100, USA
fxu6@utk.edu

Timothy J. Han, Sung Joon Kim
Global Power Electronics, Inc.
Irvine, CA 92618, USA
jhhan@gpe-energy.com

Abstract—This paper presents a SiC JFET-based, 200 °C, 50 kW three-phase inverter module and evaluates its electrical performance. With 1200 V, 100 A rating of the module, each switching element is composed of four paralleled SiC JFETs with two anti-parallel SiC Schottky Barrier Diodes (SBDs). The substrate layout inside the module is designed to reduce package parasitics. Then, experimental static characteristics of the module are obtained over a wide range of temperature, and low on-state resistance is shown up to 200 °C. The dynamic performance of this module is evaluated by double pulse test up to 150 °C, under 650 V dc bus voltage and 60 A drain current, with different turn-on and turn-off gate resistances. The current unbalance phenomenon and phase-leg shoot-through problem are analyzed too. The results by simulation and experiments show that the causes of shoot-through are JFET inside parameters, package parasitics, and high temperature. The switching losses of this module at different temperatures are shown at the end.

I. INTRODUCTION

With the increasing demand for high frequency, high power and high temperature applications, SiC power semiconductors have been expected to replace conventional Si-based power switching devices due to their attractive properties such as high breakdown voltage, fast switching, low power losses, and high temperature tolerance. Meanwhile, SiC has a higher thermal conductivity, which leads to important benefits for power dissipation and higher power handling capability. Research on SiC power devices has revealed their better efficiency compared to Si power devices due to the reduction in both conduction and switching losses [1-3]. Furthermore, with high temperature packaging, the high temperature capability of SiC power devices can be utilized [4].

References [5-7] discuss the structure of the SiC JFET in detail. The modeling and characterization of SiC JFETs, and their system applications have been reported in several papers [7-13]. Several SiC JFET and SiC diode based power modules have been presented [14-16]. In high power applications, power devices are often used in parallel in order

to achieve a higher current rating. The performance of the individual SiC JFET during paralleling operation in the module has been studied in [17]. A SiC JFET and SiC Schottky Barrier Diode (SBD) based phase-leg power module has been developed at 200 °C and used in a 18 kW three-phase inverter system in [16]. Reference [18] describes a 250 °C SiC power module containing eight SiC MOSFETs in parallel per switching element. For the package parasitics, their effects on switching speed and losses are discussed in [19-21]. The impact of source parasitic inductance on shoot-through performance is presented in [22].

This paper presents a SiC JFET-based, 200 °C, 50 kW three-phase multichip inverter module and evaluates its electrical performance. The static characteristics of this module are tested up to 200 °C, and the dynamic performance of it is evaluated over a wide temperature range, from 25 °C to 150 °C, under 650 V dc bus voltage and 60 A drain current. Current unbalance phenomenon is shown and improved. The SiC JFET inside capacitors, temperature, gate loop, and DC bus parasitic inductances impacts on phase-leg shoot-through problems are discussed.

This paper starts with the description of the module in Section II. The static characteristics of it are presented in Section III. The switching characteristics of this module, including gate drive design, test results, the analysis of current unbalance and phase-leg shoot-through, are provided in Section IV. The final conclusions are given in the last section.

II. MULTICHIP SiC JFET MODULE OVERVIEW

The authors have developed a SiC JFET-based, 200 °C, 50 kW three-phase inverter module with 1200 V, 100 A power rating, in order to meet the requirements of high power, high temperature and high efficiency applications such as AC motor control, motion/servo control, UPS, and photovoltaic systems. Fig. 1 shows the structure of the module. Each switching element in the module consists of four 4.17 mm x 4.17 mm normally-on SiC JFETs (1200 V/25 A each) with two 2.7 mm x 2.7 mm anti-parallel SiC

SBDs. All devices are from SiCED [23]. The JFETs have a nominal pinch-off voltage of -17 V and gate breakdown voltage of -25 V . The maximum junction temperature is designed to be $200\text{ }^\circ\text{C}$. Fig. 2 shows the circuit of a phase-leg, and the package layout of the phase-leg is shown in Fig. 3. Devices in the natural current commutation path are put close in order to reduce the package parasitics.

Three substrates are prepared for the module, and each substrate forms a single phase, as shown in Fig. 1. Ceramic gate substrates with thin film metal are soldered on the direct bond copper (DBC) on Si_3N_4 substrate. SiC dies are soldered to the substrate. All switching components and interconnects are isolated from the heat sink base plate. Two copper pins for control contacts are used to reduce package parasitics. SiC dies and busbars are wire bonded using 5 mil and 8 mil aluminum wires, respectively.

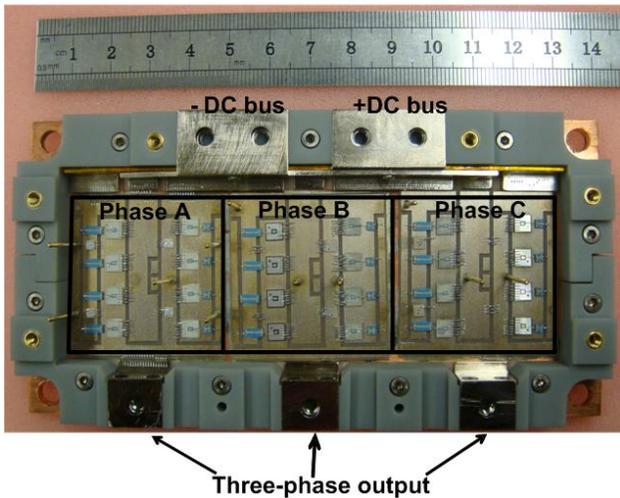


Fig. 1. Three-phase inverter module layout.

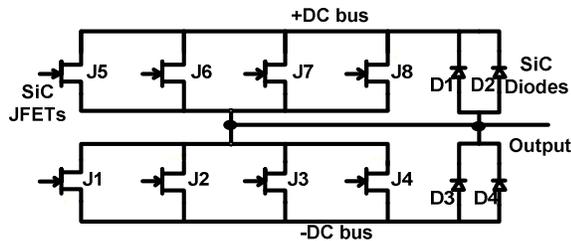


Fig. 2. Phase-leg circuit.

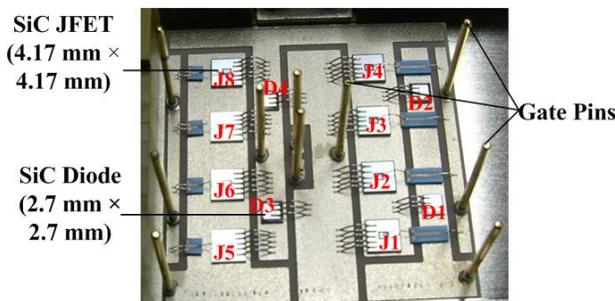


Fig. 3. Phase-leg package layout.

III. STATIC CHARACTERIZATION

The on-state resistance of the JFET measurement is based on the slope of the forward characteristic in the linear region. The forward characteristic of the four paralleled SiC JFETs in a phase-leg in the module is obtained at different temperatures from $25\text{ }^\circ\text{C}$ to $200\text{ }^\circ\text{C}$, as shown in Fig. 4. The forward characteristic of JFETs in Fig. 4 is obtained at the gate-source voltage of 0 V since they are normally-on devices. Fig. 5 to Fig. 7 show the SiC JFET phase-leg forward characteristic at different gate-source voltages (V_{gs}) at $25\text{ }^\circ\text{C}$, $125\text{ }^\circ\text{C}$, and $200\text{ }^\circ\text{C}$, respectively. Fig. 8 shows the on-state resistance changes over a temperature range from $25\text{ }^\circ\text{C}$ to $200\text{ }^\circ\text{C}$, at 0 V gate-source voltage. From Fig. 8, the on-state resistance of the four paralleled SiC JFETs in the module increases with higher temperature, from $25\text{ m}\Omega$ at $25\text{ }^\circ\text{C}$ to $55\text{ m}\Omega$ at $200\text{ }^\circ\text{C}$. Compared to a Si based power module, the on-state resistance values and the variation with temperature are smaller. In addition, the SiC devices can run at higher temperatures. Thus, the SiC based power module is more efficient in terms of conduction loss.

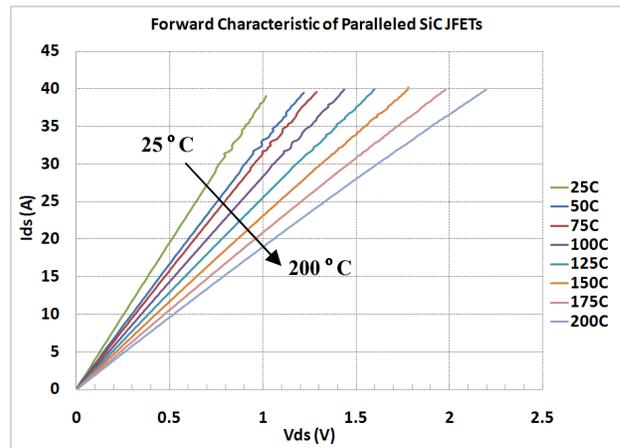


Fig. 4. Forward characteristic of four paralleled SiC JFETs in the module.

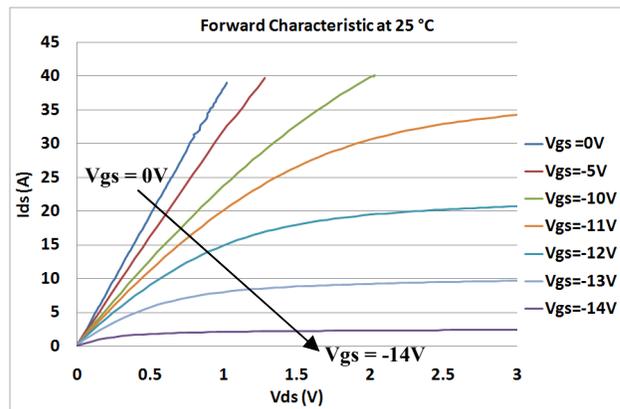


Fig. 5. Module's four paralleled SiC JFETs' forward characteristic with different gate-source voltage at $25\text{ }^\circ\text{C}$.

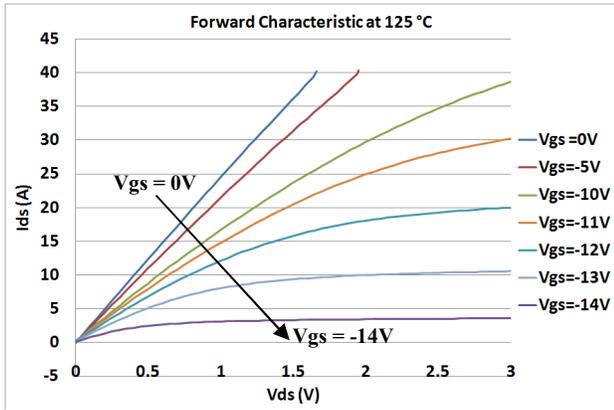


Fig. 6. Module's four paralleled SiC JFETs' forward characteristic with different gate-source voltage at 125 °C.

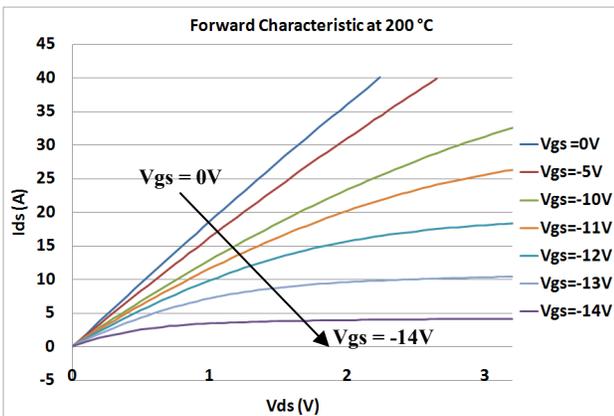


Fig. 7. Module's four paralleled SiC JFETs' forward characteristic with different gate-source voltage at 200 °C.

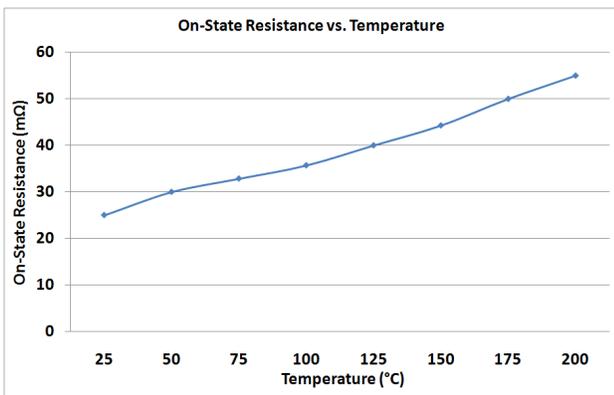


Fig. 8. On-state resistance of four paralleled SiC JFETs in the module.

Fig. 9 shows the forward characteristic of the two paralleled SiC SBDs. Since the diode conduction equivalent circuit is made up of a voltage source and a resistance R_D in series, the voltage source value is the threshold voltage value, and R_D represents the equivalent resistance of the diode when it conducts. From Fig. 9, the R_D of two paralleled SiC SBDs in the module also increases with increasing temperature. However, the threshold voltage of the SBDs decreases when the temperature increases.

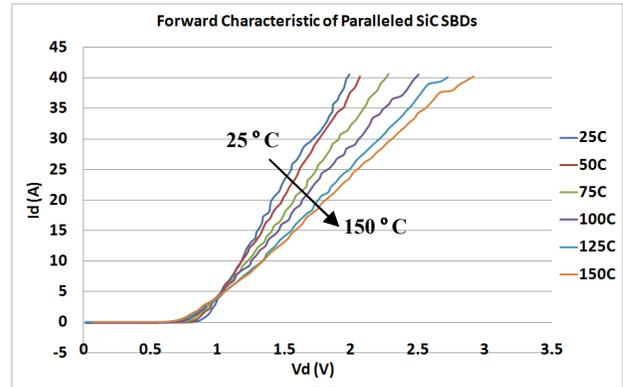


Fig. 9. Forward characteristic of two paralleled SiC SBDs in the module.

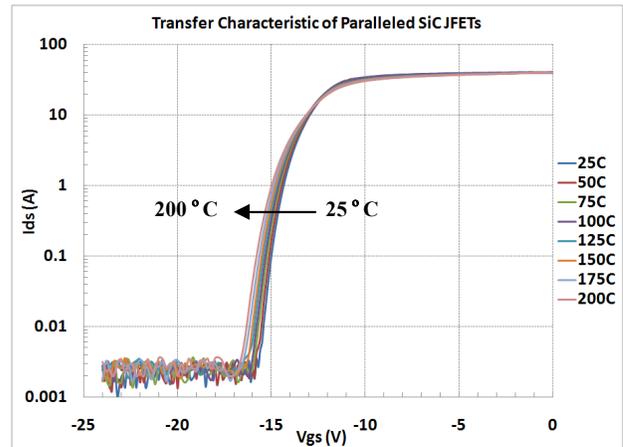


Fig. 10. Transfer characteristic of four paralleled SiC JFETs in the module.

Fig. 10 shows the transfer characteristic of the four paralleled SiC JFETs at different temperatures. Since the SiC JFETs are normally-on devices, the pinch-off voltage is negative. From Fig. 10, the pinch-off voltage decreases about 1 V with the temperature increasing from 25 °C to 200 °C.

IV. DYNAMIC CHARACTERIZATION AND DISCUSSION

The static characteristic data are not enough for inverter design and operation. The phase-leg switching behaviors of the multichip SiC JFET-based power module are tested with double pulse under 1 mH inductor load, at 650 V dc bus voltage, 60 A drain current. The package parasitics of the module are extracted by Maxwell Q3D parameter extractor. Using Saber circuit simulator, a detailed circuit simulation was conducted. The experiments are done at 150 °C.

A. Gate Drive Design

Fig. 11 shows the double pulse test (DPT) circuit with gate drive schematic. Both high side and low side switching elements are four paralleled SiC JFETs with two anti-parallel SiC SBDs, and they consist of a phase-leg in the module. In the test, the four high side JFETs are off, and the double pulse signal is applied to four low side JFET gate terminals.

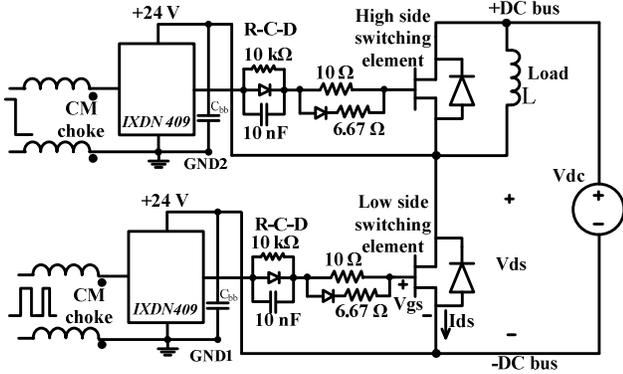


Fig. 11. Double pulse test circuit with gate drive schematic for phase-leg in SiC JFET-based module.

Considering JFET pinch-off and breakdown voltage values, and their variation in four paralleled JFETs, 0 V is chosen for turn-on and -24 V is used for turn-off. A 10 k Ω resistor and a 10 nF capacitor are used in a RCD network, which will limit avalanche current and supply high gate current peaks [7]. Gate resistances are chosen differently for turn-on and turn-off transients. In the test, for four paralleled JFETs, turn-on resistance is 4 Ω and turn-off resistance is 10 Ω , which can aid fast switching while avoiding shoot-through caused by high dv/dt . Also, a common mode (CM) choke is used to reduce the CM current induced by fast switching which will impair the switching waveform measurement, and the two isolated gate signals are sent to the input side of the CM choke.

The driver IC is IXDN409, which is based on PMOS-NMOS totem-pole structure. A 0.1 Ω coaxial shunt resistor is used to measure the drain current I_{ds} with little parasitic inductance's influence. Probe Tip Adapter (PTA) is used to measure the gate-source voltage V_{gs} . BNC is used to measure drain-source voltage V_{ds} . The shunt, PTA, and BNC share the same ground; a non-differential probe is used for the three measurements in the switching period with minimum distortion from the real curves.

For phase-leg test, shoot-through protection is needed, especially for a phase-leg with normally-on JFETs. In the test, the shoot-through protection of the phase-leg is realized by an IGBT which is series connected in +DC bus. It is driven by a current-sensing single-channel drive (IR2127). Once the current exceeds the limitation, the IGBT will be turned off to separate the phase-leg from DC power supply and protect the module.

B. Current Unbalance and Module Layout Improvement

The package parasitics significantly influence the module switching performance, especially in a high temperature multichip power module. The module package parasitic values are obtained by Maxwell Q3D parameter extractor. The simulation circuit in Saber is a phase-leg of the module with package parasitics. Since mutual parasitic inductances are less than 1/10 of self parasitic inductances, they are all neglected in the simulation.

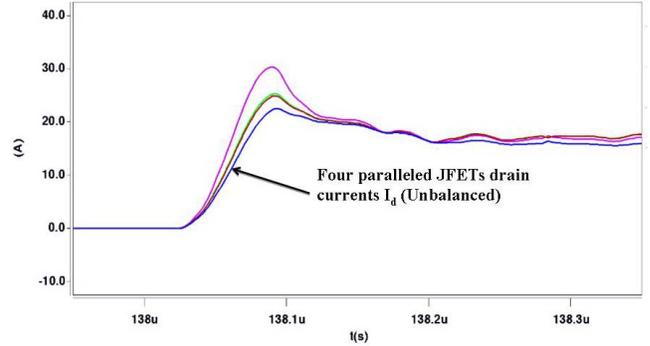


Fig. 12. Unbalanced current during turn-on transient in simulation.

In a multichip power module, current unbalance happens due to the parameter variation of each device and different package parasitics in each device loop. In the simulation, all SiC JFET models are the same, the current unbalance comes from the different package parasitics in each JFET loop (drain side, source side and gate drive parasitics of each JFET), as Fig. 12 shows. The current unbalance will lead to power loss and corresponding thermal stress differences among the paralleled devices [24].

The gate circuit layout of a power module is important regarding transient current unbalance [25]. In this SiC JFET-based multichip power module, the gate loop inductances of four paralleled JFETs are 36, 27, 27, 36 nH respectively if only one gate pin is put in the middle of the four JFETs, as shown in Fig. 13. Longer distance from gate pin to farthest JFETs leads to larger inductance in their gate loops. However, if two gate pins are put in between two closer JFETs to make the distance evenly distributed among four JFETs, their gate loop inductances will all be balanced to be 27 nH, as Fig. 14 shows. The gate loop parasitic inductances of the 1st and 4th JFETs are reduced and parasitic unbalance is improved too. Since different charge/discharge rate of JFET inner capacitors can be achieved by adjusting external gate resistors (R_g), different R_g can be applied to balance the currents. Decreasing R_g will speed up the switching transient. Meanwhile, increasing R_g will prolong the switching transient. Fig. 15 shows the waveforms of four paralleled SiC JFETs drain currents during turn-on transient, after current balancing using the resistances of 24 Ω , 21 Ω , 19 Ω , and 17.5 Ω , respectively.

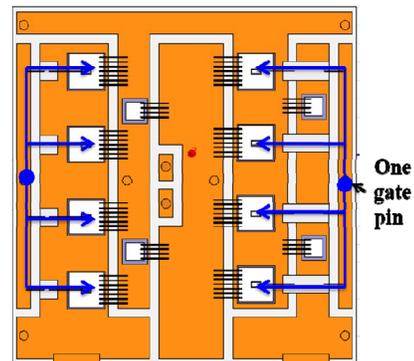


Fig. 13. One gate pin layout.

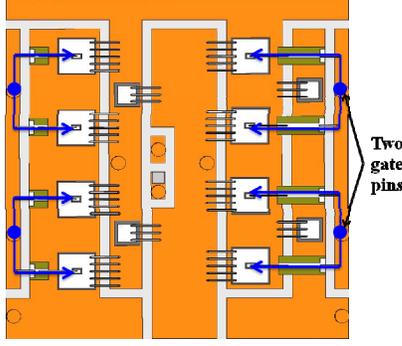


Fig. 14. Two gate pins layout.

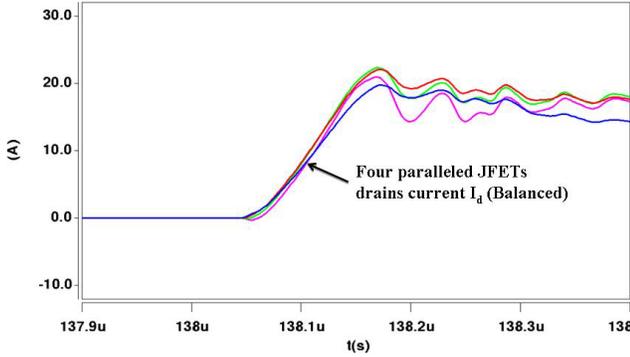


Fig. 15. Balanced current during turn-on transient in simulation.

C. Shoot-Through During Phase-Leg Commutation

1) JFET inside capacitor impact

Shoot-through is defined as both high side and low side switches in a phase-leg being turned on at the same time. It will cause additional power dissipation in the switching devices, increase losses [22], or even damage devices. Shoot-through is mainly caused by high dv/dt during a switching transient.

The structure of SiC JFET leads to the existence of intrinsic capacitors between device terminals, as shown in Fig. 16. These JFET intrinsic capacitors are a crucial factor in determining the switching speed. For a normally-on JFET, the capacitor C_{gs} is charged during turn-on transient, and the device will be turned on after the voltage across C_{gs} , V_{gs} , exceeds the pinch-off voltage. During turn-off transient, C_{gs} will discharge to reduce V_{gs} and the device will be turned off. The JFET drain and source terminal voltages vary when other switches are turning on and off. That will charge or discharge JFET inside capacitors due to dv/dt . As a result, V_{gs} varies, which may result in avalanche (V_{gs} exceeding JFET breakdown voltage) or shoot-through.

2) Package parasitic impact

The existence of package parasitics also impacts phase-leg switching behaviors and can cause shoot-through. According to simulation, voltage across the gate loop inductances (gate pins, DBC, wirebonds connecting gate pads on JFET dies to DBC) and DC bus inductances are major causes of V_{gs} exceeding JFET pinch-off voltage.

During bottom JFETs turning on, the voltage of phase-leg output terminal drops from 650 V to 0 V, and current i_g appears in top JFETs' gate loops due to dv/dt , $i_g = i_{gs} - i_{dg}$ (i_{gs} and i_{dg} are currents flowing through C_{gs} and C_{dg}), as Fig. 16 shows. In Fig. 17, i_g is negative which means that it flows from the device to the gate voltage source. When $|i_g|$ increases, the voltage across parasitic inductance V_L is negative. Since $V_{gs} = V_s - V_L$, it is possible that $V_{gs} > -17$ V if V_L is large enough ($V_s = -24$ V in simulation). Because $V_L = L_g(di_g/dt)$ (L_g is the parasitic inductance in the gate loop), small L will lead to small V_L and help to avoid shoot-through.

In addition, when the voltage of the phase-leg output terminal drops from 650 V to 0 V, the JFET inside capacitors are charged by DC voltage through the DC bus. When the current i_{bus} begins to decrease, the voltage across bus parasitic inductance V_{bus} is negative ($V_{bus} = L_{bus}(di_{bus}/dt)$, and L_{bus} is the parasitic inductance on DC bus), as Fig. 18 shows. V_{bus} makes the high side JFETs drain side voltage higher than DC voltage. Gate voltage will be increased too, and shoot-through may happen. If the gate loop and DC bus parasitic inductances are large enough to cause shoot-through, the switching transient needs to be slowed down in order to reduce dv/dt , which in turn results in longer turn-on time and higher turn-on loss.

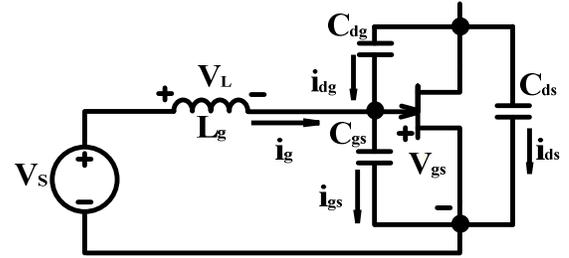


Fig. 16. JFET inside capacitors with gate loop parasitic inductance.

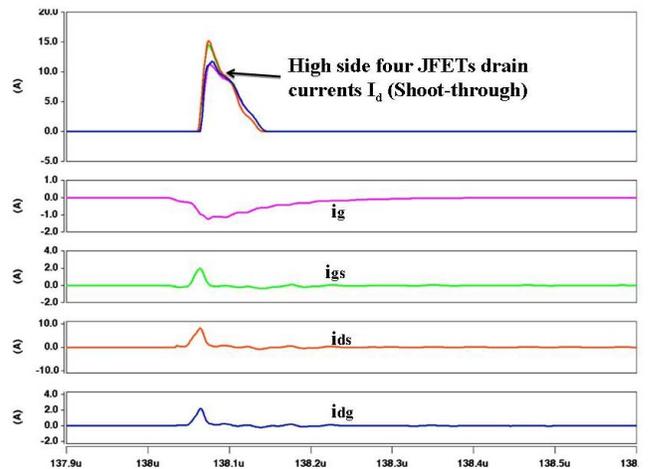


Fig. 17. High side JFETs currents during low side JFETs turning on.

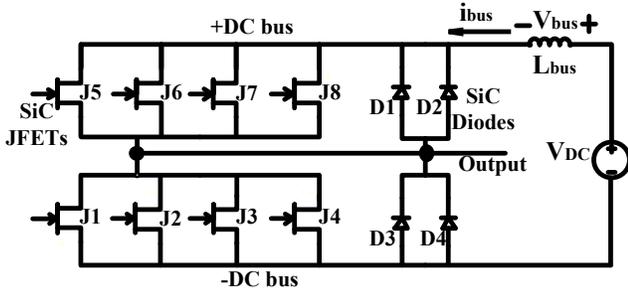


Fig. 18. Phase-leg with DC bus parasitic inductance.

3) Temperature impact

Temperature is another important factor for phase-leg shoot-through. Figs. 19 to Fig. 21 are the double pulse test waveforms at 25 °C, 100 °C and 150 °C, respectively. At 25 °C, the low side JFET drain current increases from 0 A gradually to charge the load. However, this current makes a step change to 6 A at the beginning of the charging, when the temperature increases to 100 °C. This phenomenon occurs when the high side JFETs are turned on and the current flows through both high side and low side JFETs in a phase-leg, since the current of the load inductor cannot make a step change. Checking the high side JFETs gate voltage V_{gs} , it is -15 V and exceeds the pinch-off voltage. The high side JFETs' V_{gs} is -13 V at 150 °C, and the low side JFETs' drain current jumps to 16 A at this time, which means the shoot-through is more serious.

From above, inside capacitors, package parasitics, and operation temperature are all factors for shoot-through happening. For a power module, high temperature will reduce its operation stability. Since SiC-JFET based power modules can often operate at higher temperatures compared to Si based modules, it is more important to reduce their package parasitics in order to keep their operation stability. Once shoot-through happens, it has to be avoided by slowing down the switching speed.

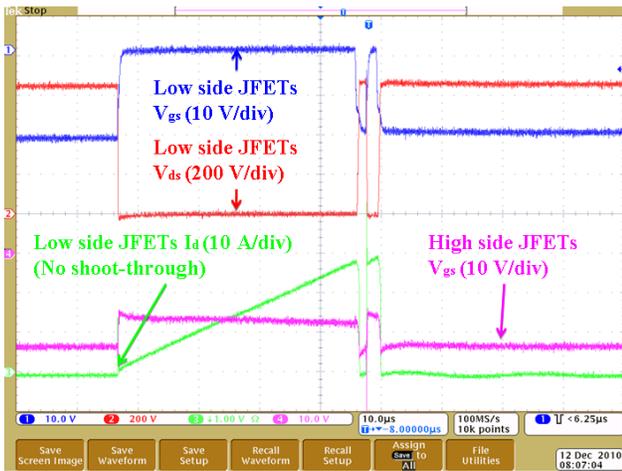


Fig. 19. Double pulse test waveforms at 25 °C.

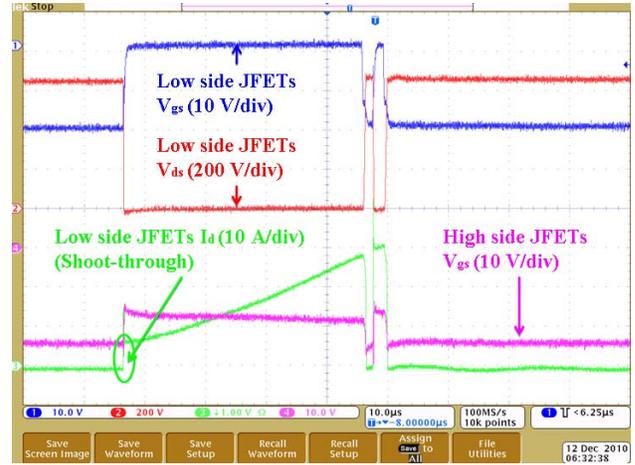


Fig. 20. Double pulse test waveforms at 100 °C.

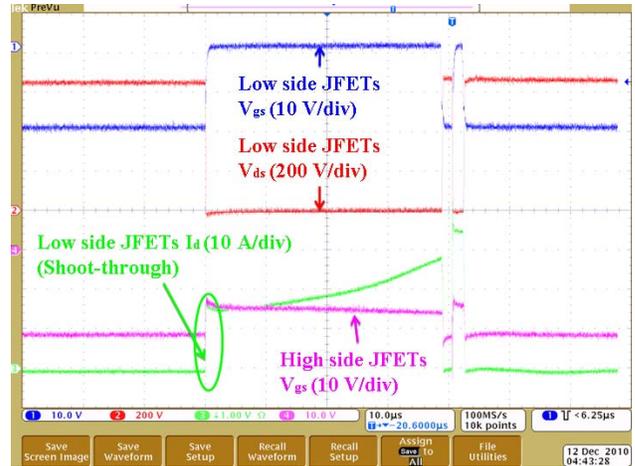


Fig. 21. Double pulse test waveforms at 150 °C.

D. Switching Test

The double pulse test is done under 650 V dc bus voltage, 60 A load current and 150 °C junction temperature. Fig. 22 shows the photo of the high temperature testing setup. The module is heated by connecting to hot plate on the bottom side of the test board. The temperature is monitored by thermocouple.

Fig. 23 and Fig. 24 are experimental waveforms of turn-on and turn-off, respectively. The turn-on overshoot current is small even at high temperature (18 A above the average current) due to the freewheeling SiC SBDs, which have no reverse recovery. Thus, the switching power losses will be reduced.

Table I lists switching time and loss obtained from simulation and experiments at 150 °C. From the results, it is obvious that this SiC JFETs and SiC SBDs based, high power, multichip, three-phase inverter module can be operated at fast switching and low switching losses at high temperature. Fig. 25 and Fig. 26 show the switching power losses as a function of four paralleled JFETs total drain current at different temperatures, under 650 V DC bus voltage. With the temperature increasing, the switching

losses decrease a little bit. The switching loss differences become larger at higher drain current values.

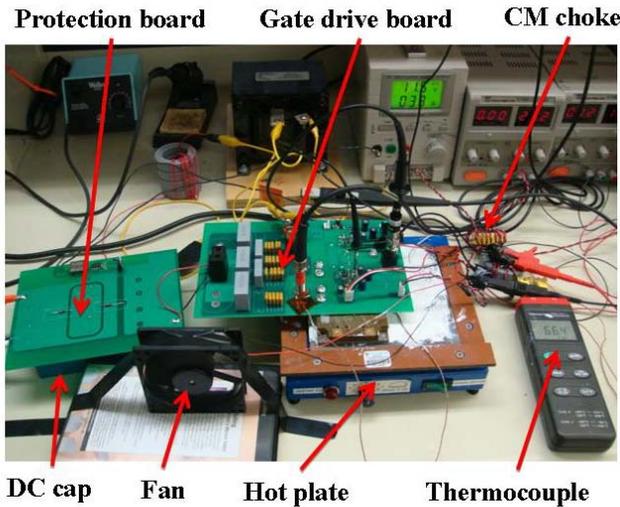


Fig. 22. High temperature switching test setup.

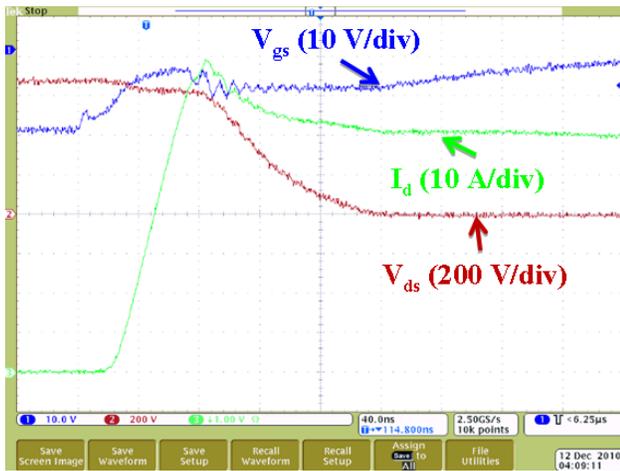


Fig. 23. Experimental turn-on waveforms at 150 °C.

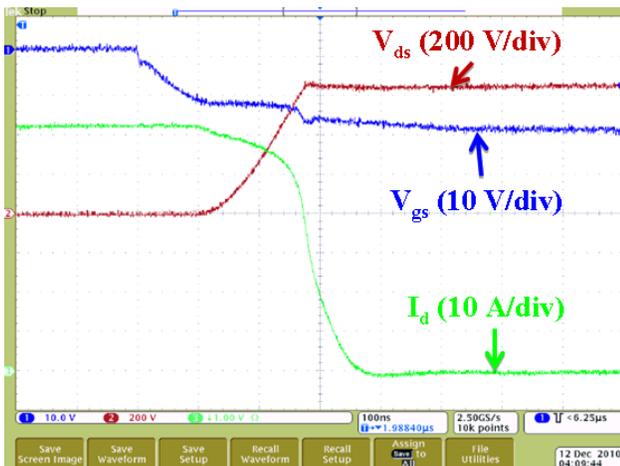


Fig. 24. Experimental turn-off waveforms at 150 °C.

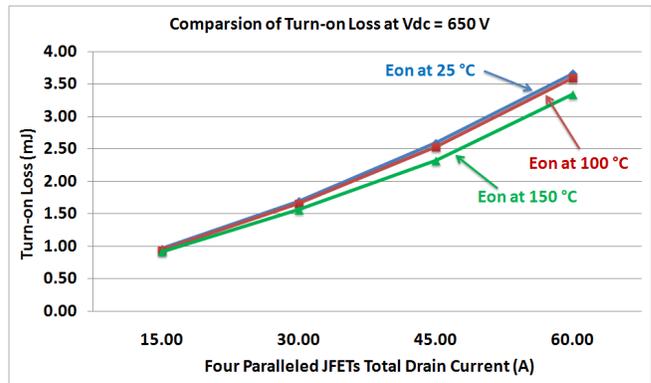


Fig. 25. Turn-on loss as a function of drain current at different temperatures.

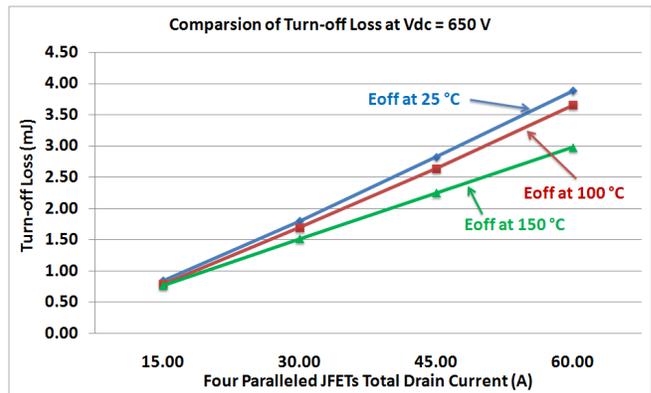


Fig. 26. Turn-off loss as a function of drain current at different temperatures.

TABLE I. SWITCHING TIME AND LOSSES OF FOUR PARALLELED JFETS IN THE MODULE AT 150 ° C

	Simulation Results	Experimental Result
Turn-on Time (ns)	130	140
Turn-on Loss (mJ)	2.85	3.34
Turn-off Time (ns)	140	170
Turn-off Loss (mJ)	2.53	2.89

V. CONCLUSIONS

A SiC JFET-based, 50 kW, multichip, three-phase inverter power module with high temperature packaging (200 °C) is designed and demonstrated. Each switching element consists of four paralleled normally-on SiC JFETs with two anti-parallel SiC SBDs. Short natural current commutation path and two gate control pins are designed to reduce package parasitics. The module static characteristics are tested up to 200 °C. The results exhibit the on-state resistance of the phase-leg is 55 mΩ at 200 °C. The switching performance is evaluated by double pulse test up to 150 °C, under 650 V dc bus voltage and 60 A load current. The 4 Ω turn-on resistance and 10 Ω turn-off resistance are used to improve its switching characteristics at high temperature.

For the multichip power module, the current unbalance phenomenon is shown. Module layout is improved by balancing gate loop parasitics, in order to balance currents. The effects of low side JFETs switching on high side JFETs

are discussed. The causes of shoot-through, including JFET inside parameters, package parasitics and temperature, are analyzed through both simulation and experiments. The key parasitics leading to shoot-through include gate loop parasitic inductance and DC bus parasitic inductance. High temperature will also make shoot-through occur more readily and reduce the operation stability of a SiC JFET-based power module.

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