Design, Modeling, and Characterization of Power MOSFET in 4H-SiC for Extreme Environment Applications

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Abstract: *Silicon Carbide (SiC) is an emerging technology for extreme environment electronics applications. In this paper, an analytical model for vertical DIMOS transistor structure in SiC is presented. The model takes into account the various short channel effects in the DIMOS channel region as well as the velocity saturation effect in the drift region. A good agreement between the analytical model and the MEDICI simulation is demonstrated. A rigorous testing and characterization has been carried out on a 4H-SiC DIMOS transistor test device. Device performance at higher temperatures is investigated. A large change in drain currents and threshold voltage are observed.*

Keywords: Silicon Carbide, DIMOS, Modeling, Characterization, Parameters extraction.

Introduction

Demand for extreme environment electronics increasing day by day and emergence of silicon carbide enhanced the development of the electronics for extreme environment. Among the wide band gap materials, silicon carbide (SiC) has received increased attention because of its potential for a wide variety of high power and high temperature applications [1-4]. It has a high electric breakdown field ($3.5x10^6$ V/cm), high electron saturated drift velocity ($2x10^7$ cm/sec), high melting point (2830 ^oC), and high thermal conductivity (4.9 W/cm-°K) that give it a great potential for extreme environment device applications. SiC is the most advanced one in the context of better quality material growth, defect-free dielectric formation, implantation doping, contacts via metallization, and other process steps.

Power MOSFETs are often used as switching devices in power electronics, power systems, traction drives, and hybrid electric vehicle (HEV) applications. Although there is no commercially available power MOSFET in SiC material, Cree has demonstrated various switching devices in SiC [5]. A group from Purdue University proposed a DIMOS in 6H-SiC with a breakdown voltage of 760V [6]. Presently, most of the research effort in SiC is on the design and fabrication of power MOSFETs. However, theoretical models of these prototypes have to be developed to study the behavior of these devices and fine-tune their characteristics. Since SiC MOSFETs are still in their infancy, there is a good opportunity now to study and model these devices so that the model can be verified using actual SiC MOSFET test devices.

An application specific optimum SiC power MOSFET is being developed for hybrid electric vehicle applications [7]. The system level benefits of SiC power electronics for hybrid electric vehicle (HEV) applications were also studied. Considering the SiC material processing limitations and feedback from the system level application group, an application specific SiC power MOSFET structure has been proposed.

Modeling of Vertical DIMOS Device

An analytical model for a DIMOS field effect transistor is developed using SiC material. The model is developed based on the methodology for a vertical double diffusion MOS model [8-9]. The proposed DIMOS model incorporates the effect of SiC device behavior. Figure 1 shows the details of the device structure identifying the different regions of operation. The model is developed from regional analyses of carrier transport in the channel and the drift regions. The active channel exists below the oxide layer and within the *p*-bodies.

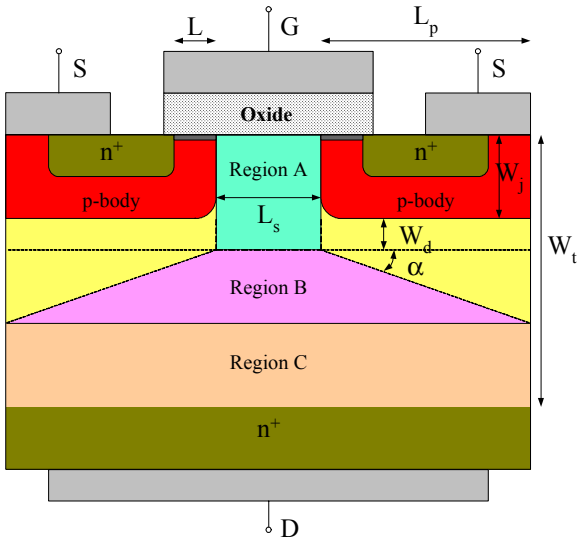

Figure 1. DIMOS structure for modeling. Labels describe the different regions and dimensions

The current/voltage characteristic in the triode region is given by Eq. 1,

$$I_{ch}=\frac{W\mu_n}{2L[1+(\mu_n/2v_{sat}L)V_{ch}]}V_{ch}[2C_{ox}(V_{GS}-V_T)-(C_{ox}+C_{do})V_{ch}] \quad (1)$$

where W is the channel width,
L is the channel length,
V_{ch} is the channel voltage,
V_T is the threshold voltage,
V_{GS} is the gate voltage,
C_{ox} is the oxide capacitance,
C_{do} is the body depletion capacitance,
μ_n is the electron mobility, and
v_{sat} is the electron saturation velocity. The drift region is divided into three parts: an accumulation region-A, a drift region-B with a varying cross-section area, and a drift region-C with constant cross-section. The corresponding voltages to these regions are V_A, V_B, and V_C for regions A, B, and C, respectively and they are given by the following equations.

$$V_A = \int_0^{W_j+W_d} E_y\,dy = \frac{I_D(W_j+W_d)}{W(L_s qN_d\mu_n) - I_D/E_C} \quad (2)$$

$$V_B = \frac{I_D}{WqN_d\mu_n \cot\alpha}\log\left\{\frac{WqN_d\mu_n(L_s+2L_P)-I_D/E_C}{WqN_dL_s\mu_n - I_D/E_C}\right\} \quad (3)$$

$$V_C = \frac{I_D\left(W_t - W_j - W_d - L_P\tan\alpha\right)}{WqN_d\mu_n(L_S+2L_P)-I_D/E_c} \quad (4)$$

where W_j is the depth of n^+ contact region,
W_d is the depth of depletion region,
W_t is the total thickness of epilayer,
L_s is the length of accumulation region, and
L_p is the length of p-body. Total drift region voltage is $V_{drift} = V_A + V_B + V_C$, and the voltage across the drain and the source is $V_{DS} = V_{drift} + V_{ch}$. The voltages and the currents of the above mentioned two sets of equations for the drift region and the channel region are implicitly related. The drain current, I_D is equal to the total channel current I_{ch}, which sets a relationship between the two sets of equations. An iterative solver was developed to evaluate the voltages and the currents. 4H-SiC material parameters were used to evaluate the model.

The model is farther verified by simulating the same device structure in the commercial device simulator MEDICI. A summary of the device structure and doping levels, used in the simulation, is shown in Table 1. The proposed device structure and the device dimensions are selected in such a way that a practical device can be built on the basis of currently available SiC technology.

Table 1. Device Dimensions for the Proposed 4H-SiC DIMOS

Device dimensions		
Channel width	**400 µm**	
Channel length	**1 µm**	
Oxide thickness	**500 Å**	
p-bodies separation	**20 µm**	
Epilayer thickness	**25 µm**	
Doping		
Region	*Doping level*	*Impurity*
n-drift	**4×10^{15}cm^{-3}**	Nitrogen
p-bodies	**4×10^{17}cm^{-3}**	Aluminum
n+ region	**1.5×10^{20}cm^{-3}**	Nitrogen

Simulation Results

The simulation results from the analytical model and numerical simulator are shown in Figure 2 and 3, respectively. The output currents of the vertical MOSFET obtained from the analytical model remain in the saturation region for the device parameter values used in the computations. Numerical simulations demonstrated a clear quasi-saturation effect in the vertical MOSFET. The gate voltage has control over the drain currents as long as the drain current enters the saturation region before the velocity saturation occurs. However, the gate loses its control over the drain currents when the velocity saturation of the

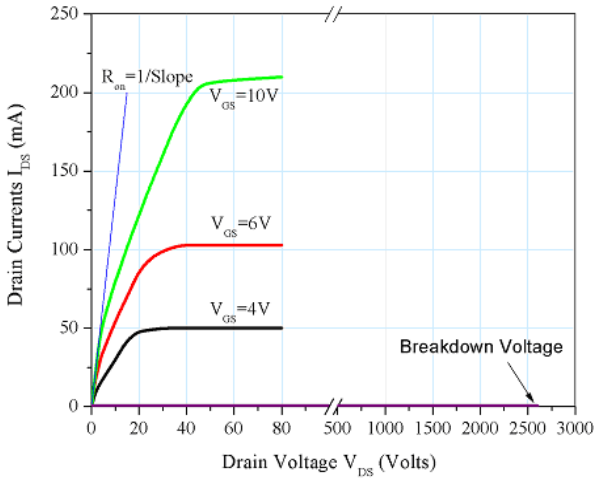

Figure 2. Output characteristics of the analytical model

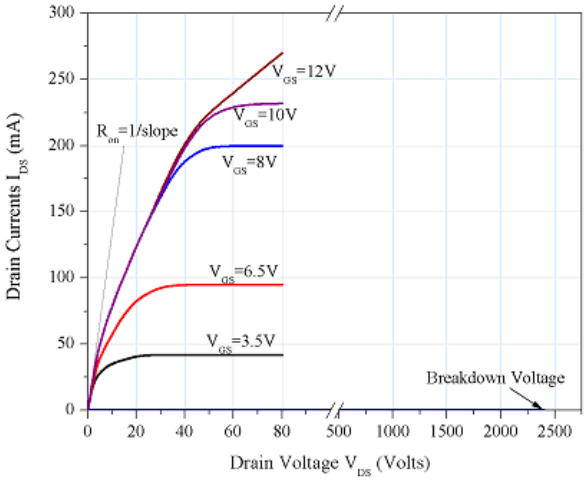

Figure 3. Output characteristics of the MEDICI simulations

Table 2. Summary of the Analytical Model and Device Simulator Results

	Analytical model	MEDICI simulations
Drain currents	220 mA at V_{GS} = 10V	232 mA at V_{GS} = 10V
Specific on-resistance	54 mΩ·cm^2	60 mΩ·cm^2
Breakdown voltage	2.6 kV	2.3 kV

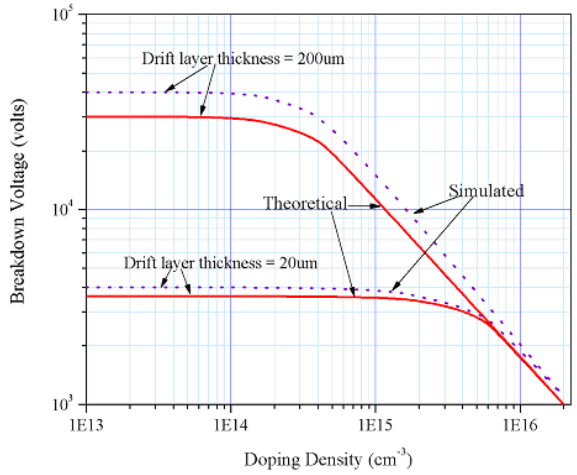

Figure 4. Variation of breakdown voltage with doping density

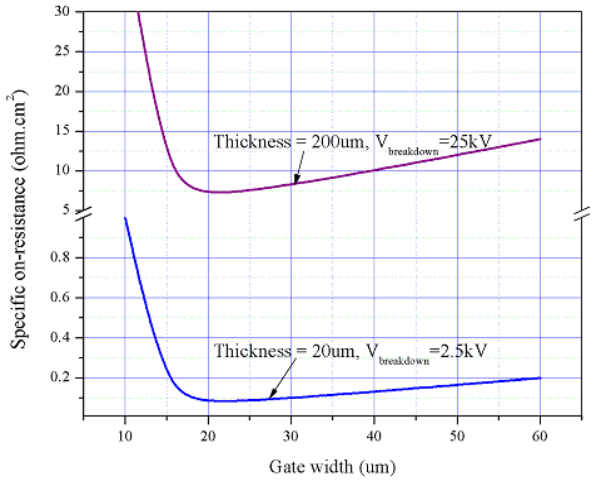

Figure 5. Variation of specific on-resistance with gate width

carrier occurs earlier than the drain current. It is also observed that the quasi-saturation effect occurs at a higher gate voltage for larger *p*-body separations and for higher drift layer doping densities. From the analytical model a drain current of 220 mA is obtained for a gate voltage of 10 V, whereas the device simulator yielded a drain current of 232 mA for a gate voltage of 10 V.

Figure 6. Test setup for DC characterization

Figure 4 shows the comparison of the theoretical and the simulated values of the breakdown voltages with the drift layer thickness as a parameter. The simulated values closely follow the theoretical one. The impact of increasing gate width upon the specific on resistance is shown in Figure 5. The channel and the accumulation layer resistances increase with the gate width. Table 2 summarizes the simulation results.

Testing and Characterization

A DIMOSFET fabricated in 4H-SiC has been tested and characterized at room temperature and at elevated temperature. The test device was obtained with the collaboration of Cree Research Inc., Raleigh, North Carolina. A custom DC measurement system was used to facilitate the DC characterization of the SiC-DIMOSFET test device (Figure 6). A Hewlett Packard HP4145B Parameter Analyzer was used for two primary measurement tasks: measurement of the output characteristics and the transfer characteristics of the test device.

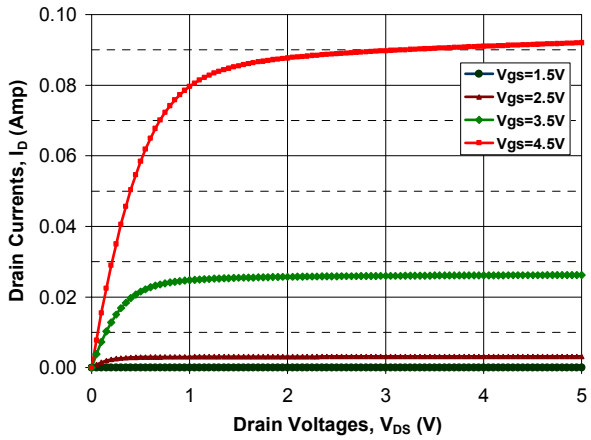

Figure 7: DIMOS output characteristics measured at a temperature of 200°C

The output characteristic of the DIMOS test device at 200°C is shown in Figure 7. A noticeable change of the drain current at higher temperature is observed. At 25°C, the drain current in the saturation region is about 7 mA with a gate voltage of 5 V, and it rises to a value of 40 mA at the same gate voltage but at 100°C. The current reaches a value of 90 mA with a gate voltage of 4.5 V at 200°C. The major reason for the current change is the reduction in

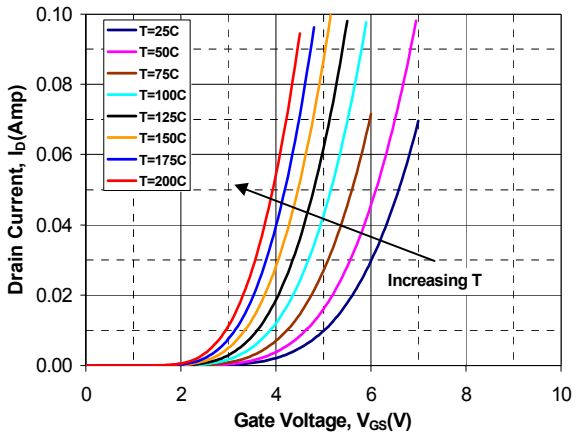

Figure 8: DIMOS transfer characteristics at different temperatures

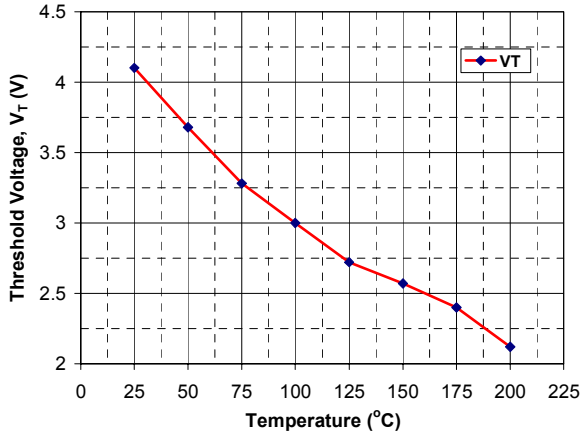

Figure 9: DIMOS threshold voltage, V_T variation with temperature

the threshold voltage and thereby a boost in the drain current with the same gate voltage.

The transfer characteristics at different temperatures are shown in Figure 8. The transfer curves show an interesting behavior, which is different from that of silicon power MOSFETs. In silicon power devices, transfer characteristics show a cross over with the increase of temperature, which is due to the negative temperature dependency of the threshold voltage. However, in a SiC device, transfer characteristics shift in parallel (i.e no crossover) due to the positive temperature dependency of the threshold voltages. The threshold voltage variation with temperature is shown in Figure 9. The threshold voltage changes from 4.1V (at 25°C) to 2.2V (at 200°C).

Conclusions

An analytical model for DIMOS has been developed. A device structure is also proposed to verify the model in 4H-SiC material. A good agreement between the analytical model and the MEDICI simulation is demonstrated. Quasi-saturation effect in DIMOS is observed. The quasi-saturation effects imposed on the *p*-body spacing and drift region doping help to achieve a device structure for the desired current level and breakdown voltage. Device performance at higher temperatures is investigated. A large change of the drain current is observed. The large variation of the threshold voltages at higher temperature results in the huge change of currents.

Acknowledgements

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