AlGaN/GaN MODFET Device for High Temperature Applications

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Abstract

The objective of this paper is to investigate the feasibility and explore the potential of GaN-based devices for high temperature applications. An analytical temperature model based on modified charge control model is developed for the proposed device. The major tasks of this paper include the establishment of the compact model including the thermal effects and the validation of the analytical results and experimental data with numerical simulator. Device reliability and high temperature device operation are investigated. The temperature effect on transport characteristics predicts the device behavior in extreme environments. The analysis of the proposed model shows that the device demonstrates significant degradation at elevated temperatures. Preliminary results from the temperature model and the measured data at room temperature indicate that the device could survive in extreme environments. The calculated values of the critical parameters suggest that the proposed device can operate in the GHz range for temperature up to 600 ^{0}K. So far, extensive investigations have been conducted on the potential of AlGaN/GaN MODFETs for high temperature applications. But the state-of-the-art of GaN based devices indicate exponentially increasing device failure rate at elevated temperatures.

Keywords: AlGaN/GaN, MODFET, high temperature

1.0 Introduction:

GaN and related alloys have attracted a great deal of interests in high frequency applications even at elevated temperatures. Currently, GaN based heterostructures are the most essential structures for utilizing the prominent electrical and optical properties of nitride semiconductors [1]. With the high breakdown electric field and the low carrier generation rate by thermal activation in wide-bandgap semiconductors, much higher doping levels can be achieved at high temperature. AlGaN/GaN HEMTs can be used in extreme conditions where Si-based devices cannot be used. Because of the intrinsic properties, GaN is suitable for high temperature operation and radiation hardness [2].

The charge control model presented here includes the effects of the channel conductance in the saturation region, the n-type thin GaN cap layer on AlGaN and the parasitic resistance due to the undoped GaN buffer layer. The model presented in this paper includes the effects of temperature variation (100 ^{0}K-600 ^{0}K) on the threshold voltage, doping concentration, the carrier mobility, and the saturation velocity. The approach shows better agreement with the experimental data.

2.0 Device Technology:

Charge control models were developed for the simulation of band profiles and charge distributions of the GaN based heterostructures [7,8]. Based on the charge control models, we presented the effect of structure parameters on the electronic properties of GaN based heterostructures. Due to the existence of strong polarization field across the nitrides multi-layer, a two dimensional electron gas (2DEG) with the density up to 10^{13}cm^{-2} can be achieved in the AlGaN/GaN heterostructure without any doping. [2,3]. There are several possible sources of electrons in 2DEG at the AlGaN/GaN heterointerface: the GaN buffer layer, the AlGaN barrier layer, and the AlGaN surface states. To obtain a highly uniform and highly reliable AlGaN/GaN HEMT, one has to suppress frequency dependent instabilities, such as large g_m dispersion, gate-lag and current collapse. Therefore the polarization-induced surface charge is controlled by the n-type doping in a thin GaN cap on AlGaN and stabilized n-GaN-surface between gate and ohmic electrodes [4]. However, for further understandings of the device, it is important to evaluate the effective electron velocity in the channel at high temperature.

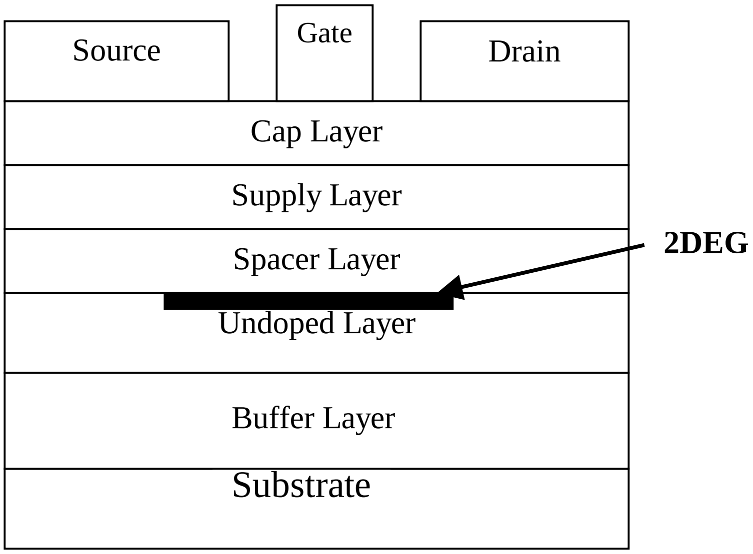

Figure 1: Proposed device structure

In light of the fact that trapping/de-trapping leading to current collapse mainly occurs in the gate-to-drain spacing region, one is motivated to minimize this spacing region. Gate self-aligned HEMTs could be an ideal solution to the current collapse problem. However, self-aligned implantation needs very high activation temperature. Progress in the self-aligned technology will likely lead to a big breakthrough in the device performance, and drive GaN HEMTs into commercialization.

Figure 1 shows the proposed device structure. The device structure consists of 1 μm thick $Al_{0.35}Ga_{0.65}N$ quantum well channel separated by 30 Å of undoped $Al_{0.35}Ga_{0.65}N$ spacer layer from 400 Å thick *n*-type $Al_{0.35}Ga_{0.65}N$ supply layer. The function of the undoped spacer layer is to reduce the impurity scattering. A 30 nm GaN buffer layer can be grown on a SiC/Sapphire substrate. The concentration of two-dimensional electron gas (2DEG) is controlled by the application of the gate voltage. The doping concentrations and thickness of various layers are selected to provide adequate channel charge density.

Temperature dependency of energy gap (eV) for GaN is given in [5]:

$$E_g = Eg\,(0) - 7.7x\,10^{-4}\,x\,T^2/\,(T+600) \qquad (1)$$

The temperature-dependent mobility ($cm^2/V/s$) is reported in [6, 7]

$$\mu_n\,(T) = -8.7\,x\,10^{-5}\,T^2 - 0.4T + 411 \qquad (2)$$

The threshold voltage is given in [6, 7],

$$V_{th} = \phi_b - \frac{qN_2 d_d^{\,2}}{2\varepsilon_2} - \frac{qN_d d_1^{\,2}}{2\varepsilon_1} + \frac{\Delta E_{f1}}{q} \qquad (3)$$

The equivalent or total capacitance per unit area, C_{eq} is given by,

$$\frac{1}{C_{eq}} = \frac{\Delta d + d_i + d_d}{\varepsilon_2} + \frac{d_s}{\varepsilon_{Si}} \qquad (4)$$

There are many material parameters that are related to the calculation of the threshold voltage, and a number of empirical relationships have been obtained from the experimental data [5].

The resistance of the metallic contact is neglected due to the large contact area in the proposed device structure. The energy levels in the quantum well channel and the electron wave function inside and outside the quantum well are evaluated by self-consistently solving Schrödinger and Poisson's equations [7,8].

3.0 Results:

The HEMTs characteristics can be classified into DC and RF based on critical parameter, reliability and uniformity. The critical parameter are the maximum drain current, the threshold voltage, the peak DC transconductance, break down voltage and output conductance. The gate geometry scaling on DC characteristics is also important. GaN HEMTs shows negative resistance at high voltage and current. It is because of self-heating of the devices due to the poor thermal conductivity of sapphire [6].

In order to fully develop the potential of the device at high temperature, it is very important to evaluate the high temperature performance of the device not only at dc but also at high frequency.

HEMT has wide range of applications that include low temperature as well as high temperature electronics. But the operation of GaN MODFET at low temperature produces a substantial enhancement in device performance over room temperature. This is mainly due to the higher carrier mobility and the lower leakage current. The output current voltage characteristics at room temperature compared with the experimental results in Figure 2.

Figure 3 shows the saturation current as a function of gate voltage over a temperature range from 100 ^{0}K-600 ^{0}K. The f_T values of the device show a significant improvement over the low temperature range in Figure 4. Figure 5 shows temperature effect on transconductance characteristic.

Medici^{TM} is an industry standard device simulator that can predict the electrical characteristics of arbitrary two-dimensional structures under user specified operating conditions. The simulator takes voltage bias at the electrode and determines the current at each terminal. More realistic device structure and detailed device inside can be visualized (Figure 6). Figure 7 shows the Medici simulation; saturation current as a function of gate voltage Thus precise control of layer thickness and material composition is possible for complete analysis.

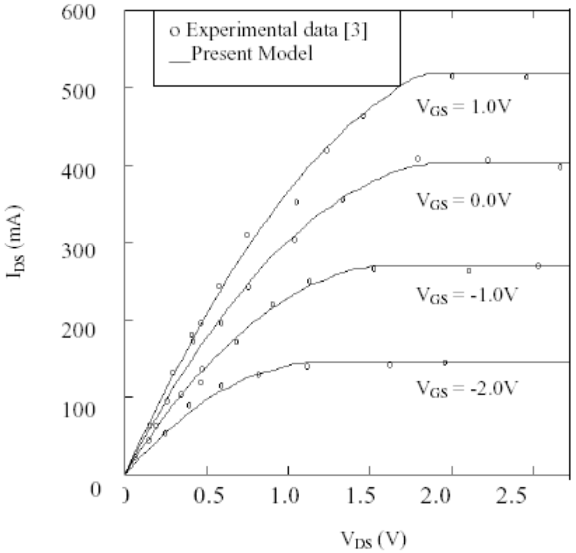

Figure 2: The output current voltage characteristics at room temperature

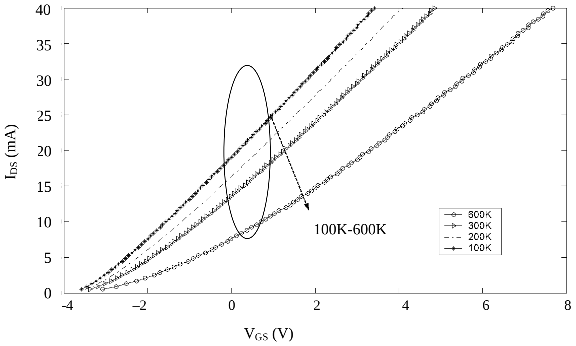

Figure 3: Temperature effect on saturation current as a function of gate voltage

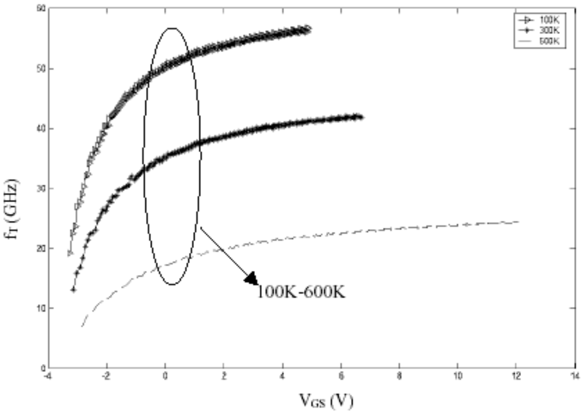

Figure 4: Temperature effect on unity gain cut off frequency

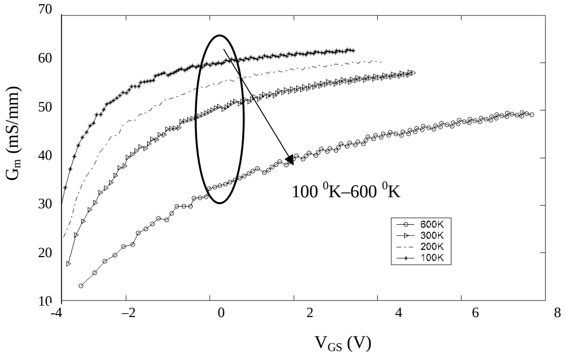

Figure 5: Temperature effect on transconductance characteristic

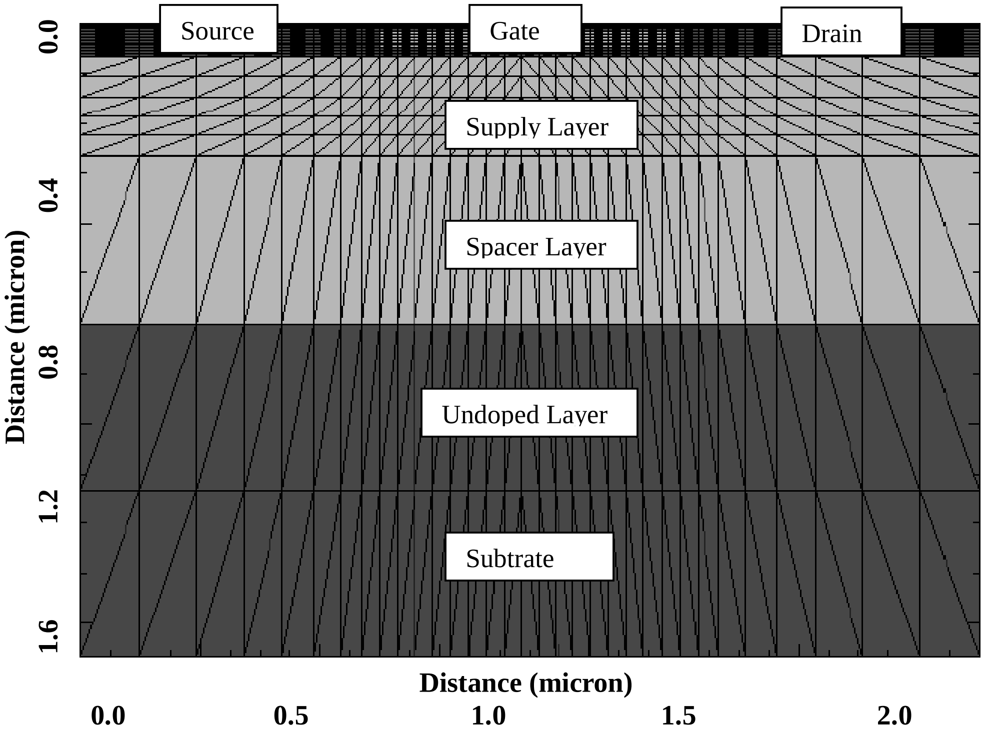

Figure 6: Medici simulation; HEMT Device structure

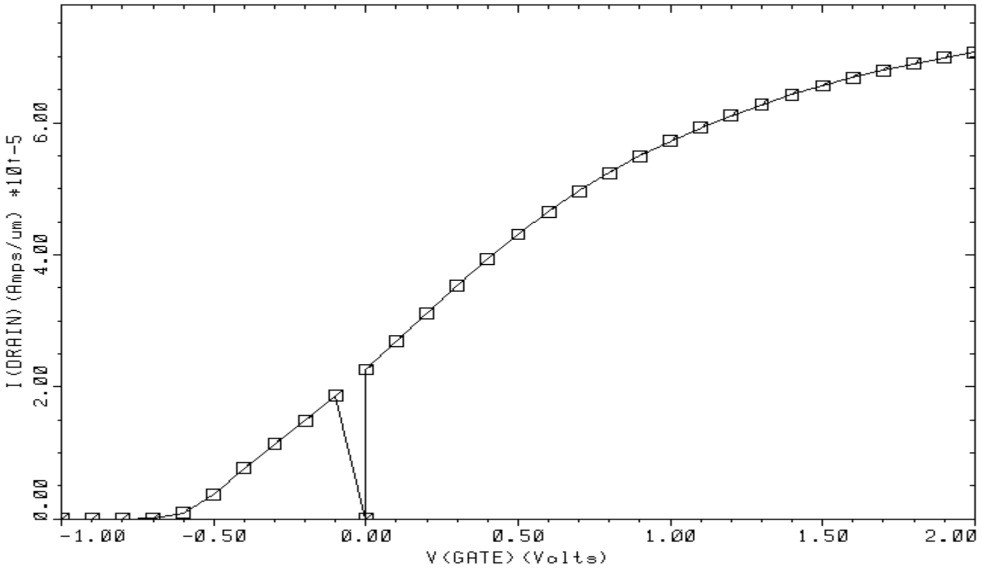

Figure 7: Medici simulation; Saturation current as a function of gate voltage

4.0 Conclusion:

There are two major problems limiting the GaN HEMT performance at high temperature. One is the current collapse and the other is the gain compression at high current level. Thus MOS gate HEMT can be an attractive alternative. The gate leakage current for the MOS gate HEMT is much smaller than that of HEMT. But the state-of-the-art of GaN based devices indicate exponentially increasing device failure rate at elevated temperatures. Thus the technical strategy requires comprehensive development efforts with many industrial and academic partnerships.

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