

SOI-Based Integrated Circuits for High-Temperature Applications

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Abstract

Potential shortage of world wide petroleum supply in the near future has created an enormous demand for green vehicles that use higher power electric motor drive in their traction systems. Application of power electronic modules in automobiles has generated the need for reliable and low-cost high-temperature electronics which can operate at the extreme temperatures that exist under the hood. In this paper, we are presenting an improved version of our earlier work on high-temperature and high-voltage integrated silicon-on-insulator (SOI) based gate circuit for SiC FET switches. This driver circuit has been designed and implemented using 0.8-micron, 2-poly and 3-metal BCD on SOI process. The prototype chip has been successfully tested up to 200°C ambient temperature without any heat sink or cooling mechanism. This gate-driver chip is intended to drive SiC power FETs in DC-DC converters in a hybrid electric vehicle. The converter modules along with the gate-driver chip may be placed next to the engine where the temperature can reach up to 175°C. Successful operation of the circuit at this temperature with minimal or no heat sink, and without liquid cooling, will help to achieve higher power-to-volume as well as power-to-weight ratios for the power electronics module.

Key Words: High-temperature, high-voltage gate driver, voltage-regulator, silicon-on-insulator.

I. Introduction

Global oil production is predicted to reach its peak by year 2015 [1]. After reaching the maximum, oil production will start to decrease sharply. At present time, the world is using four times more oil than is being discovered. In the USA, oil provides 99% of the fuel used in its transportation sector. This huge worldwide demand for petroleum-based fuel is potentially threatening to cause its shortage in near the future. This possibility is inspiring university researchers, government agencies and industries to develop smarter technology for the transportation sector. In addition, the growing concern for environmental pollution caused by the burning of fossil fuel is also inspiring many to support green vehicles.

At present, researchers are working on three major technologies to incorporate the advantages of electric motor drive in the automotive sector. Hybrid-electric vehicles (HEV), the leading technology among the three, use both internal combustion or diesel engines and electric motors to improve the performance and efficiency of the vehicle. Plug-in-hybrids (PHEV) use larger battery packs and external charging capability to make it possible to reap the benefits of electric vehicles while overcoming their

drawback of limited range. These vehicles do not use the internal combustion engine (ICE) for shorter distances (usually up to 30 miles). Fuel-cell vehicles (FCV) generate their own electricity using hydrogen or other fuel convertible to hydrogen. FCVs are widely considered as the future replacement of the internal combustion engine vehicles (ICEV). This replacement could save 60% of the primary energy consumption, and can reduce the CO₂ emission by 55% [2]. But FCVs are not yet in a position to challenge ICEVs for performance, cost, fuel storage, and large scale manufacturability [2]. On the other hand HEVs are gaining more attention for their better performance and fuel economy compared to ICEVs. Transition from ICEV to HEV means switching from mechanical and hydraulic systems to electromechanical systems.

A typical arrangement of a series/parallel HEV is shown in Fig. 1. Developments in the hybrid automobile industry have generated an enormous need for different power electronic modules (such as DC/DC converters and DC/AC inverters) capable of operation at elevated temperatures. Integration of power converters and smart power devices into the drive train requires semiconductor devices capable of working at 150°C to 200°C for air cooled devices [3]. Applications of high-temperature electronics in

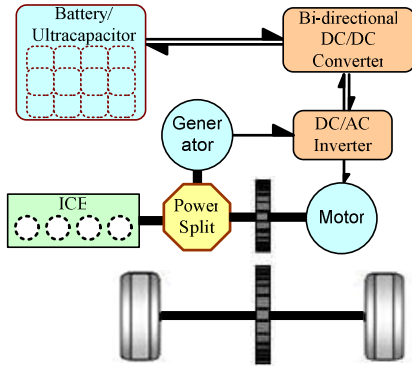


Fig. 1. Typical topological arrangement of Series/Parallel HEV.

automotive systems will continue to grow with their increased availability and reduction in price. It is predicted that by 2013 each automotive will contain on the on the average \$2285 worth of electronics within its frame [4].

DaimlerChrysler, Eaton Corporation, and Auburn University have reported high-temperature automotive electronics requirements in [5] (Table I). Much of the cavity under the hood the temperature is more than 150°C. The junction temperatures for integrated circuits can easily be 25°C higher than the ambient temperature. Hence electronics used in automotives, especially those placed close to the engine, need to be able to work at temperatures at or above 150°C.

The alternatives to high-temperature devices and circuits are complicated thermal management systems that add weight and volume resulting in reduced power-to-volume and power-to-weight ratios. These thermal management approaches introduce additional overhead that can negatively offset the desired benefits of the electronics relative to the overall system operation. The additional overhead in the form of longer wires, extra connectors, and/or cooling system can add undesired size and weight to the system, as well as increased potential for failure [6]. By removing the heat sink and long interconnects, an order of magnitude savings in overall mass and volume of the power electronic modules can be achieved.

This work presents a silicon-on-insulator

Table I. Automotive Temperature Ranges [5]

In-transmission	150-200°C
On-engine	150-200°C
On Wheel-ABS sensors	150-250°C
Cylinder pressure	200-300°C
Exhaust sensing	Up to 850°C, ambient 300°C

(SOI) based high-temperature, high-voltage integrated gate driver circuit for automotive applications. In all power electronic circuits, a gate driver is an essential component to control the turning “on” and “off” of power switches. In HEVs or FCVs, power converter modules along with the drivers are required to be placed very close to the engine to optimize the performance. Hence, the ambient temperature of the gate driver IC will be 150°C or higher. The first prototype of the gate driver circuit has been successfully tested with a SiC power MOSFET at 20 kHz and up to 200°C without any heat sink and cooling mechanism [7]. An improved version of this gate driver design has been implemented and tested for more reliable performance. Till now it has been successfully tested up to 190°C. This new design also includes a temperature compensated on-chip voltage regulator to minimize the number of external voltage supplies to the chip. Simulation and test results for this new prototype are presented in this paper.

II. Device Technology for High Temperature Electronics

In the automotive, aerospace and energy production industries there is an ever increasing demand for electronic circuits capable to operate at ambient temperature higher than 150°C. But the maximum rated ambient temperature for most of the commercially available silicon-based integrated circuits is 85°C [3]. Si-based devices rated for military and automotive applications are marked for only 125°C.

Wide bandgap (WBG) semiconductors, because of their larger energy bandgap, are capable of operating at much higher temperatures than silicon. In the future, WBG semiconductors will be the material of choice for simultaneous realization of high-power and high-temperature applications. Silicon Carbide (SiC) based devices are the most widely researched wide bandgap semiconductor to date for power switch realization [8]. SiC-based devices are expected to be able to operate up to 600°C. However, SiC-based power switches are not

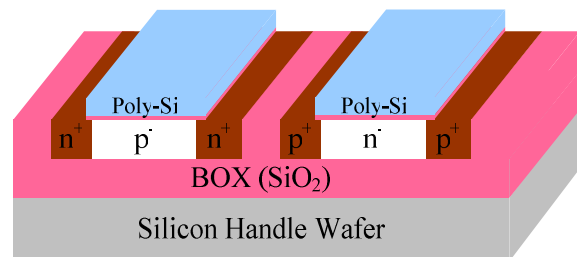


Fig. 2. Cross section of an SOI CMOS structure.

yet commercially available. SiC-based integrated circuit manufacturing will take longer to become commercially available.

In high-temperature electronics, junction leakage is a major concern in bulk CMOS processes. This causes higher junction temperature compared to the ambient and potentially leads to the failure of the circuit. Silicon-based CMOS with reduced leakage current for high temperature operation is realized with the silicon-on-insulator structure as shown in Fig. 2. A buried insulator layer in the SOI structure greatly decreases the leakage path associated with the drain and the source p-n junction diodes. The presence of the buried oxide also reduces off-state source to drain carrier emission leakage that physically occurs deeper in the p-type substrate of bulk MOSFETs. In addition, threshold voltage variation with temperature is smaller in SOI devices than in bulk devices [9]. SOI also provides improved latch-up immunity, which ultimately increases the reliability of the circuit operation at higher temperature [10]. These properties make SOI-based circuits capable of operating successfully in the 200°C-300°C temperature range which is well above the range of conventional bulk silicon-based devices.

III. High-Temperature, High-Voltage Gate-Driver Design

In literature different gate driver topologies have been presented for FET-based power switches [11-15]. Among these only the circuit reported in [14] is capable of operating at a junction temperature up to 200°C, while others can work only up to 125°C. The authors of [15] have presented a low-loss high-frequency half-bridge gate driver circuit on SOI for driving MOSFET switches. However, there is no mention of the temperature capability of the circuit. We have presented our first prototype of SOI-based high-temperature, high-voltage gate driver circuit in [7]. In this work, we are presenting an improved

version of that gate driver circuit. Design focus of this iteration was to make it more robust and incorporate the bootstrap capacitor on chip. A block diagram level schematic of the gate driver circuit implemented in this design is shown in Fig. 3. Compared to our first prototype, in this design “dead zone generator” and “pulse shaper” blocks are added. The purpose of these new blocks is explained in the following discussion.

Two high-voltage (45 V) NMOSs (M_L and M_H) with large aspect ratios constitute the half-bridge output stage of the gate driver circuit. Complementary switching of these two NMOSs connects the output terminal (i.e. gate terminal of power switch) to one of the two supply rail voltages (V_{DDH} and V_{SS}). Rail voltages will depend on the type (MOSFET or JFET) of power switch and its gate voltage requirement for its turning “on” and “off”. The key criterions for designing the output stage of any driver are the peak current requirement, on resistances, switching speed and gate voltage magnitude. The topology used in this circuit consists of two NMOS transistors stacked together. NMOS transistor has lower on resistance and higher switching speed compared to its PMOS counterpart. LDMOSs with 45 V breakdown voltages are used to get larger output voltage swing.

Because of their large W/L ratios, both of the transistors in the output stage present large capacitive loads to the control electronics part of the gate driver circuit. But these two transistors need to be switched fast to get the desired low turn-on and turn-off time of the power switch. Fast switching of these transistors are also important to minimize the switching losses. To meet the transient current requirement to charge the large gate capacitances of these transistors, multi-stage buffers with gradually increasing sizes (exponential horn) are employed in the design.

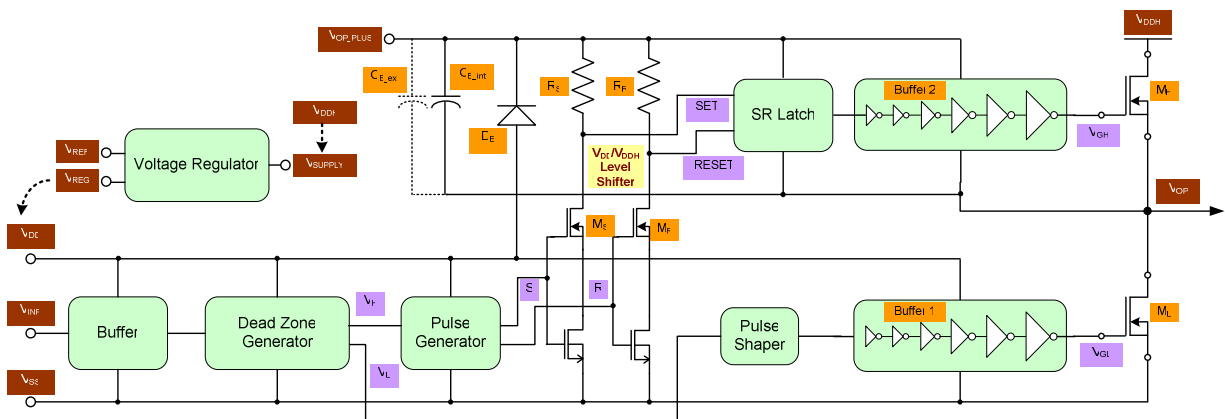


Fig. 3. Schematic of the high-temperature, high-voltage gate driver circuit.

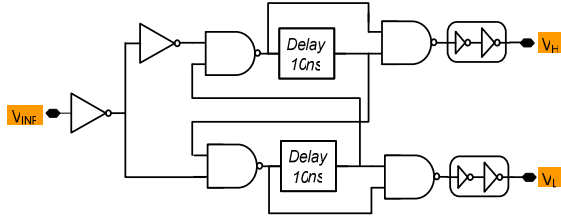


Fig. 4. Dead zone generator circuit.

The gate voltage signals of the two output stage high-voltage NMOS transistors need to be carefully managed to prevent their simultaneous on-state conduction. Otherwise large short circuit or “crowbar” current will result, causing die temperature to increase. To ensure a break-before-make type operation, we have introduced a dead zone between the gate signals. The “dead zone generator” block added in this version of the gate driver circuit controls the duration of the non-overlapping gate signals for M_H and M_L transistors. Fig. 4 shows the schematic of this circuit. This uses similar circuit topology to that of a complementary clock generator with the addition of a delay circuit. Since the pulse trains generated by this circuit pass through different circuit components, an additional “pulse shaper” circuit is used to further modify the low side gate signal to ensure complementary switching of M_L and M_H .

The dead zone generator block generates two non-overlapping complementary copies (V_H and V_L) of the buffered input signal which are then further processed to generate appropriate gate signals for the NMOS transistors in the output stage. The latch control circuit takes V_H as its input and generates two narrow pulse trains (S and R), one at the rising edge of V_H and one at its falling edge. These pulse train signals S and R have durations of only 10 ns to ensure minimum power loss in R_S and R_R resistors shown in Fig. 3.

These S and R signals alternately turn “on” and “off” the M_S and M_R high voltage NMOSs which effectively level shifts the low voltage logic signal from V_{DD} level to V_{DDH} level. Voltage drop across R_S and R_R by the complementary switching of M_S and M_R generates the ‘SET’ and ‘RESET’ signals. The SR latch used here is an active low latch that is controlled by the ‘SET’ and ‘RESET’ signals. This latch’s output is used to generate the high-side gate signal V_{GH} . The V_L output of the dead zone generator is further processed by the “pulse shaper” circuit for further timing adjustment in V_L . This adjustment is needed for unequal delay associated with the circuits

generating the high-side and low-side gate signals from V_H and V_L .

In the first prototype, a 5-nF external bootstrap capacitor was used to generate a floating voltage source for the circuitry generating the gate voltage for the high-side NMOS (M_H). Improvement of the circuit design in this version makes the size of this bootstrap capacitor smaller. A 1.2 nF on-chip capacitor has been added in this new design to make it fully integrated. The inclusion of an on-chip capacitor also alleviates the problem of finding reliable high temperature off-chip capacitors, thus helping to achieve more reliable performance at elevated temperature. The bootstrap circuit, consisting of diode (D_B) and bootstrap capacitor (C_{B_int}), generates a voltage level (V_{OP_PLUS}) higher than the highest rail voltage available (V_{DDH}). This is required for “Buffer 2” in Fig. 3, the SR latch, and the level shifter in order to generate the V_H gate signal for the M_H transistor. The node V_{OP} acts as the floating ground reference point for the high-side circuitry.

IV. High Temperature Voltage Regulator

In this prototype we have included an on-chip voltage regulator to generate the low bias voltage (V_{DD}) from the high supply voltage (V_{DDH}) to the chip. Depending on the gate voltage of the SiC power switch that this driver is driving, the V_{DDH} can be set to any value starting from 15 V to 30 V. Hence the regulator in this chip needs to be functional over wide input voltage range (15 V to 30 V). Output voltage of the regulator will replace the V_{DD} supply voltage. Another critical aspect of this regulator design is that it also needs to generate fairly constant voltage over a wide temperature range (-50°C to 200°C). A schematic of the voltage regulator (low-dropout type) topology used in this work is shown in Fig. 5. This circuit has two distinct building blocks. The first block is a bandgap reference (BGR) circuit

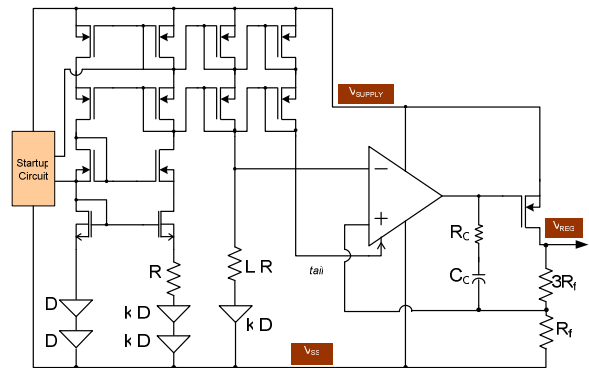


Fig. 5. On-chip voltage regulator circuit schematic.

which generates a constant reference voltage over wide temperature variation. The second block is a single stage differential amplifier which forms a negative feedback loop with a PMOS transistor. A compensation circuit has been added to improve the phase margin of the voltage regulator. The temperature compensated reference voltage generated by the BGR circuit is used as the reference voltage for the differential input amplifier. Temperature coefficient (TC) of the bandgap reference is minimized by proper weighting of the positive TC of the thermal voltage with the negative TC of the diode forward voltage in the circuit. A simulation result showing the variation of the regulator output voltage in response to an input voltage variation from 15 V to 30 V at different temperatures is shown in Fig. 6. At any temperature the voltage variation is less than 200 mV for input voltage variation of 15 V while with any fixed supply voltage this variation is less than 110 mV for temperature variation from -50°C to 200°C . Simulations also show the successful operation of the gate driver circuit biased by this regulator.

V. Design Implementation

This high-temperature gate driver circuit has been designed and implemented in a $0.8\text{-}\mu\text{m}$ BCD SOI process. The gate driver circuit including voltage regulator and on-chip bootstrap capacitor occupies an area of 5 mm^2 ($2,240\text{ }\mu\text{m} \times 2,240\text{ }\mu\text{m}$) including pads and ESD protection circuits. NMOS devices in the half-bridge output stage occupy a major portion of the chip area. They are sized ($W/L = 28,000\text{ }\mu\text{m}/1.6\text{ }\mu\text{m}$) to provide large peak current to the load. Each of these NMOS transistors is comprised of seven hundred 45 V NMOS devices ($W = 40\text{ }\mu\text{m}$) connected in parallel. The high-voltage devices are

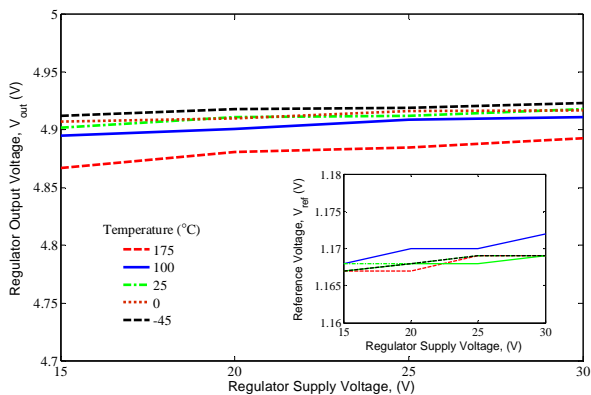


Fig. 6. Voltage Regulator output in response to supply voltage variation at different temperatures. Inset: Reference voltage generated by the bandgap reference circuit at different temperatures.

well isolated from the low-voltage devices through thick dielectric layers. The layout of the high-voltage devices resembles a “race-track” structure [16].

At elevated temperature one of the severe chip failure mechanisms is electromigration. In this failure mechanism current flow over time gradually displaces microscopic metal traces on an interconnect, eventually leading to failure [17]. To alleviate this problem all the metal interconnects were made oversized to reduce the current density through them. In all possible cases top metal layers were used to carry the heat to the top surface. This will help minimize the die junction temperature.

For the new design, schematic level simulations were performed over temperature from -40°C up to 175°C . The circuit was simulated with a capacitive load of 10 nF in series with $10\text{ }\Omega$ resistance to mimic the gate of a SiC-based power switch. Fig. 7 shows the output current generated by the driver along with the current flowing through the M_H and M_L transistors. Simulation results ensure the complementary switching of M_H and M_L . This will reduce the power dissipation through these devices and help keep the junction temperature closer to the ambient temperature.

VI. Experimental Results

Fig. 8 shows a microphotograph of the second generation prototype of the gate driver circuit. Multiple pad connections are used for the power supply and output nodes to minimize the parasitic bond wire inductance. The chip was bonded in a ceramic package which is capable of operating above 200°C . Test boards made of polyimide material are used for high temperature testing of the prototype chip. High temperature solder and wires are used for reliable testing of the chip.

The prototype ICs were tested with 4.7-nF capacitor load in series with $10\text{-}\Omega$ resistor at different

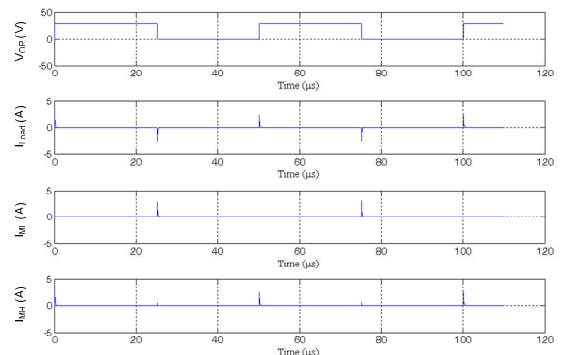


Fig. 7. Output voltage and current supplied by the driver circuit and currents through M_L and M_H .

temperatures. The output voltage was raised to 20 V_{p-p} and was successfully tested up to 150°C. The driver circuit was also tested at different temperatures while driving a 1200 V, 10 A SiC MOSFET sample from Cree. A 10 Ω resistive load was used with the SiC MOSFET in common source configuration. A 5-A switching current was allowed to pass through the load and the switch when it was turned “on” by the driver. During temperature testing the gate driver chip and its test board were placed inside an environmental chamber temperature. Fig. 9 shows the digital input signal (blue), gate driver output (pink), and load voltage at the drain terminal of the SiC MOSFET (cyan) at 190°C. Thus far three test chips have been successfully tested at or above 150°C for several hours and all the chips are still functional and there is no deterioration in the performance of these chips up to this temperature. One difference that we observed during experiment compared to the simulation is that the low bias voltage (V_{DD}) needed to be higher than the simulation value (5 V) to make the chip function properly at temperatures higher than 115°C. Currently we are investigating the test board to find the possible reason of this problem. The first prototype of the gate driver circuit was successfully tested with 10 nF capacitor and 10 Ω resistor up to 175°C [7]. It was also tested with SiC MOSFET up to 200°C ambient temperature [18]. In the first prototype there were several incidents of failure of the chip that have been resolved in the new version.

VII. Conclusions and Future Work

Though this gate driver has been designed for automotive applications, this could be easily applicable to any harsh environment applications where conventional bulk silicon-based devices could not deliver efficient and cost-effective solutions. For

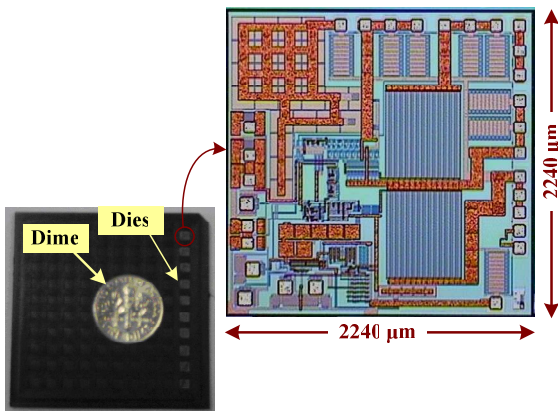


Fig. 8. Micrograph of the fully integrated high temperature gate driver circuit showing the size of the dies compared with a dime.

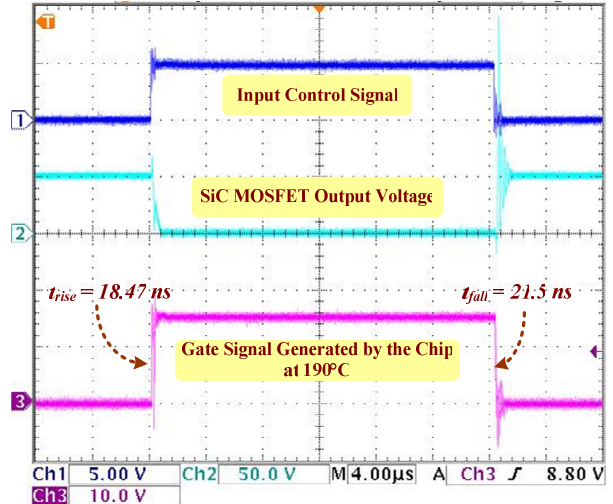


Fig. 9. Test results at 190°C ambient temperature.

efficient and effective integration of wide bandgap power devices into power electronic modules, SOI-based integrated circuits capable of working above 150°C ambient temperature are needed to interface them with control circuitry. The improved high-temperature and high-voltage gate-driver circuit presented in this paper is part of a research effort to design a heat-sink-less DC-DC converter module for hybrid electric vehicles that can be placed close to the engine. The occasional failure issue of the first prototype has been resolved in this second prototype. A 1200-V, 10-A SiC MOSFET switch has been successfully switched by this driver up to 190°C ambient temperature for several hours without any heat sink and cooling mechanism. The rise-time and fall-time were measured to be 18.5 ns and 21.5 ns respectively. Compared to the first prototype, the bootstrap size has also been reduced and has been included in the chip to make it fully integrated. In the future we will test the on-chip regulator circuit for different load conditions and at wide temperature range. We will also incorporate protective features like over temperature protection, short-circuit and low-voltage protection in the gate driver circuit.

Acknowledgment

This work was funded by Oak Ridge National Laboratory through the U.S. Department of Energy’s Vehicle Technologies Program.

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