A Universal BCD-on-SOI Based High Temperature Short Circuit Protection for SiC Power Switches

Liang Zuo[1,*], S. K. Islam[1], M. A. Huque [1], B. J. Blalock[1], and L. M. Tolbert[1,2]
[1]Min H. Kao Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996-2100
[2]Oak Ridge National Laboratory, Oak Ridge, TN 37831-6472
[*]leozuo@utk.edu

Abstract

In recent years, the rapid increase in the market for hybrid electric vehicles has generated great demand for low-cost, high-volume, high-temperature power converters that can work in harsh environment (temperature ≥ 150°C) conditions. Most of the commercially available power semiconductor devices and associated control electronics are rated for maximum of 85 ℃ ambient temperature. Under this circumstance, wide bandgap (WBG) semiconductors have become a better alternative due to their ability to operate at much higher temperatures (≥500 ℃) than conventional bulk silicon based devices. As with any other power devices, SiC switches also require fault detection and protection mechanisms for their reliable application to real systems. One severe fault situation is the short circuit at the load end, which can cause very high surge currents that flow through the power switches. Quick detection and removal of the short circuit fault current by external circuitry is required to protect the power switch as well as the power converter module.

This work presents a high-temperature (≥200°C), high-voltage short circuit protection (SCP) for SiC power devices. The circuit is designed using a resistor sensing method to provide protections for both "normally ON" and "normally OFF" SiC FET switches. A rail-to-rail input comparator is employed to ensure that the circuit operates under different power supply levels. The prototype circuit is implemented using a 0.8-micron, 2-poly, and 3-metal BCD-on-SOI process. The die size for the protection circuit is 0.52 mm^2 (845 μm×612 μm). The circuit has been successfully tested up to 200 ℃ ambient temperature under power supplies ranging from 10 V to 30 V without any heat sink or cooling mechanism.

Key words: SiC, BCD-on-SOI, high-voltage, short-circuit protection, high-temperature.

I. INTRODUCTION

Speculation suggests that world oil production will reach its peak by 2015 [1]. Failure to initiate mitigation of oil consumption will result in a significant impact on world economy. Since 99% of fuel used in transportation is provided by oil, one effective method is to replace a large amount of fuel consuming vehicles. Hybrid electric vehicles (HEVs) and plug-in HEVs (PHEVs), on the other hand, are potential substitutes because of their better fuel efficiency and high output power compared to conventional internal combustion engine vehicles (ICEVs). HEV and PHEV industrial development has generated great demand for different power converters (DC/DC converters and DC/AC inverters) that can be placed under the hood where the ambient temperature is around 150˚C to 200˚C [2] [3].

However, most commercially available Si-based power switches cannot be used inside these power converters since their maximum rated temperature is 125˚C for military and automotive applications. At higher temperature, the intrinsic carrier concentration of silicon becomes comparable to intentional device doping, which creates undesired large leakage current, and leaves the conductivity of the semiconductor device out of control. Wide bandgap semiconductors (WBG), however, have much smaller intrinsic carrier concentration than their silicon counterparts. This property theoretically allows device operation at a junction temperature of more than 800˚C [4].

Among all the wide bandgap semiconductors, silicon carbide (SiC) based devices have been attracting continuous research in recent years [5]. The high breakdown field and high thermal conductivity of the SiC device provides extremely high power density and efficiency compared to silicon based

devices. Unfortunately, SiC based power switches are not yet readily available in the commercial market at this time. Only SiC Schottky diodes are commercially sold in the market.

One gate driver circuit is already realized for SiC power switches using a 0.8-μm BCD-SOI process with operating temperature range from 25˚C to 200˚C [6].

SiC and other WBG power switches still need to be protected from short circuit conditions like other current limiting power devices. The short circuit fault usually results from either wiring misconnections at the terminal or motor winding insulation failure [7]. Under these fault conditions, the high surge drain current, with magnitude mainly limited by the device's own gain, will impose mechanical and thermal stress on the power switch severely degrading its reliability and lifetime.

A protection circuitry is necessary to remove the fault current within microseconds. The protection circuit should also be capable of operating at ambient temperatures up to 200˚C since it must be placed near the power switch under the hood. Presently there are several proposed short circuit protection topologies [8-10]. Most designs use discrete devices to implement the SCP that can require significant area, cost, and power consumption. Several proposed solutions integrate SCP with gate driver circuitry on chip using a bulk CMOS process but target operating temperatures below 125˚C.

Conventional bulk CMOS processes exhibit high leakage current at temperatures over 125˚C thanks to the parasitic PN junction. Also, CMOS device transconductance decreases at elevated temperature, as well as the overall circuit performance. And the destructive mechanism latch-up is a major concern for bulk CMOS at high temperature. The SOI fabrication process though offers a better solution at the evaluated temperature because the buried insulation layer in its cross-sectional structure greatly inhibits the leakage path associated with the drain and source PN junction diodes. The latch-up phenomenon in conventional bulk CMOS process is also avoided by using an SOI process; therefore, further increasing the reliability of circuit operation at high temperatures.

This work presents a BCD-on-SOI based short circuit protection circuit applicable for both SiC MOSFET and SiC JFET switches. It is tested at temperatures from 25˚C to 200˚C and power supply voltages from 10 V to 30 V. This SCP circuit is integrated with the gate driver core circuit [6] and an on-chip voltage regulator with output of 5 V [11]. They all share the same power supplies.

The remaining parts of this paper are organized as follows: Section II introduces the short circuit behavior and protection schemes. The description of short circuit protection is discussed in Section III. Section IV presents the temperature stable voltage reference. Finally, test results are presented in Section V.

II. SHORT CIRCUIT BEHAVIOR AND PROTECTION SCHEMES

The maximum operating current in SiC power switches is restrained by its material quality deficiency [4]. Overrated current density will place extreme electrical stress on the devices. Therefore, normally SiC power switches are only operated at tens of amperes. A short circuit protection scheme is necessary to prevent the operating device from failure by exceeding its maximum current ratings.

Short circuit fault can fall into two categories in most cases: fault under load (FUL) and hard switch fault (HSF) [7]. The FUL results from a short circuit at the load during the device's "ON" state operation. The drain voltage is quickly brought up to a much higher value. Accordingly, this large *dV/dt* causes a transient current i_{DG} to flow through the Miller capacitance C_{DG}. The gate voltage is then pulled up immediately since i_{DG} flows back to the driver circuit through the gate resistor *Rg*. Inevitably, the fault current is increased to an undesired value as the gate voltage is out of control. Hard switch fault, on the other hand, means the short circuit is formed at the load before the power switch turns "ON". Large *dV/dt* does not exist upon switching since the system voltage is consistently applied across the device. However, due to the large drain voltage, the drain current is still beyond its limit during the "ON" state.

The immediate removal of the gate voltage can clear the device from both fault conditions. But the rapid fall of the fault current combined with the DC loop inductance creates over voltage at the drain terminal above the system power supply. The magnitude of this over voltage is decreased by increasing the resistance of *Rg*, because with larger *Rg* it takes longer for the gate driver to shut down the power switch. Hence, the value of *Rg* plays an important role in both FUL and HSF. By decreasing *Rg*, overrated current of the power device during FUL is controlled by clamping the gate voltage at a smaller value. Alternately, higher *Rg* is preferred because it decreases the over voltage.

To protect the device from failure under either FUL or HSF conditions, imminent detection of fault current and shutdown of the power switches are necessary. In addition, the protection circuit should also be insensitive to any nuisance current surges and should not affect the switching performance of the

SiC switch. Several protection schemes are frequently employed in the design of SCP.

Figure 1 depicts de-saturation protection [12]. It utilizes a sense diode to detect the over voltage at the drain terminal. This method features fast operation and simple topology. However, it cannot detect an exact fault current level which makes the indication of fault condition ambiguous. In addition, to also protect SiC JFET power switch, sufficient reference voltage with a magnitude higher than the positive power supply is required to be compared with the fault voltage across V_{DS} [8], which necessitates an additional power supply for the gate driver chip. This power supply voltage is not available in this application.

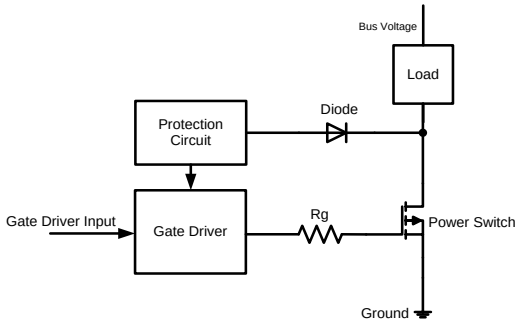

Figure 1. De-saturation SCP.

Another method shown in Figure 2 employs a test power switch with its area proportionally scaled to the main switch [13]. By connecting the two power switches in parallel, the current in the test switch follows the same pattern with the main switch drain current. Thus, any fault current is detected by connecting a sense resistor in series with the test switch. The advantage of this circuit is that it may be fully integrated on chip with a gate driver, including the sense resistor since the current that flows through it is a small proportion of the main switch's current. Unfortunately, the limited availability and cost of SiC power switches make this method unattractive.

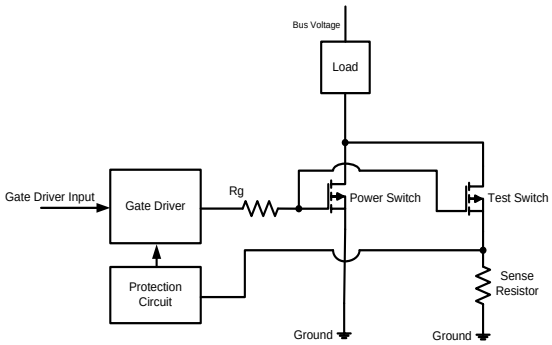

Figure 2. SCP using test SiC switch.

Figure 3 illustrates a straightforward technique by using a sense resistor directly with the source of the SiC switch. Unlike Figure 2, this topology is capable of detecting accurate fault current levels for both SiC MOSFET and JFET power switches. The reference voltage for comparison is hundreds of milli-volts, because the fault signal across the sense resistor is required to be small in order not to affect the conduction performance of the power switch. As a result, an on-chip voltage reference is possible even with a power supply of only a few volts (positive power supply for driving SiC JFET switches). The drawback of this topology is that it requires a very low inductance power resistor to eliminate any unwanted transient response due to the inductance.

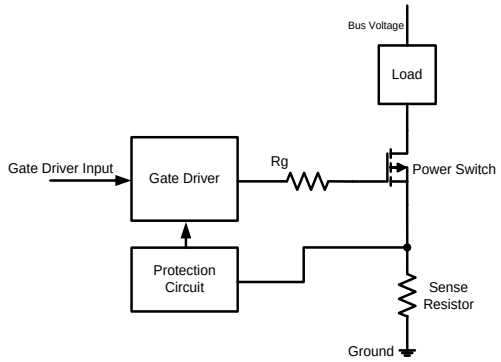

Figure 3. SCP using sense resistor.

III. SHORT CIRCUIT PROTECTION CIRCUIT

This work adopts the resistor sensing method to implement high temperature short circuit protection to take advantage of its flexibility with different power supply schemes for either SiC MOSFET or JFET power devices, as stated earlier.

The block diagram (Figure 4) consists of a voltage reference, a rail-to-rail comparator, an output buffer, and an off-chip resistor. The off-chip resistor is connected in series with the source of the power switch and converts the fault current into voltage. It cannot be integrated on chip since its value is selected based on the fault current level of one specific power switch and will withstand operation current of several amperes. A rail-to-rail comparator is employed to compare the short circuit sensing voltage input to the voltage reference which is generated by the voltage reference block. It is capable of discriminating mV-level signals, and designed with hysteresis for rejecting small nuisance input signals [14]. The output buffer is powered by a 5 V digital supply, and used to output digital fault signals.

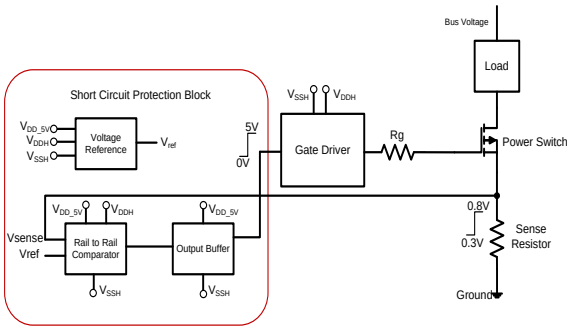

Figure 4. Block diagram of SCP.

The circuit monitors the current through the power switch via the voltage drop across the sense resistor to determine if it exceeds a certain fault level (i.e. 400 mV), and if so, the comparator will quickly detect a fault (i.e. in less than 10 ns) and then send a 5-V digital signal to the output buffer. The buffer is able to distinguish the fault signal from any nuisance current spike. Typically, for a current surge less than several microseconds, it will be filtered by the R-C delay in the buffer. If high current persists, the short circuit fault is identified by the output buffer; fault signal is triggered and sent to core gate driver circuit. This allows the gate driver to turn off the power switch completely in order to protect it from any further damage.

IV. ON CHIP VOLTAGE REFERENCE

An on-chip voltage reference is required in the SCP to be compared with the short circuit sensing voltage. It is kept small because the sensing voltage should not affect the conduction performance of the power switch. A conventional bandgap voltage reference circuit has an output voltage of around 1.2 V [15] [16], which is not suitable in this application.

This work implements a voltage reference with the output of 400 mV over a wide temperature range from 25˚C to 200˚C. It utilizes two series connected and temperature compensated resistors, sourcing a temperature stable current through the resistors. The schematic of this circuit is provided in Figure 5. One p+ extension resistor *R1* and a poly resistor *R2* are connected in series. Since poly resistors have negative temperature coefficient (TC) and p+ extension resistors have positive TC, then properly sizing the resistors relative to one another and sourcing a constant current through them will produce an output voltage that is temperature independent.

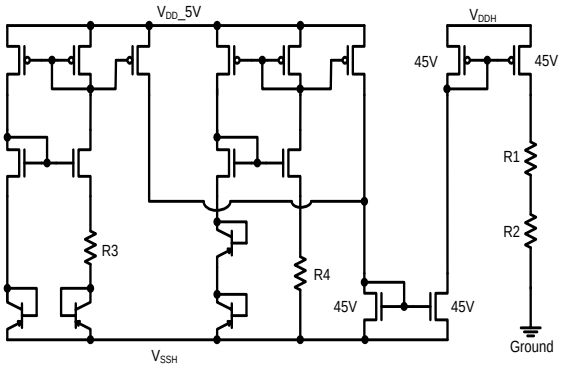

Figure 5. Schematic of voltage reference.

The temperature stable current is generated by combining a PTAT current and a CTAT (Complementary To Absolutely Temperature) current. PTAT current is mirrored from a bandgap voltage reference circuit and CTAT current is created using two stack diode voltages placed across a resistor element. The proposed temperature stable current reference is then the summation of PTAT current and CTAT current. The output current mirror is implemented with high voltage LDMOSFETs for working under different V_{DDH} scenarios, i.e. V_{DDH} changes from 1 V to 30 V. The output current is expressed as

$$I_{ref} = \frac{V_T \ln(N)}{R_3} + \frac{2 \cdot V_{BE}}{K \cdot R_3} \qquad (1)$$

where N is the number of diodes used in the PTAT leg, R_3 and R_4 represent the resistors in the PTAT and CTAT legs, respectively. The resistor ratio R_4/R_3 is defined as K. The effective temperature coefficient of the output current is represented by

$$TCI_{ref} = -TCR + \frac{1}{V_T \ln(N)K + V_{BE}} \left(\frac{\partial V_{BE}}{\partial T} + \frac{\partial V_T}{\partial T} \cdot 2 \cdot K \right) \qquad (2)$$

If the temperature coefficients of the resistors R_3 and R_4 are known, then theoretically, by optimizing the ratio of K and N, the zero temperature coefficient current reference is achieved.

Figure 6 shows the measurement result of the output voltage reference. It indicates a small curvature characteristic with 10-mV change from 25˚C to 200˚C.

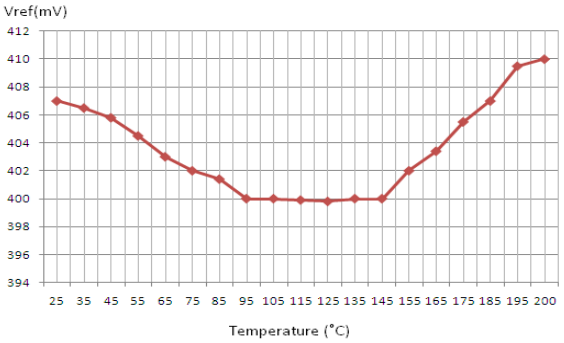

Figure 6. Measurement result of on chip voltage reference.

V. MEASUREMENT RESULTS

Measurements have been conducted over wide temperature range and different power supplies on this short circuit protection circuit.

Figure 7 and Figure 8 show the DC performance of this SCP under both room temperature and 200˚C with power supplies V_{SSH} = −15 V and V_{DDH} = +15 V. The input of sense signal is swept from 300 mV to 500 mV (blue line), while the purple line shows the output of SCP. Note that the switching point and hysteresis of the rail-to-rail comparator in the SCP have less than 15 mV drift over temperature.

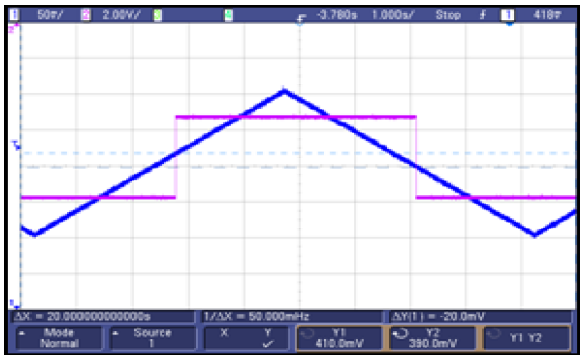

Figure 7. DC performance measurement under room temperature.

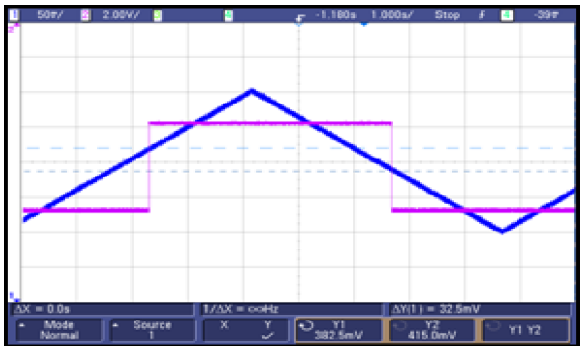

Figure 8. DC performance measurement under 200˚C.

This SCP circuit was tested with a gate driver (GD) core circuit [6] with gate resistor of 4.3 Ω and load capacitor of 10 nF. Figure 9 and Figure 10 provide the transients response under both room temperature and 200˚C with the power supply voltage range of 30 V. The gate driver has been successfully turned "OFF" around 8 µs after the fault current occurs.

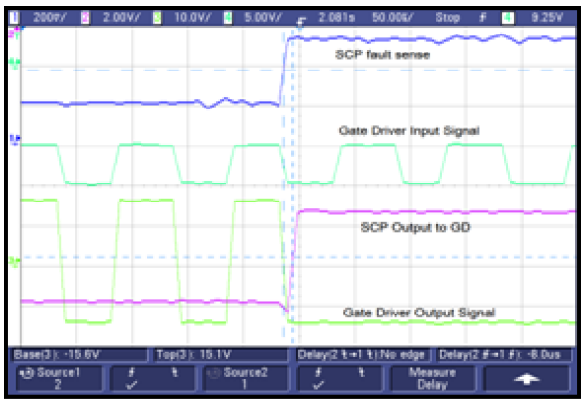

Figure 9. SCP tested with gate driver circuit and 10 nF load capacitor (Room temperature).

Figure 10. SCP tested with gate driver circuit and 10 nF load capacitor (200˚C).

Other power supply schemes (V_{SSH} = −15 V, V_{DDH} = 5 V and V_{SSH} = −3 V, V_{DDH}=7 V) have also been successfully tested to verify the protection function for either normally-ON and normally-OFF power devices.

VI. LAYOUT AND CHIP IMPLEMENTATION

Figure 11 provides the chip micrograph of this high temperature short circuit protection circuit. The total layout area is 0.52 mm^2 (845 µm × 612 µm). To improve the circuit reliability at high temperature, each individual circuit sub block is surrounded by trenches. The chip was packaged in a Kyocera 145-

pin PGA ceramic package to facilitate testing numerous on-chip circuit blocks.

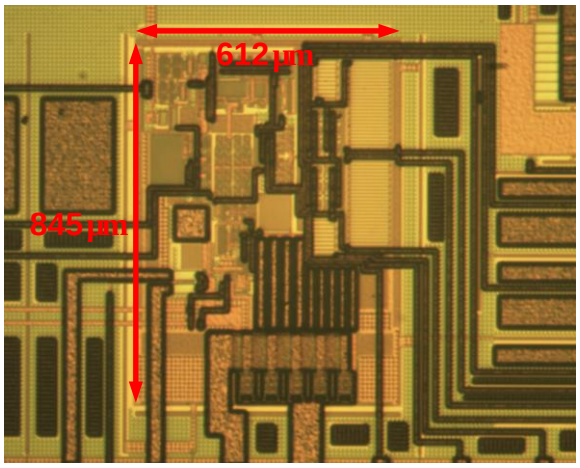

Figure 11. Chip micrograph of short circuit protection.

VII. CONCLUSION

A universal BCD-on-SOI based high temperature short circuit protection for SiC power switches was proposed and fabricated. A full discussion of short circuit behavior, protection methods, and a detailed description of the proposed short circuit protection circuit using the resistor sensing method are presented in this work. The circuit proposed in this work can provide short circuit protection for either SiC MOSFET or SiC JFET power switches over a temperature range of 25˚C to 200˚C. The circuit's reaction time for power switches under fault condition is less than 8 µs over the entire temperature range.

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