# A High-Temperature Folded-Cascode Operational Transconductance Amplifier in 0.8-µm BCD-on-SOI

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**Abstract**

*The rapid growth of the hybrid electric vehicles (HEVs) has been driving the demand of high temperature automotive electronics target for the engine compartment, power train, and brakes where the ambient temperature normally exceeds 150°C. An operational transconductance amplifier (OTA) is an essential building block of various analog circuits such as data converters, instrumentation systems, linear regulators, etc. This work presents a high temperature folded cascode operational transconductance amplifier designed and fabricated in a commercially available 0.8-µm BCD-on-SOI process. SOI processes offer several orders of magnitude smaller junction leakage current than bulk-CMOS processes at temperatures beyond 150°C. This amplifier is designed for a high temperature linear voltage regulator; the higher open-loop gain of this amplifier will enhance the overall performance of a linear regulator. In addition, the lower current consumption of the OTA is critical for improving the current efficiency of the linear regulator and reducing the power dissipation at elevated temperature. A PMOS input pair folded cascode OTA topology had been selected in this work, PMOS input pair offers wider ICMR (input common-mode range) and empirically lower flicker noise compared to its NMOS counterpart. By cascoding current mirror load at the output node, the folded cascode OTA obtains higher voltage gain than the symmetrical OTA topology. The PSRR (power supply rejection ratio) is also improved. A on-chip temperature stable current reference is employed to bias the amplifier. The amplifier consumes less than 65µA bias current at 175°C. The core layout area of the amplifier is 0.16mm$^2$ (400 µm × 400 µm).*

Keywords-high temperature electronics, operational transconductance amplifier, inversion coefficient, temperature stable current reference,

## I. INTRODUCTION

The application of high temperature electronics could be found among well logging, aerospace, nuclear and automotive industries. The high temperature electronics inside hybrid electric vehicles (HEVs) are normally placed under the hood, where the ambient temperature is around 150°C to 200°C [1]. This research presents a high temperature folded-cacode operational transconductance amplifier (OTA) for high-temperature applications such as hybrid electric vehicles.

SOI fabrication processes are more suitable for analog circuits operated at elevated temperature compared to bulk-CMOS fabrication processes thanks to the reduced junction leakage current. As shown in Fig 1,the bulk-CMOS analog ICs will suffer significant performance degradation at elevated temperatures due to the effect of leakage current [2]. In addition to the fabrication process technology, circuit design techniques need to be addressed for high temperature IC design. An important concept for maintaining the linearity of the circuit over temperature is to minimize the temperature coefficient of the biasing current. Stability and matching are also very crucial for amplifiers, voltage regulators, ADCs and oscillators operating at elevated temperature [3]. The goal of this research is to develop a low-power, high gain folded cascode operational transconductance amplifier for elevated temperature. This work utilizes high temperature analog IC design techniques and methodology to design an amplifier; in addition, a temperature stable current reference is utilized to bias this amplifier.

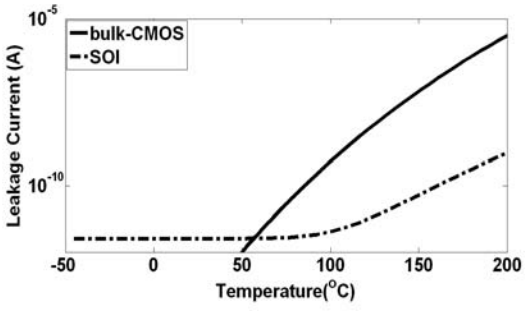


**Fig 1. Simulation of leakage current in Bulk-CMOS and SOI Process**

The design methodology for the folded cascode operational transconductance amplifier is discussed in Section II. Section III presents the temperature stable current reference and voltage reference. Chip implementation is presented in Section IV. Finally, the conclusion is presented in Section V.

## II. Inversion Coefficient Design Methodology

An operational transconductance amplifier (OTA) is the fundamental building block of analog integrated circuits. Its higher open-loop gain will enhance the overall performance of an analog electronic system. The lower quiescent current consumption of the OTA is very important for reducing the power dissipation at elevated temperature. Literatures [4 - 6] propose a $g_m/I_D$ technique to design a high temperature SOI OTA. This work presents a high temperature OTA design based on the inversion coefficient design methodology. The inversion coefficient can offer the circuit designer a meaningful insight in selecting MOSFETs operating in weak, moderate, and strong inversion mode. Optimization of the circuit performance is easily achieved by utilizing the inversion coefficient [7, 8]. In [8], moderate inversion optimizes the tradeoff between gain, speed, and power consumption. Unfortunately, traditional BSIM3V3 models do not characterize moderate inversion operation very well. BSIM3V3 can show a 40% error in moderate inversion operation. However, the EKV-2.6 model offers more accurate modeling in moderate inversion operation [9]. The BCD-on-SOI process technology used in this work employs EKV models; hence, inversion coefficient methodology is utilized in designing the OTA. The fixed normalized inversion coefficient(IC) can be defined as

$$IC = \frac{I_D}{2n_0\mu_0 C_{ox}' V_T^2 (\frac{W}{L})} \quad (1)$$

where $I_D$ is drain current, $n_0$ is the sub-threshold slope factor, $\mu_0$ is the mobility, $C_{ox}$' is gate oxide capacitance, $V_T$ is the thermal voltage, $W$ and $L$ represents the width and the length of the transistor, respectively. Fig 2 provides the simulation result of NMOS ($W$ = 48 µm, $L$ = 2 µm) transconductance efficiency versus. Inversion coefficient from –45°C to 175°C. Fig 3 depicts the simulation result of MOSFET's Early voltage versus temperature from –45°C to 175°C, NMOS, PMOS, and HVNMOS denotes regular NMOSFET, regular PMOSFET and High Voltage NMOSFET, respectively. From Fig 3, the inversion coefficient represents all regions of operation of a MOSFET. The weak inversion (WI) region represents inversion coefficient of less than 0.1, the moderate inversion (MI) lies between the inversion coefficient ranging from 1 to 10, and the strong inversion (SI) indicates inversion coefficient of greater than 10.

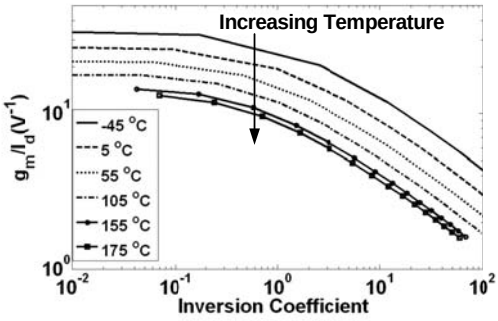


**Fig 2. NMOS transconductance efficiency vs. inversion coefficient**

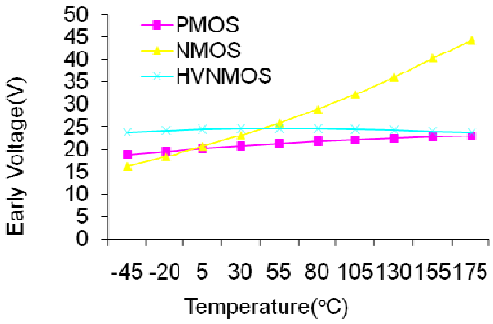


**Fig 3. Simulation of MOSFET's Early voltage vs. temperature for $I_D$ = 15 µA.**

Fig 4 shows the schematic of a PMOS input pair folded cascode OTA. The PMOS input pair offers wider ICMR (input common-mode range) and empirically lower flicker noise than its NMOS counterpart [10]. By utilizing a cascode current mirror load at the output node, the folded cascode OTA has higher CMRR, PSRR and dc gain than simple Miller OTA topology. The DC voltage gain of a folded cascode OTA is expressed as

$$Av(T) \cong \left(\frac{g_{m\_in}}{I_{d\_in}}(T)\right) \cdot (V_{A\_pcas}(T) // V_{A\_ncas}(T)) \quad (2)$$

where subscript "*in*" represents the transconductance of input differential pair, $V_{A\_pcas}$ represents the early voltage of the PMOS cascode current mirror given by

$$V_{A\_pcas}(T) \cong \left(\frac{g_{m\_M9}}{I_{d\_M9}}(T)\right)\left(V_{A\_M9}(T) V_{A\_M11}(T)\right) \quad (3)$$

and $V_{A\_ncas}$ represents early voltage of NMOS cascode current mirror,

$$V_{A\_ncas}(T) \cong \left(\frac{g_{m\_M7}}{I_{d\_M7}}(T)\right)\left(\frac{V_{A\_M7}(T)V_{A\_M5}(T)V_{A\_M3}(T)}{2V_{A\_M3}(T)+V_{A\_M5}(T)}\right) \quad (4)$$

Fig 2 shows that the $g_m/I_d$ parameter decreases with increasing biasing current. This indicates that the devices are moving toward the strong inversion region, resulting in higher power consumption than devices biased in moderate inversion. Fig 3 indicates the Early voltage of NMOS and PMOS is relatively constant over temperature when the biasing current is fixed at 15 µA. In this work, both the input pair and the cascode current mirror are both biased in the moderate inversion region to help optimize power consumption versus performance at elevated temperature. Table 1 gives the aspect ratio, the inversion coefficient and the transconductance efficiency of the amplifier at 175°C. All devices in the OTA are operating within the moderate inversion region (see Table 1). Alternatively, lower power consumption can be achieved by biasing the transistors in weak inversion [6, 7, 8], but at the expense of significantly reduced bandwidth. In addition, the intrinsic device voltage gain, $g_m r_o$, does not include the temperature dependent effects of $g_m$ and $r_o$. By means of the inversion coefficient methodology, the temperature dependence of the voltage gain of the amplifier can be more readily understood.

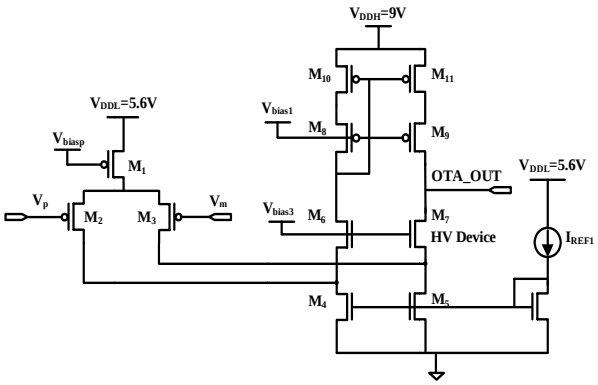


**Fig 4. Folded-Cascode Amplifier**

Notice that the input differential pair and the cascode current mirror load do not share the same supply voltage as in a conventional folded cascode OTA. The PMOS input pair connects to the 5.6-V supply from the on-chip pre-regulator. The cascode current mirror requires higher supply voltage from the on-chip pre-regulator to increase the output voltage swing. The voltage variation at output node may swing from $2V_{DS,\,SAT}$ to $(9\ V - 2V_{SD,SAT})$. HV (25-V) NDMOS ($M_6$, $M_7$) are needed to avoid device breakdown due to excess voltage stress on drain-source terminal (5.5 V). Transistors $M_1$-$M_5$ and $M_8$-$M_{11}$ are regular MOSFET devices.

**Table 1. Aspect ratio, transconductance efficiency and inversion coefficient of OTA at 175°C**

| MOS | Type | W/L (µm/µm) | IC | $g_m/I_d$ |
|---|---|---|---|---|
| $M_1$ | PMOS | 100/2 | ~4.75 | ~7 |
| $M_2$, $M_3$ | PMOS | 200/5 | ~3 | ~6.5 |
| $M_4$, $M_5$ | NMOS | 48/2 | ~3.25 | ~5 |
| $M_6$, $M_7$ | HVNDMOS | 20/1.3 | ~5. 5 | ~10 |
| $M_8$~$M_{11}$ | NMOS | 96/2 | ~2.5 | ~7 |

Fig 5 gives the simulated open-loop DC voltage gain and unity-gain frequency of the proposed OTA versus temperature. The simulated result confirms the DC voltage gain is proportional to the product of $g_m/I_d$ and the Early voltage of the MOSFET. The input pair of OTA consumes 30 µA and the cascode current mirror load consumes another 30 µA. The simulated unity-gain frequency is decreasing with temperature due to mobility degradation at elevated temperature [2, 5].

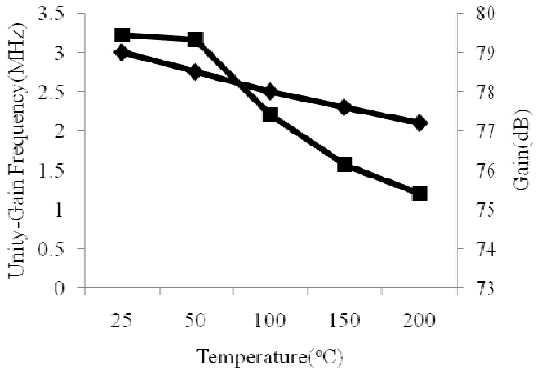


**Fig 5. Simulated OTA DC gain ( -■- ) and unity-gain frequency ( -◆- ) over temperature**

## III. TEMPERATURE STABLE CURRENT REFERENCE AND VOLTAGE REFERENCE

A temperature stable current reference is needed for enhancing the performance of the OTA at elevated temperatures [5]. If the current reference can maintain constant current over temperature, then power dissipation of the OTA will essentially be

independent of temperature. In this work, approximately 120 µA of the quiescent current is consumed by the OTA and the temperature stable current reference.

Several temperature stable current reference design topologies have been proposed and published. This work is targeted to reduce the use of off-chip components. High temperature off-chip passive components are more costly than typical passive components (< 125°C). In addition, the off-chip passive devices add parasitic capacitance to the circuit and require extra PCB real estate overhead.

SOI process technology minimizes the leakage current and extends the operating temperature beyond 125°C. Nevertheless, the circuit design techniques need to be chosen in order to minimize the temperature coefficient of the biasing current over the wide temperature range and reduce the complexity of the design approach.

This work includes a temperature stable current reference circuit (Fig 6) which uses a PTAT (proportional to absolute temperature) current and CTAT (complementary to absolute temperature) current [11]. The CTAT current can be obtained from a diode. The voltage variation with respect to temperature of a diode is about −1.2 mV/°C. Weighted summation of the PTAT current and CTAT current will generate a temperature stable current. Two separate supply voltages (5.6 V and 9 V) are connected to the input differential pair of the OTA and the current mirror load, respectively. Therefore, two separate temperature stable current reference circuits are required. The lower voltage current reference ($I_{ref1}$) is designed to bias the input pair of the OTA. The effective temperature coefficient is expressed as

$$TCI_{REF} = -TCR + \frac{1}{V_T \ell n(N) K + V_{BE}} \left( \frac{\partial V_{BE}}{\partial T} + \frac{\partial V_T}{\partial T} \cdot 2 \cdot K \right) \quad (5)$$

where $N$ is the number of diode used in the PTAT leg and $R_1$, $R_2$ represent the resistors in the PTAT and the CTAT legs, respectively. The ratio of the resistor $R_2/R_1$ is defined as $K$. If the temperature coefficients of the resistors $R_1$ and $R_2$ are known theoretically by optimizing the ratio of $K$ and $N$, the zero temperature coefficient temperature stable current reference is achieved.

The measured current variations of the low-voltage current reference ($I_{REF1}$ nominal 13 µA) and high voltage current reference is ($I_{REF2}$ nominal 27 µA) is about 7% and 6% from 25°C to 175°C, respectively, shown in Fig 7. This current reference circuit has been tested up to 200°C; 25°C above the maximum temperature the fabrication process suggested (175°C).

The bandgap reference (BGR) circuit provides the reference voltage. The output reference voltage of BGR is expressed as:

$$V_{REF} = 2V_{BE} + 2\frac{R_2}{R_1} \cdot V_T \cdot \ln K \quad (6)$$

Here, $V_{BE}$ is the base-emitter voltage of the bipolar, $V_T$ is thermal voltage, and $K$ is the number of diodes in parallel; $R_1$ and $R_2$ are the resistors in the proportional to absolute temperature (PTAT) leg and the output reference voltage leg of the BGR circuit. The second term of $V_{REF}$ is used to cancel the negative temperature coefficient (TC) of the diodes.

Fig 8 shows the measured reference voltage variations over temperature from 25°C to 200°C. The maximum reference voltage variation is about 3% from 25°C to 200°C.

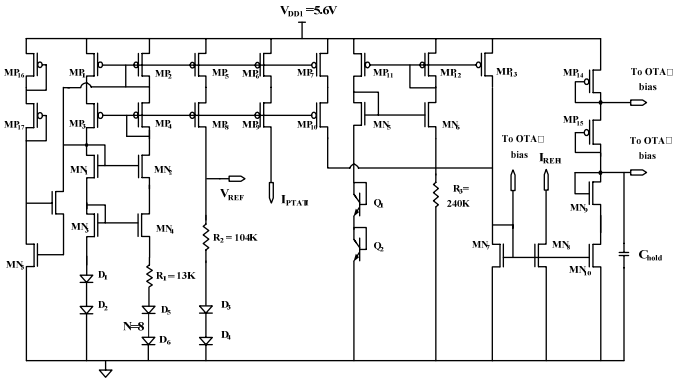


**Fig 6. Schematic of the BGR and the temperature stable current reference ($I_{REF1}$).**

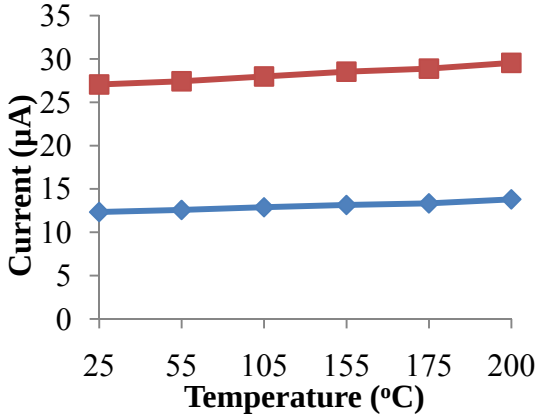


**Fig7. Measured current variation of $I_{REF1}$ and $I_{REF2}$ over temperature.**

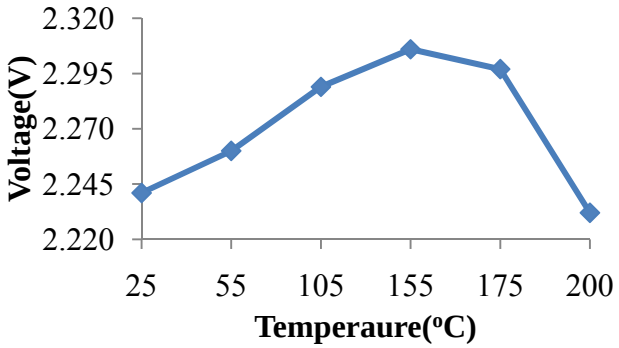


**Fig 8. Measured reference voltage, $V_{REF}$, over temperature.**

## IV. Layout and Chip Implementation

Fig 9 shows the chip micrograph of the high temperature folded cascode operational transconductance amplifier (OTA). The total layout area of the amplifier, including temperature stable current reference and pre-regulator, is 1.92 $mm^2$ (1,600 µm × 1,200 µm); the core layout area of the amplifier is 0.16$mm^2$ (400 µm × 400 µm). To alleviate electron migration at high temperatures, metal interconnections were drawn 1.5X wider than the foundry's design rules required. Each individual sub block is surrounded by trench, and the chip was packaged in Kyocera DIP-40 ceramic package.

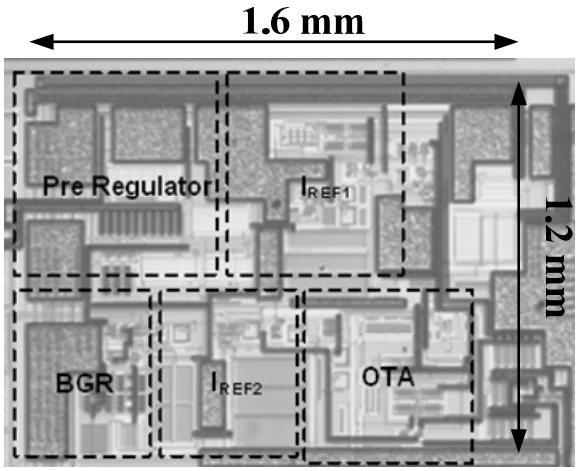


**Fig 9. Chip micrograph of high-temperature folded cascade OTA.**

## V. Conclusions

A high-temperature folded cascade operational transconductance amplifier chip has been designed and fabricated. A detail description of the high temperature design techniques and the implementation of the high temperature/voltage folded cascade OTA in BCD-on-SOI process are presented in this paper. The amplifier consumes a total of 65 µA bias current at 175°C; the lower bias current can reduce the power dissipation at elevated temperature. In addition, a temperature stable current reference stabilizes the gain of the OTA across temperature.

This folded cascade amplifier is utilized as an error amplifier of a high temperature linear voltage regulator. The amplifier can also be utilized in other high temperature electronics (such as sensors, data converters, etc.) whereas a typical bulk-CMOS amplifier cannot provide the circuit performance as that achievable in SOI [12] beyond 125°C.

## Acknowledgment

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## References

[1] M.A. Huque, S.K. Islam, B.J. Blalock, C. Su, R. Vijayaraghavan and L.M. Tolbert, "Silicon-on-Insulator Based High-Temperature for automotive applications," IEEE International Symposium Industrial Electronics, pp. 2538-2543, June 30, 2008.

[2] F. Shoucair, "Design Consideration in High Temperature Analog CMOS Integrated Circuits," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. 9, issue 3, Sep 1986.

[3] T. Romanko, "Extreme Design: Developing integrated circuits for -−55ºC to +250ºC" www.honeywell.com/hightemp.

[4] D. Flandre, L. Demeus, V. Dessard, A.Viviani, B. Gentinne, J.-P. Eggermont, "Design and application of SOI CMOS OTAs for high–temperature environments," IEEE Transactions on Circuits and Systems: Analog and Digital Signal Processing, Vol. 49, 2002.

[5] J.-P. Eggermont, D. De Ceuster,D. Flandre, B. Gentinne, P.G.A. Jespers, J.-P. Colinge, "Design of SOI CMOS operational amplifiers for applications up to 300°C," IEEE Journal of Solid-State Circuits, Vol. 31 , issue.2 , 1996

[6] F. Silveira, D. Flandre, P.G.A. Jespers, "A $g_m/I_D$ based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," IEEE Journal of Solid-State Circuits, Vol. 31, No.9, Sept. 1996.

[7] D.M Binkley, "Tradeoffs and Optimization in Analog CMOS Design," 14th International Conference on Mixed Design of Integrated Circuits and System. pp. 47-60, 21-23 June 2007.

[8] D. M. Binkley, "Tradeoffs and Optimization in Analog CMOS Design" Wiley, August 2008.

[9] S. C. Terry, J .M. Rochelle, D. M. Binkley, B. J. Blalock, D. P. Foty, M. Bucher, "Comparison of a BSIM3V3 and EKV MOSFET model for a 0.5 µm CMOS process and implications for analog circuit design," IEEE Transactions on Nuclear Science, Vol. 50, Issue 4, part 1, pp.915 - 920 Aug. 2003.

[10] Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design," Oxford University Press, USA; 2 edition, 2002.
[11] D. A Badillo. "1.5V CMOS current reference with extended temperature operating range," IEEE International Symposium on Circuits and Systems, Vol.3, pp.III-197 - III-200, 26-29 May 2002.
[12] D. Flandre, J.-P. Eggermont, D. De Ceuster, P. Jespers, "Comparison of SOI versus bulk performances of CMOS micropower single-stage OTAs," Electronics Letters Vol. 30, Issue: 23, pp. 1933 – 1934, 1994.