4H-SiC GTO Thyristor and p-n Diode Loss Models for HVDC Converter

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Abstract— **The increase in use of power electronics in transmission and distribution applications is the driving force for development of high power devices. Utility applications like FACTS and HVDC require cost effective and highly efficient converters with high power ratings. SiC power devices have some exceptional physical properties that make them highly reliable at high power, high temperature, and high frequencies. This paper presents the modeling of temperature dependent 4H-SiC GTO thyristor and p-n diode loss models. The conduction and switching losses of the devices for various operating conditions have been simulated and compared for SiC and Si devices. These loss models are integrated with an HVDC transmission system to study the effect of Si and SiC devices on the system in terms of system efficiency and system cost management.**

I. INTRODUCTION

As the utility industry is undergoing expansion and deregulation, more focus has been on reliability and efficient utilization of the existing power systems. Also, the demand has increased for economical operation of the transmission systems, which involve high operational costs. Implementing power electronic circuits has provided solutions to meet these challenges and has resulted in improved performance of the systems. High Voltage DC (HVDC) transmission and Flexible AC Transmission Systems (FACTS) are the widely recognized power electronic applications in the transmission and distribution industry. HVDC systems and FACTS applications like Voltage Source Converter (VSC) transmission, back-to-back ties based on VSC technology have been installed successfully in several locations worldwide. It is important to develop new devices and improve the characteristics of the devices such that they are efficient in their electricity conversion. VSC technology is an emerging technology, and uses high power devices like GTOs, GCTs, IGCTs, IGBTs. GTOs have high blocking voltage and current handling capability. They are suitable for high power dc applications due to low on-state losses, and are free from oxide interface problems. However, GTO suffers from high switching losses due to long tail current.

The high power converters also require diodes, which match the main switches in power ratings and should be able to switch faster. Si devices are limited in breakdown voltages and have higher lifetimes due to the material limitations of Si.

SiC bipolar devices have the potential to block voltages up to 25 kV because of the high electric field strength of the SiC material. SiC p-n diodes rated at 19 kV have been reported in [2]. They can operate at high junction temperature because of the wide band gap of SiC. They also have low thermal resistivity because of the high thermal conductivity of SiC. Thus, SiC devices can operate at high power densities because of faster heat dissipation of the device. The switching losses in SiC GTO thyristors are less because of reduced drift region width and hence can be switched faster. SiC p-n diodes have been reported to have on-state voltage drop and switching speeds comparable to ultra fast switching Si diodes [15]. Their switching losses are almost constant with increase in temperature ensuring reliable operation. System cost and system efficiency are affected by the performance of the GTO thyristor and p-n diodes stacked in the valves.

To study the impact of a device at the system level and to realize the benefits of using the device, its detailed device model is required. GTO thyristor and p-n diode loss models have been developed using power loss equations derived based on device behavior during conduction and switching modes of operation. The loss models were interfaced with a HVDC transmission system model to study the comparison of the Si and SiC devices on the system efficiency and cost savings.

II. DIODE LOSS MODEL

A. Static losses

The static power dissipation in a diode can be expressed as function of forward and reverse leakage current densities J_f, J_r, forward and reverse voltages V_f, V_r, which correspond to the power dissipation in forward conduction and reverse blocking states [14].

$$P_{static} = (J_f \cdot V_f + J_f^2 \cdot R_{on}) \cdot d + J_r \cdot V_r (1-d) \tag{1}$$

$$R_{on} = \frac{(V_b / E_c)}{q \cdot \mu_n \cdot N_D + \dfrac{(\mu_n + \mu_p) J_f \cdot \tau_a}{(V_b / E_c)}} \tag{2}$$

where d is the duty cycle and R_{on} is the specific resistance of

the drift region. The leakage current in SiC p-n diodes is negligibly low due to low thermal generation rate; hence, the second term in the equation can be neglected. Table I gives a list of the variables used in the equations found in this paper.

B. Dynamic losses

The turn-on energy losses of a p-n diode are negligible compared to turn-off losses, which are the main losses. The energy dissipated during the turn-off is dependent on the charge stored during the forward conduction of the diode. The charge stored is a function of the ambipolar lifetime τ_a and the forward current density. The switching losses of a p-n diode can be modeled as [14],

$$P_{sw} = J_f \cdot \tau_a \cdot V_r \cdot f_s \qquad (3)$$

III. GTO THYRISTOR LOSS MODEL

A. Conduction Losses

The on-state power loss is mainly due to conduction losses, and for a GTO thyristor the on-state power loss equation has been derived to be [8],

$$P_{on-state} = J \cdot (E_g/q) + J \cdot (3\pi/8) \cdot (kT/q) \cdot \exp(3V_B/2L_aE_c) \qquad (4)$$

In (4), the first term in the sum corresponds to the loss due to the voltage drop across the junction, and the second term corresponds to the voltage drop due to on-state specific resistance in the lower base region. This equation can further be simplified and reduced to an expression that is dependent on fewer parameters.

$$P_{on-state} = J \cdot (E_g/q) + J \cdot (3\pi/8).(kT/q).\exp(D) \qquad (5)$$

where,

$$V_B = \varepsilon(N_a + N_d) \cdot E_c^2 \big/ (2q \cdot N_a \cdot N_d) \qquad (6)$$

$$\tau_a = \tau_n + \tau_p \qquad (7)$$

$$L_a = (D_a \cdot \tau_a)^{0.5} \qquad (8)$$

$$D_a = 2 \cdot D_n \cdot D_p \big/ (D_n + D_p) \qquad (9)$$

$$D_n = (kT/q) \cdot \mu_n \qquad (10)$$

$$D_p = (kT/q) \cdot \mu_p \qquad (11)$$

$$D = (\varepsilon(N_a + N_d) \cdot E_{bd} \cdot 1.5) / (2 \cdot q \cdot N_a \cdot N_d \cdot \sqrt{(KT/q)}(\mu_n \cdot \mu_p) \cdot \tau_a / (\mu_n + \mu_p)) \qquad (12)$$

B. Switching Losses

The equations for energy losses, during turn-on and turn-off operations, are shown in (13) and (14) below [8]. During turn-on, it is assumed that the turn-on gain is very high,

$$E_{off} = 1/2 \cdot (\varepsilon_s \cdot E_c V/(1 - \alpha_{\overline{npn}})) \sqrt{V/V_B} + J\alpha_{npn,max} \cdot \tau_a \qquad (13)$$

$$E_{on} = 1/3 \cdot \varepsilon_s \cdot E_c V \sqrt{V/V_B} + J^2 \cdot (3\tau_a \cdot V_B^2)/(\varepsilon_s \cdot \mu_n \cdot E_c^3) + (E_g/2q) \cdot J\tau_a \qquad (14)$$

hence it can be assumed that the current rise is very fast. During the turn-off period, assuming unity gain turn-off, the energy loss equation is derived as an open base npn

Table I: Explanation of Symbols

k	Boltzmann constant (J/K)
v_s	electron saturation velocity (cm/s)
V_B	breakdown voltage (V)
D_a	ambipolar diffusion coefficient (cm²/s)
D_n, D_p	electron and hole diffusion coefficients (cm²/s)
N	electron concentration (cm⁻³)
q	electron charge (C)
E	electric field (V/cm)
E_c	avalanche breakdown electric field (V/cm)
E_{on}, E_{off}	turn-on and turn-off losses (J/cm²)
J	current density (A/cm²)
L_a, L_n	ambipolar and electron diffusion lengths (cm)
$P_{on-state}$	on-state losses (W·cm⁻²)
V	applied voltage (V)
$\alpha_{\overline{npn}}$	average current gain during voltage rise
R_{sp}	ideal specific on-state resistance (ohm·cm²)
N_A, N_D	acceptor and donor concentrations (cm⁻³)
$\alpha_{npn,max}$	maximum common-base current gain for a given applied voltage
α_{npn}	average common-base current gain when applied voltage
ε_S	varies from 0 to V permitivity of the semiconductor (F/cm)
μ_n, μ_p	electron and hole mobility (cm²/V·s)
τ_a	ambipolar carrier lifetime (s)
τ_n, τ_p	electron and hole lifetimes (s)

transistor turn-off and also assuming that the entire anode current flows to the gate terminal [8].

The switching power losses can be calculated using the total energy loss equation as,

$$P_{switching} = (E_{on} + E_{off}) \cdot f_s \qquad (15)$$

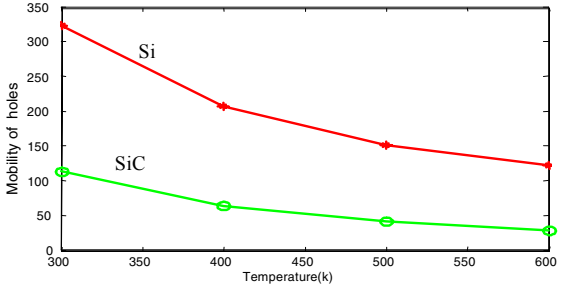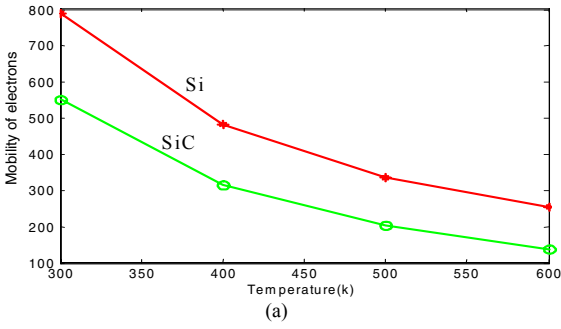The total power loss in the device is given as,

$$P_{total} = P_{conduction} + P_{switching} \qquad (16)$$

IV. MOBILITY MODEL

The loss model equations of the p-n diode and GTO thyristor are dependent on doping densities, mobilities, temperature, and applied voltage and current. For a given operating voltage and current, the model behavior varies with temperature because the electron and hole mobilities vary with temperature. In addition, the doping density is fixed for a desired rating of the device. A temperature dependent mobility model is used in the loss models. The equations used in the mobility model are given in [9] as,

$$\mu_o = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_D + N_A}{N_{ref}}\right)^\alpha} \qquad (17)$$

where $N_A + N_D$ is the total doping concentration, μ_{max} and μ_{min} are the minimum and maximum mobilities of electrons and holes, N_{ref} is the doping concentration for p-type and n-type materials calculated empirically, and α is the curve fitting parameter measure of how quickly the mobility changes from μ_{min} to μ_{max}.

Fig. 1. Mobility calculation of (a) electrons and (b) holes for Si and SiC.

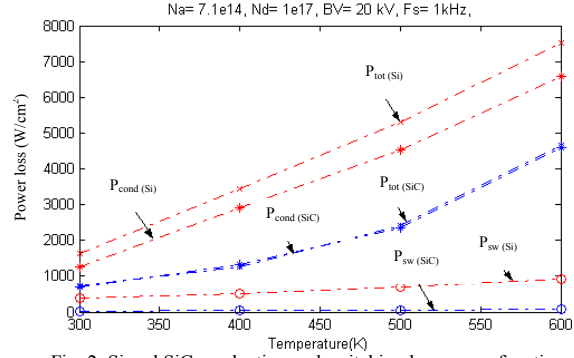The temperature dependence of the mobility model can be calculated as,

$$\mu = \mu_o \times \left(\frac{T}{T_o}\right)^{\gamma} \quad (18)$$

$$\mu^E(E) = \mu \left/ \left(1 + |\mu E / v_s|^{\beta}\right)^{\frac{1}{\beta}}\right. \quad (19)$$

where μ_o is the mobility at room temperature T_o, γ is a constant and varies from -1.8 to -2.5 for n-type and p-type SiC materials, E is the applied electric field, V_s is the saturation velocity, and β is a constant. The data used to calculate the mobilities are given in Table II [9], [10], [11]. Fig. 1 shows the variation in the mobility of the electrons and holes as a function of temperature.

V. SIMULATIONS

The loss models developed were simulated to study the device behavior for different operating conditions. The SiC devices are doped for a desired breakdown voltage $V_B = \varepsilon(N_a + N_d) \cdot E_c^2 / (2q \cdot N_a \cdot N_d)$ [12] and are rated at 20 kV. The Si GTO thyristor is rated at 5000V, and for comparison, four Si devices are assumed to be connected in series to achieve the same required voltage-blocking rating. The model is studied for variation in temperature for different current and voltage ratings. The frequency of operation is 1 kHz and the model was tested for a temperature range of 300 K – 600 K. It should be noted that the Si GTO thyristor cannot withstand more than 423 K; however, the model is tested at elevated temperatures for comparison purposes. The devices are subjected to a current density range of 100 A/cm^2 – 500 A/cm^2 and the duty cycle is assumed to be 50%. The data used in simulation is shown in Table III [13].

Fig. 2. Si and SiC conduction and switching losses as a function of temperature for J=200 A/cm^2, V= 5000V.

A comparison plot of different losses of Si and SiC devices is shown in Fig. 2. Conduction losses dominate because at lower switching frequency the switching losses are low, and the main power loss is a function of on-state resistance. Si GTO thyristor conduction losses are more than the SiC GTO thyristor conduction losses, primarily because of the difference in the on-state specific resistance. It is found that the conduction losses of the Si GTO thyristor are at least double that for the SiC device. The switching losses of SiC GTO thyristor are at least 12 times less than the Si device.

Table II: Parameters Used in Mobility Model

	Si	4H-SiC
Minimum and maximum electron mobility, $\mu_{minn,}$ μ_{maxn}, [cm^2/V·s]	65, 1360	50, 950
Minimum and maximum hole mobility, $\mu_{minp,}$ μ_{maxp} [cm^2/V·s]	50, 505	10, 180
Electron and hole ionization coefficients, α_n α_p	0.91, 0.63	0.76, 0.56
Reference electron and hole concentrations, $N_{refn,}$ N_{refp} [cm^{-3}]	8.5 x10^{16} 6.3 x10^{16}	2.2x10^{17} 2.3x10^{17}

This noticeable difference between the switching losses of Si and SiC devices is mainly because for the same blocking voltage, the thickness of the blocking layer in a Si device is more than that of a SiC device. The thinner blocking layer thickness in SiC devices is because of the higher electric breakdown strength of SiC material due to wide bandgap. Thus, the charge stored in the drift region is less, which results in faster switching. The lower conduction and switching losses of SiC devices show that they have high efficiencies compared to Si devices. The diode loss model is not discussed as it has been extensively studied in several papers. However, the simulations were conducted on diode model for several operating conditions. The switching losses of SiC p-n diode rated at 20kV are less compared to Si diode rated at 5kV. However, the conduction losses of SiC p-n diode were high compared to Si p-n diode for different temperatures. This is because of the higher R_{on} due to higher rating of the device.

VI.   HVDC SYSTEM

The configuration chosen for the study is a monopolar configuration, and the transmission system is based on voltage source converter technology. The converters at both

Table III. Simulation Data

Parameter	4H-SiC	Si
(E_g), Energy gap (eV)	3.2	1.11
ε_r, relative permitivity	9.7	11.8
E_c, critical electric field (V/cm)	2.3×10^6	0.3×10^6
V_{sat}, saturation velocity (cm/s)	2×10^7	1×10^7

ends are voltage source converters also known as forced commutated converters. The converter configuration is a two-level, six-pulse three-phase full bridge converter and the arrangement is as shown in Fig. 3. The system model is designed to emulate the ac characteristics, and it is assumed that one substation is the sending end and the other is the receiving end.

A.   Simulation Specifications

- System ratings: 120 kV dc link, up to 75 MW delivered to the receiving end.
- Device ratings: SiC– 20kV, 200 A/cm^2; Si– 5kV, 200 A/cm^2
- The model is tested for a temperature range of 27° – 200^oC. The maximum value of 200^oC was chosen to evaluate the SiC device losses above the maximum operating temperature (150^oC) of Si device.
- Simulation is initialized using steady state operating values.
- The system frequency is 60 Hz, GTO thyristor switching frequency is 2 kHz.

B.   System Simulations

The system model described in earlier sections and the control systems have been implemented using PSCAD/EMTDC software. PSCAD/EMTDC is a simulation tool for analyzing power systems. PSCAD is the graphical user interface and EMTDC is the simulation engine. This software is most suitable for simulating the electromagnetic transients of the electrical systems. It also has the feature of interfacing MATLAB/SIMULINK, and hence has the flexibility of interfacing various MATLAB/SIMULINK models. The device models, which were discussed in the earlier sections, have been interfaced with the HVDC system model. This system model has been developed for the specifications listed in the previous section. A program was written in FORTRAN 99 to interface the SIMULINK device models.

VII.   RESULTS

The power loss profiles are obtained from system model simulations. The losses are a function of the conduction current and vary proportionally with the square of current. The current flows through the diode when there is a power reversal, and the current through the GTO thyristor is zero. The GTO thyristor losses are dominant losses as it is the main power switch. Also, it was shown that switching losses of GTO are less compared to conduction. This is because the switching frequency is low and thus the switching losses are less compared to the conduction losses. However, for the same switching frequency, the losses are more for a Si GTO thyristor than a SiC GTO thyristor. The total loss of SiC GTO thyristor is less than Si GTO thyristor as expected,
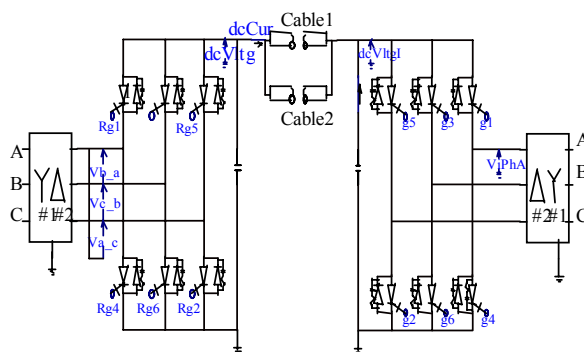

Fig. 3. Converter configuration of system model.

since the on-state resistance of Si GTO thyristor is more than that of a SiC GTO thyristor. As mentioned earlier, switching losses of the diode are dominant losses. However, the switching losses of SiC diode are less compared to Si diode. The losses increase with an increase in temperature due to the increase in on-state resistance. The loss profiles obtained for diodes and GTOs were used to calculate the system efficiency and system cost savings.

A.   Efficiency Calculation

The efficiency is calculated based on the power loss profile obtained at different operating conditions. The instantaneous losses are a function of the instantaneous current. The instantaneous current depends on the modulation index and the switching angles generated by the PWM-based controller. The average loss over several cycles of the fundamental is calculated to find the power loss. The average power loss for Si and SiC GTO thyristors and diodes is shown in Fig. 4. The average power loss for a single device over a few cycles is measured from the plots, and the corresponding converter efficiency is calculated. The efficiency calculations are based on the dc power in the dc link, average loss in the devices, and the number of devices in the converter.

$$\text{Efficiency} = (P_{dc} - P_{loss})/ P_{dc} \qquad (20)$$

$$P_{loss} = P_{avg} \cdot (n_t) \qquad (21)$$

Total number of devices
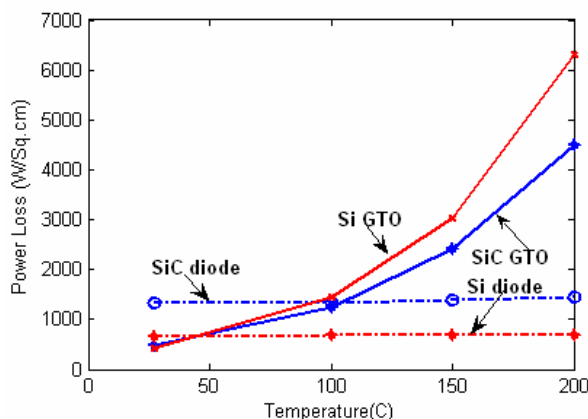
$$n_t = (n_v) \cdot (n_c) \cdot 6 \qquad (22)$$

Fig. 4. Average loss profiles for SiC and Si devices.

Table IV. Efficiency of Si Converter

Temp (K)	$P_{loss,GTO}$	$P_{loss,diode}$	Eff %
300	433.3	672.26	98.54
373	1443.1	674.12	97.32
423	3041.2	675.03	95.40
473	6301..9	676.40	91.49

Table V. Efficiency of SiC Converter

Temp (K)	$P_{loss,GTO}$	$P_{loss,diode}$	Eff %
300	475.2	1326.8	99.37
373	1245.6	1344.9	99.14
423	2402.1	1392.0	98.77
473	4506.9	1451.8	98.12

Table VI. Efficiency of Hybrid Converter

Temp (K)	$P_{loss,GTO}$	$P_{loss,diode}$	Eff %
300	433.3	1326.8	99.00
373	1443.1	1344.9	97.78
423	3041.2	1392.0	95.84
473	6301..9	1451.8	91.92

Where, P_{avg} is the average loss of a single device, P_{loss} is the total losses of the converter, n_t is the total number devices in the converter, n_v is the number of devices in series, and n_c is the number of devices in parallel.

Table IV shows the efficiencies of a Si converter for an HVDC interface; Table V shows efficiencies of a SiC converter, and Table VI shows the efficiencies of an hybrid converter which has Si GTOs and SiC p-n diodes. The efficiency plots of the converters are shown in Fig. 5. The efficiency of the SiC converter is higher compared to Si converter and the difference becomes significant at higher temperatures. This is because of the difference in losses of the SiC and Si devices. There is marginal difference between the Si converter and the hybrid converter efficiency. This is because the Si diodes which are rated at 5kV are replaced by SiC diodes rated at 20kV. Hence, the loss per SiC diode is higher due to the higher blocking voltage of the device as shown in Fig. 4. However, it should be noted that the number of SiC devices used in the converter is less compared to the Si converter, which results in system savings. Also, a small increase in efficiency of the SiC at different temperatures is a significant factor considering the fact that several megawatts of power being delivered.

B. System Cost

The system cost savings is calculated based on the power loss profile obtained for different operating conditions. The cost savings was calculated for different ratings of the devices at 100°C.
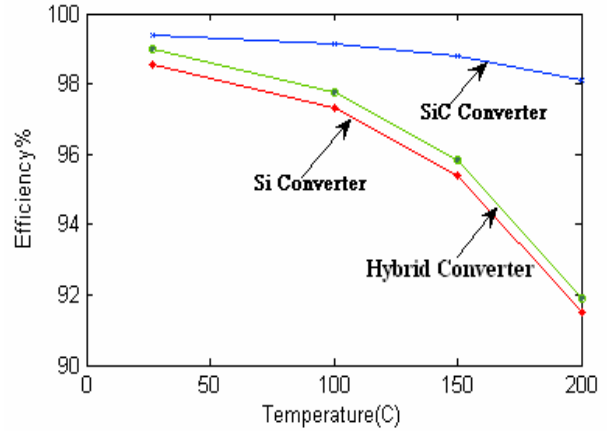

Fig. 5. Efficiency plot for different converters.

Savings Calculation:

Difference in losses,

$$\Delta P_{loss} = (P_{(loss, Si)} \times n_t) - (P_{(loss, SiC)} \times n_t) \qquad (23)$$

Converter operates for 365 days/year and 24 hours/day:

Difference in energy loss/year,

$$\Delta E_{loss}/yr = \Delta P_{loss} \times 365 \times 24 \qquad (24)$$

Assuming a rate of $0.04/ kW·hr:

$$Savings/year = (\Delta E_{loss}/yr) \cdot (\$0.04) \qquad (25)$$

where, $P_{(loss, Si)}$ is the average power loss per device in the Si converter, $P_{(loss, SiC)}$, is the average loss per device in the SiC converter, and n_t, is the total number of devices used in the converters.

Table VII shows the values of cost savings for converters with SiC devices rated at 20kV, 200 A/cm^2 and Si devices rated at 5kV, 200 A/cm^2. As seen in Table VII using SiC GTO thyristor and p-n diodes rated at 20kV, 200 A/cm^2 results in significant system cost savings over a year. Even though the average loss per device for a SiC diode is higher, the cost savings achieved by replacing Si diodes with SiC diodes is significant. The total number of Si devices used to achieve the system power rating is 1560 and the total number of SiC devices used is 396.

The ratio of number of devices in the SiC converter compared to the Si converter is less because SiC devices have a higher voltage rating compared to Si devices. Thus, the reduction in number of devices results is operational cost savings. Even though SiC devices are expensive, the operational cost savings and the less number of devices required supercede the cost of the devices. With fewer devices, less auxiliary components like snubber circuit, reactors, and capacitors required and the installation costs will be less. Hence, the overall system cost will be reduced. The complexity of the system control is also reduced to a great extent with the reduction in number of devices.

Table VII. System Cost Savings with Different Converters

Converter	Average Losses	kW-hr/year	Cost Savings
Si/SiC	1091kW	9,553,537 kW-hr	$ 382,141
Si/Hybrid	275 kW	2,486,215 kW-hr	$ 96,249

It was also shown in the previous section that the efficiency of a converter with SiC devices is higher compared to a Si converter. This illustrates that the higher rating and higher temperature handling capability of SiC devices results in the better performance of the system.

VIII. CONCLUSIONS

Based on the simulation results presented in this paper, the system cost savings can be reduced, and system efficiency can be improved if the number of devices required is less. It was shown that SiC devices with higher blocking voltages can replace Si devices in ratio of 1:4, thereby reducing the system operational costs and complexity. SiC devices also have low losses compared to Si devices at higher temperatures because of the higher thermal conductivity. Hence SiC devices improve the system performance compared to Si devices. The high temperature operation results in increased power density and reduced thermal management requirements. Additionally, the device operating area limits can be improved due to reduced losses; hence, the maximum switching frequency can be increased for high power densities. The use of VSC technology demands highly efficient converters with higher power devices with minimal losses. The HVDC system model study revealed that the SiC-based converter is more efficient compared to the Si-based converter. Thus using high power SiC GTO thyristors and p-n diodes, the system cost savings can be improved. Hence, it can be concluded that with improved current density of SiC devices and when they become commercially available, they can effectively replace the conventional Si based converters.

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