Performance of "Ultra-High" Efficient Electronic Ballast for HID Lamps Using SiC Devices

Lakshmi R. Gopi Reddy[1], Leon M. Tolbert[1], Hui Zhang[1], Tom F. Cheek, Jr.[2]
lgopired@utk.edu, tolbert@utk.edu, hzhang18@utk.edu, tomcheek@flash.net

[1]The University of Tennessee
Electrical and Computer Engineering
414 Ferris Hall
Knoxville, TN 37996-2100, USA

[2]EPIC Systems, Inc.
10503 Forest Lane
Suite 140
Dallas, TX 75423, USA

***Abstract*—A new electronic ballast circuit for High Intensity Discharge (HID) lamps to achieve an "ultra" high efficiency of 95% is proposed in this paper. The first stage of the ballast which is the power factor correction boost converter has demonstrated an efficiency of >97% using Si MOSFET as the switch. The second stage of the ballast, a DC to high frequency inverter has been designed to achieve >98% efficiency. Thus the overall efficiency of the ballast is expected to be >95%. The performance of the "ultra high" efficient electronic ballast when SiC MOSFETS are used is discussed in the paper. A loss model has been developed to compare the efficiency of the electronic ballast when using Si or SiC devices.**

Index Terms—**Electronic ballast, HID lamps, resonant inverter, power loss modeling, Silicon Carbide (SiC).**

I. Introduction

High Intensity Discharge (HID) lamps make a major impact on lighting and energy consumed in lighting. The HID lighting systems can be made more efficient by improving the ballast energy efficiency and by providing flexible energy-saving features. Therefore, an opportunity to provide an impact on the illumination efficiency of the various lighting sectors such as industrial, residential, commercial, etc., is significant. Innovative power electronics technology and optimum circuit design are considered to improve efficiency of the ballast in the power range of HID wattage.

HID lamps, like fluorescent lamps require high voltages to initiate discharge and also current limitation after start-up. These features are implemented in the electronic ballast. Electronic ballasts have advantages of reduced weight, lower losses, quiet operation, and improved control over magnetic ballasts which are generally inexpensive, simple, and reliable. Electronic ballasts are more expensive and may offer less reliability than magnetic ballasts.

An electronic ballast for an HID lamp in general can be divided into two stages: 1) Power factor correction, and 2) high frequency driver stage. The first stage consists of an input filter (for EMI reduction) and a full bridge rectifier that converts the input rms voltage into DC voltage. The rectified voltage is then fed through a power factor correction (PFC) circuit that maintains the power factor of the system to unity thereby improving the efficiency. The PFC consists of a dc-dc converter where in the switching device is controlled so as to maintain the phase difference between the input current and voltage to almost zero. The second stage consists of a DC to high frequency inverter with resonant tank circuit at the output to drive the lamp. Fig. 1 illustrates the electronic ballast structure in block diagram.

Several ballast designs have been proposed in the literature for low-power lamps and also high power lamps [1-3,19,20]. Ref [20] describes an electronic ballast design that achieves 96% efficiency but at low lamp powers of around 33 watts. A similar design at high output powers is used in this design. Among the 250 watt electronic ballast designs, no efficiencies greater than 92% were reported [2, 19].

In this paper, a half-bridge inverter with parallel resonant circuit is proposed to be used. The efficiency in the first stage of the ballast is >97% and an efficiency of >97% is expected in the second stage, thereby obtaining an overall "ultra-high" efficiency of >95% for the ballast.

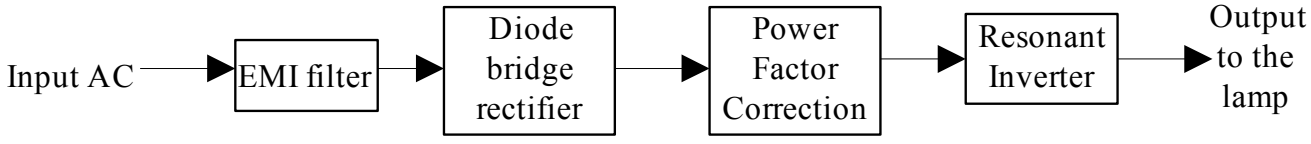


Fig. 1. Block diagram representation of electronic ballast

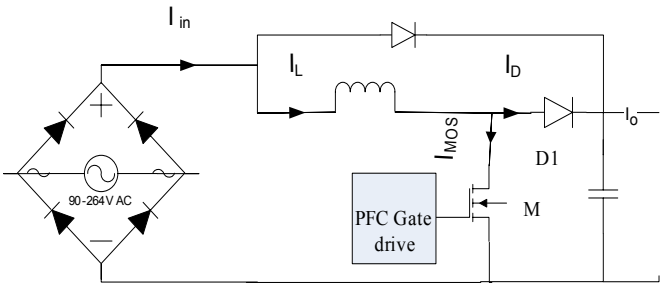


Fig. 2. Basic PFC boost converter.

II. Electronic Ballast

A. Front End PFC Boost Converter

The front-end PFC converter is basically a boost converter. Synchronous operation can be obtained at high frequencies which can reduce EMI and current ripple in the bulk capacitor [1]. For this electronic ballast design, a 250W boost power factor correction converter with input voltage of 120 V, output voltage of 400 V, and switching frequency of 100 kHz is used. For output powers greater than 300 W, the boost PFC should operate in continuous conduction mode.

Fig. 2 shows a typical PFC converter. The input is sinusoidal voltage varying from 90 V to 265 V at line frequency of 60 Hz. The input is fed into a diode bridge rectifier where the ac voltage is rectified to DC. This DC voltage is fed into the boost converter to get a higher output voltage of 385-400 V.

For the control strategy of PFC, the two important considerations are that the output voltage should be constant and the input current must follow the input voltage. For an output feedback loop to control and maintain constant output voltage while maintaining power factor of the input current, either the multiplier approach or the voltage follower approach can be used. In the multiplier approach, the input current feedback loop is programmed from the input voltage such that the DC-DC converter operates as a current sink. The multiplier approach can be divided into

a) Average current control
b) Peak current control
c) Variable hysteresis control.

These three control methods basically define the type of PFC controller that can be used for simulation. The average current control mode has been simulated using PSIM. In the average current control method, the inductor current is sensed and filtered by a current error amplifier which drives the PWM. Thus, in the inner current loop, the average input current tends to approach the reference. The converter works in CCM (continuous conduction mode) [4-12].

The gate signal generating integrated circuit of the PFC is modeled to vary the duty cycle so as to maintain constant output voltage and also maintain input power factor to be near unity. The current and the voltage are in phase by the power factor controlling gate driver circuit. The boost diode D1 and the switching MOSFET M were originally Si devices, but have been replaced with a SiC Schottky diode and SiC MOSFET respectively to examine the efficiency gains possible with these devices.

B. Resonant Inverter

The output of the PFC circuit is fed into an inverter to obtain high frequency pulses to the output. The topologies are implemented with one, two, or four switches. Most of the electronic ballasts use a half-bridge inverter.

The output of the inverter is passed through a passive filter to obtain more sinusoidal output voltage. Types of resonant filters that can be used include:

a) LC series resonant
b) LCC series resonant
c) LC parallel resonant

In this application, a parallel resonant half bridge inverter is used because of its advantages: 1) low harmonics, 2) minimum number of switches, 3) high frequency operation, 4) low acoustic noise, and 5) improved luminous efficacy [14]. A series resonant inverter is described in [13].

III. Si vs. SiC devices

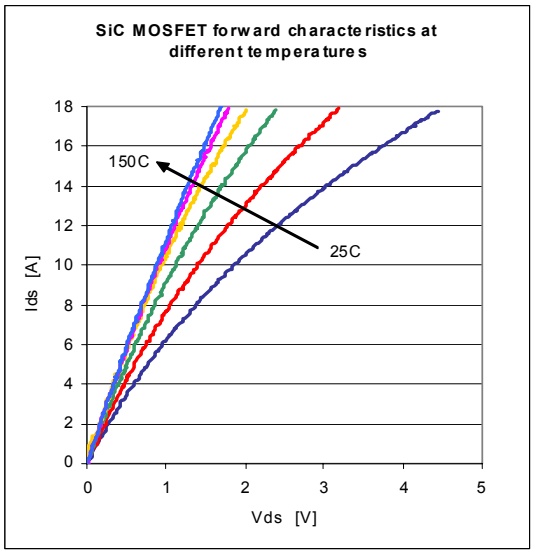
Static and switching tests required to characterize the MOSFET devices have been conducted. The I-V curves indicate the temperature variation of the on-resistance for an 800 V, 10 A SiC MOSFET from Cree as shown in Fig. 3. The resistance of the SiC MOSFET decreases with increase in temperature until near 150 °C where it begins to increase.

The I-V characteristics for a Si MOSFET rated at 600 V, 10 A indicate an increase in resistance with temperature as shown in Fig. 4. The threshold voltage decreases with temperature in both Si and SiC as shown in Fig. 5.

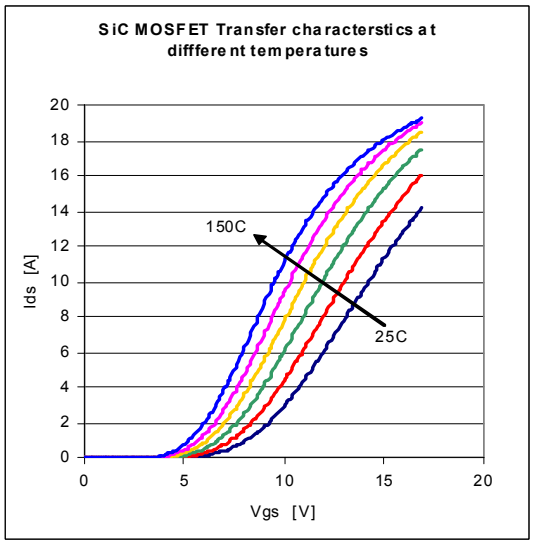
To determine switching characteristics, a double-pulse gate signal was used to drive the MOSFET, and the applied voltage was 200 Vdc. An inductive load of 8 mH was used, and the current was varied from 2 to 10 A. The temperature of the device was varied from 25 to 150 °C for the testing. The switching energy losses for the device during turn-on and turn-off as a function of temperature are plotted.

Fig. 6 shows that for the SiC MOSFET the energy losses increase with increase in current and decrease with temperature. At lower currents, the change in temperature has no significant effect on the losses; however, for higher currents the decrease in losses with temperature is more significant in turn-on losses than in turn-off losses.

The forward voltage drop across the diode is higher for the SiC diode than that for Si. The reverse recovery time is reduced in SiC; it is considered to have near-zero reverse recovery charge because it is a Schottky device and hence results in a significant reduction in recovery time compared to the Si pn diode.



(a) Forward I-V characteristics



(b) Transfer characteristics

Fig. 3. Experimentally tested characteristics of SiC MOSFET.

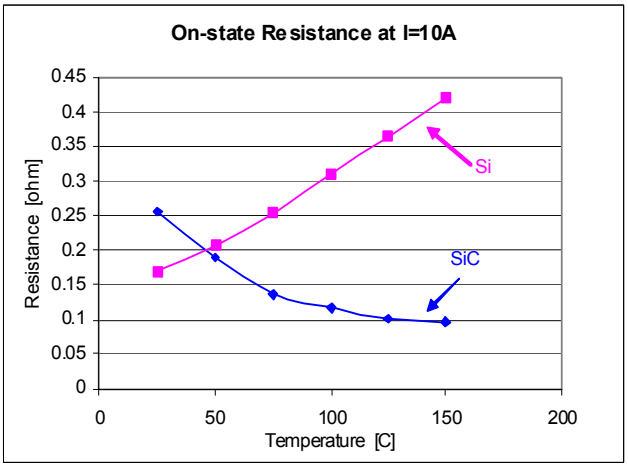


Fig. 4. Variation of on-resistance with temperature in Si and SiC MOSFETs.

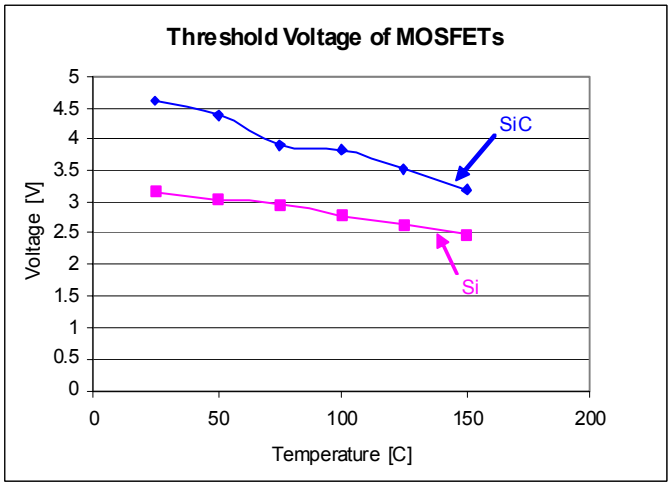
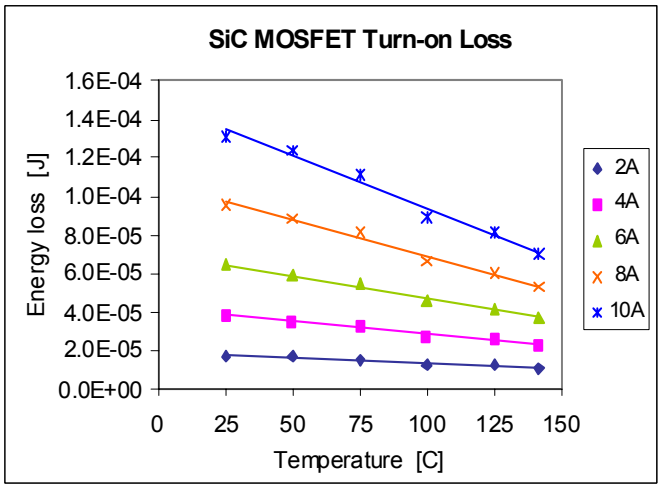
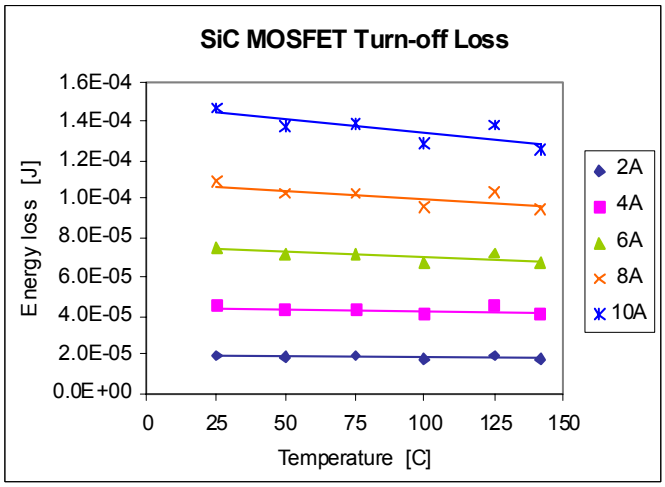


Fig. 5. Variation of threshold voltage with temperature for Si and SiC MOSFETs.



(a) Variation of turn-on losses with temperature



(b) Variation of turn-off losses with temperature

Fig. 6. Switching losses in a SiC MOSFET.

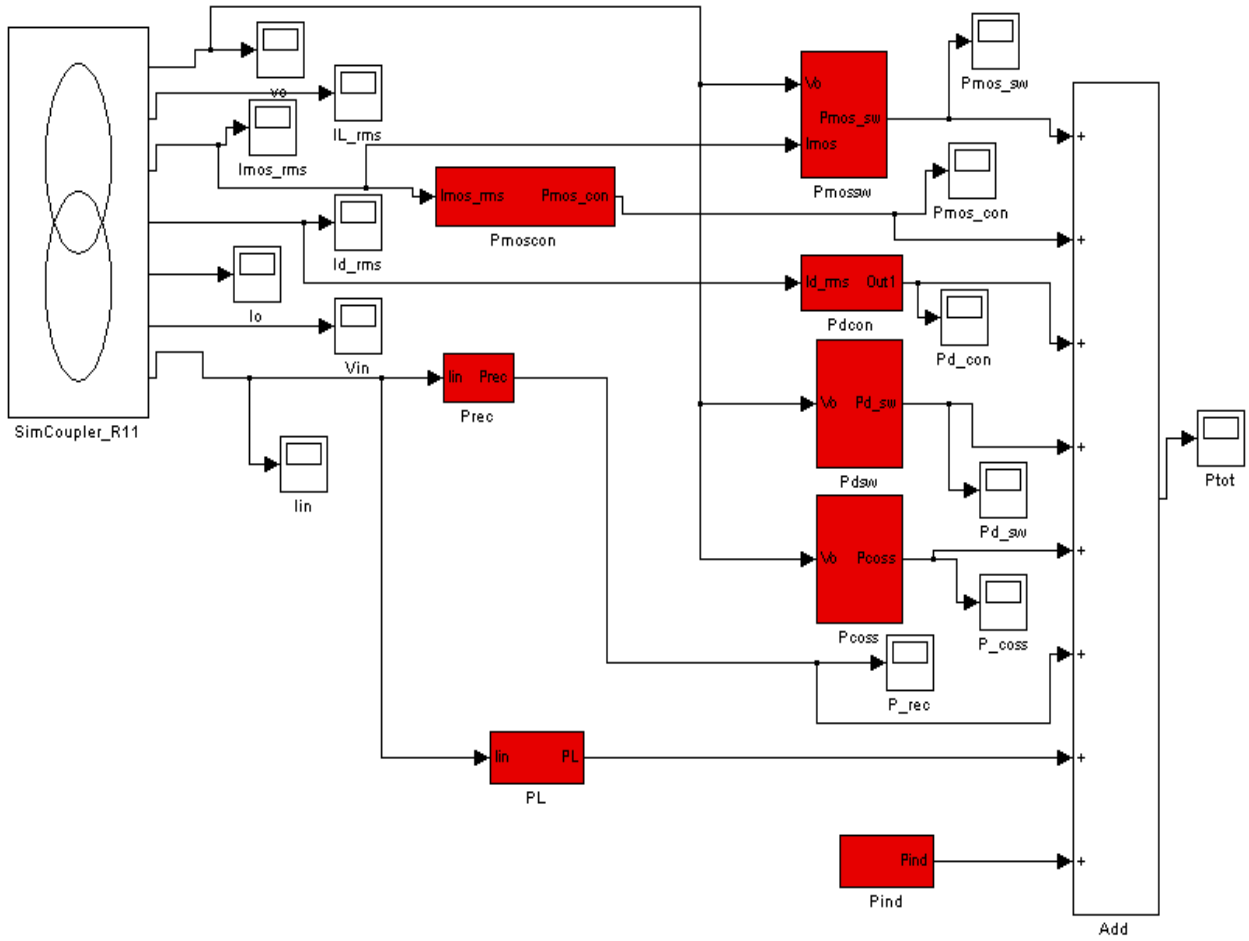


Fig. 7 Simulink model for power loss calculation using Simcoupler to couple PSIM and Simulink.

IV. Loss Modeling

Using device testing and a device physics model, a power loss model for the devices can be developed [18]. Then, an averaging technique and control strategy must be incorporated into the overall converter loss model. A thermal equivalent circuit then must be developed, and the resultant thermal values fed back into the converter loss model.

The losses in the diodes and MOSFETs are divided into conduction and switching losses. The switching losses are dependent on the switching frequency; switching losses in the MOSFET and the diode have to account for removal of the stored charge in the junction capacitances also. The conduction losses are the losses in the drift region, channel, and contacts when the device is conducting. It is dependent on the resistance and the square of the current through it. The equations for calculating these losses are given in [15].

The switching losses in the MOSFET are given by (1)

$$P_{MOS\_sw} = \left(\frac{1}{2}\times V_o \times I_{Lrms} \times 0.9 \times t_{sw} \times f\right) + \left(\frac{1}{2}\times C_{oss} \times V_o^2 \times f\right) \quad (1)$$

where V_o is the output voltage, I_{Lrms} is the rms inductor current, t_{sw} is the switching time, f is frequency of operation, C_{oss} is the output MOSFET capacitance. The first part of the switching loss is obtained by averaging the area under the transition waves of voltage and current during turn on and turn off switching times. The switching time t_{sw} is the sum of rise and fall times of the current. The second part of the switching loss in the MOSFET is due to the output capacitance C_{oss} measured between the drain and source with the gate- source voltage, V_{gs}, zero for AC voltages. C_{oss} is given by the drain to source capacitance C_{ds} in parallel with the gate to drain capacitance C_{gd}. The output capacitance decreases with voltage hyperbolically. For high voltages across the MOSFET and high switching frequency, this loss becomes significant. The output capacitance of the SiC MOSFET is 21pF and that of Si MOSFET is 48 pF at 400V.

Equation (2) gives the conduction losses in the MOSFET.

$$P_{MOS\_con} = \left(I_{MOSrms}\right)^2 \times R_{ds} \quad (2)$$

where R_{ds} is the on-resistance of MOSFET and I_{MOSrms} is the rms current through the MOSFET. The conduction loss when the MOSFET is conducting is mainly an I^2R loss due to the

on-state resistance of the MOSFET. The values of R_{ds} for Si and SiC are 0.19 and 0.25 at 25^0 C from Fig. 4. This implies there is an increase of conduction loss in SiC MOSFET at room temperature.

The conduction losses in the diode are given by (3):

$$P_{D\_con} = \left(I_{Drms}\right)^2 \times R_{on} + V_{on} \times I_{Drms}\,, \qquad (3)$$

where R_{on} is the on resistance of the diode, V_{on} is the on-state forward voltage drop of the diode, I_{Drms} is the rms current through the diode. The conduction loss in the Schottky diode is due to the on-state resistance and the diode forward voltage drop V_{on}.

The equation for calculating the switching losses in the diode is given by (4):

$$P_{D\_sw} = Q_c \times V_o \times f\,. \qquad (4)$$

V_o is the output current of the PFC converter, and Q_c is the reverse recovery charge of the diode. The switching loss in the diode is mainly due to the reverse recovery charge that has to be removed before when the diode is to be turned on. The reverse recovery charge for SiC diode is almost $1/5^{th}$ that of a Si diode which results in significant efficiency improvement with the use of SiC Schottky diode.

A Simulink model has been developed based on these equations. The values of voltage and current have been coupled from the PSIM model of the PFC converter circuit to the loss model in Simulink as shown in Fig. 7.

Efficiency calculated from preliminary simulation results and calculation of total losses in the PFC circuit with varying input voltage has shown that the use of SiC MOSFET and diode will actually result in decreased efficiency by as much as 2% at lower voltages. The efficiency of SiC MOSFET improves with higher input voltage. Note that the SiC MOSFET was rated for 800 V whereas the Si MOSFET was rated for 600 V.

The total losses include the losses due to the boost inductor, the losses in the rectifier bridge, the losses due to the boost capacitor, and the device losses in MOSFET and diode. The current and voltage values have been extracted from the simulation results of the PFC circuit in PSIM. The differences in the losses for the Si-based circuit and the SiC-based circuit are due to zero reverse recovery charge of the SiC Schottky diode and the lower output capacitance of the SiC MOSFET as compared to that of a Si MOSFET. The major increase in losses in SiC MOSFET as compared to Si MOSFET with same gate driver is attributed to increase in switching times and conduction losses of the SiC MOSFET.

V. Experimental Results

Fig. 8 shows the assembled circuit board of a 250 W HID ballast with the PFC and resonant inverter stages. The choice of components in the circuit was optimized in the design for efficiency improvement. Experimental tests were performed on the proof of concept ballast. The input voltage was varied from 90 Vac to 264 Vac and resistive load of 250 W was applied across the output of the PFC that produced 400 V. Fig. 9 shows the inductor current and drain voltage of the MOSFET waveforms obtained experimentally for 120 Vac input from the PFC circuit. The PFC boost converter in literature has at most reached an efficiency of 96% [1-3, 16, 17, 19, 20]. Fig. 10 demon-strates the power factor correction achieved using the PFC circuit. A power factor of 0.99 is achieved using the design in Fig. 8.

Fig. 8. Assembled ballast board with PFC and inverter stages connected.

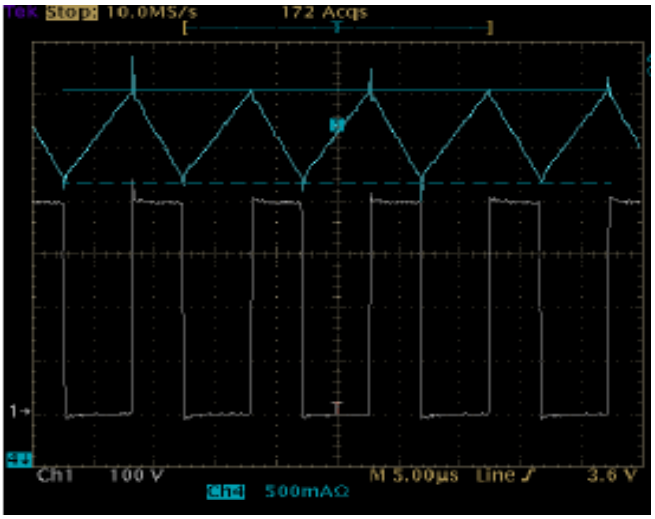


Fig. 9. Inductor current and drain-source voltage in input voltage across MOSFET.

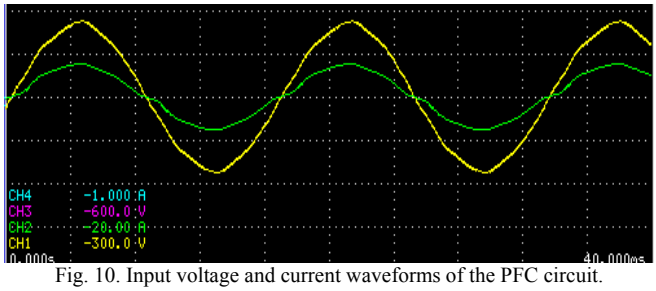


Fig. 10. Input voltage and current waveforms of the PFC circuit.

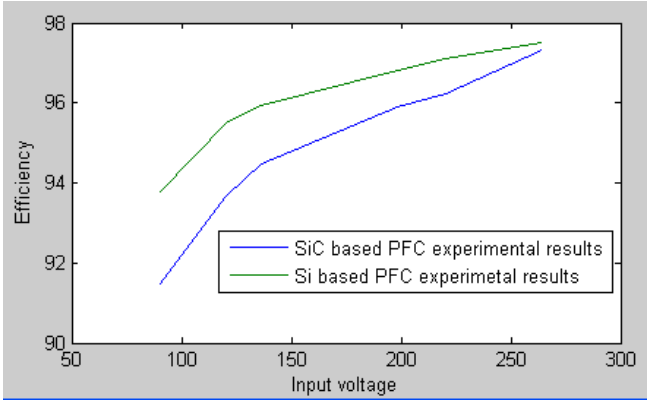


Fig. 11. Experimental values of efficiency vs. input voltage for Si and SiC based PFC.

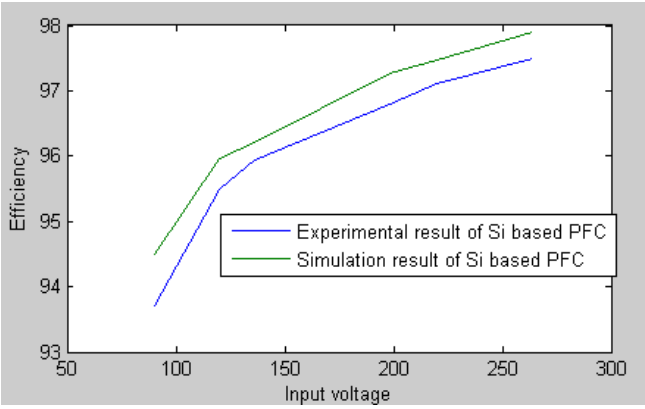


Fig. 12. Comparison of simulation and experimental results of Si-based PFC.

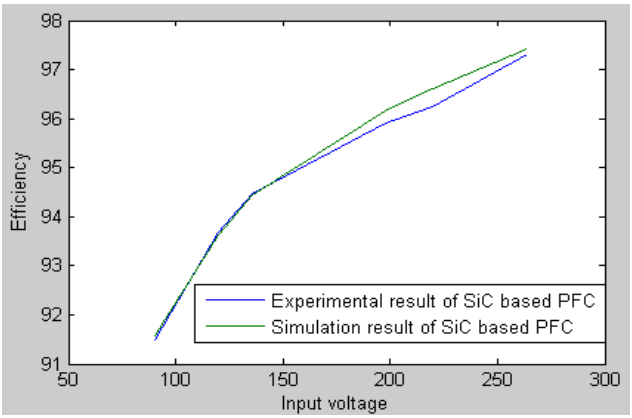


Fig. 13. Comparison of simulation and experimental results of SiC-based PFC.

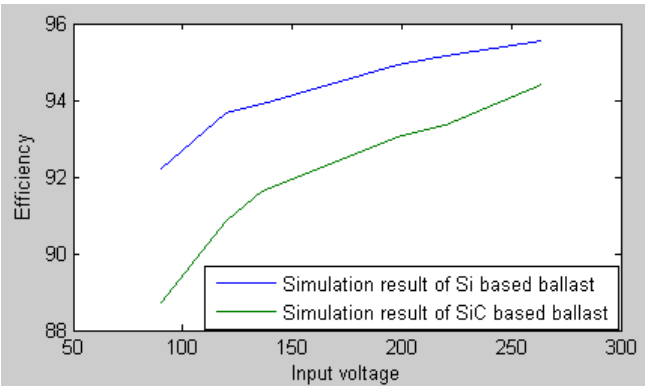


Fig. 14. Simulation result comparison of Si and SiC based ballast.

The silicon MOSFET was next replaced by the SiC MOSFET characterized in Figs. 3 and 4, and the efficiency of the converter was again measured. Fig. 11 compares experimental efficiency values of the PFC by using Si and SiC MOSFETs. We observe that the efficiencies of SiC-based PFC are lower than that of Si-based PFC.

Figs. 12 and 13 demonstrate the simulation and experimental efficiency results of a Si and SiC-based PFC, respectively. It can be observed that the simulation results are in accordance with the experimental results. The simulation model describes more closely the losses in the SiC-based PFC than the Si-based PFC.

Fig. 14 compares the simulation results of Si and SiC ballasts which includes the front-end PFC and the resonant inverter. The efficiency of just the resonant inverter portion of the circuit was greater than 97% for the Si-based inverter and for that of SiC-based inverter, the efficiency was near 97%.

The decrease in efficiency of the SiC-based ballast can be attributed to the increase in switching times of SiC MOSFET which is dependent on device design and greater drain source resistance R_{DS} of SiC MOSFET at room temperature as shown in Fig. 4. Also, it should be emphasized that the SiC MOSFETs were simply inserted as a one-to-one replacement for the Si MOSFETs. A new gate drive design with lower gate resistance is needed to take more advantage of the SiC MOSFET's intrinsic properties.

VI. Conclusions

SiC devices are expected to have better operating characteristics when compared to Si devices. However, for this application where one to one replacement of the MOSFET has been done, the efficiency of the system decreases when SiC devices are used. The switching times of the SiC MOSFET were greater than that of the Si MOSFET. A design of the gate drive circuit that would enhance faster switching is needed to exploit the SiC advantages to improve efficiency. However, the efficiency of the ballast with the Si MOSFET is close to 95% as predicted from the simulation results. The efficiency of the PFC portion of the ballast has been verified experimentally to be greater than 97%.

References

[1] M. W. Fellows, "A Study Of The High Intensity Discharge Lamp Electronic Ballast Interface," *IEEE Industry Applications Society Annual Meeting*, 12-16 Oct. 2003, pp. 1043–1048.

[2] C. Chompoo-inwai, W. Tangsrianugul, V. Pornpojratnakul, S. Banjongjit, "Development Of An Electronic Ballast For A 250 Watt High Intensity Discharge Lamp," *IEEE Industrial and Commercial Power Systems Technical Conference*, 2-6 May 2004, pp. 40–44.

[3] R. Redl, J.D. Paul, "A New High-Frequency And High-Efficiency Electronic Ballast For HID lamps: Topology, Analysis, Design, And Experimental Results," *Fourteenth Annual Applied Power Electronics Conference and Exposition,*14-18 Mar 1999, vol. 1, pp: 486-492.

[4] A. K. Jha, B. G. Fernandes, A. Kishore, "A Single Phase Single Stage AC/DC Converter With High Input Power Factor And Tight Output Voltage Regulation," *Progress in Electromagnetics Research Symposium*, March 2006, vol. 2, no. 4, pp. 322–329.

[5] A. Pandey, D. P. Kothari, A. K. Mukerjee, B. Singh, "Modelling And Simulation Of Power Factor Corrected AC-DC Converters," *International Journal of Electrical Engineering Education*, July 2004, vol. 41, no. 3, pp 244-264.

[6] M.R. Sahid, N.A. Azli, N.D. Muhammad, "A comparative study on the performances of the boost PFC circuit," *Proceedings of Power and Energy Conference, 2004*, 29-30 Nov. 2004,pp: 143- 147

[7] L. Rossetto, G. Spiazzi, P. Tenti, "Control techniques for power factor correction converters," *Proc. PEMC'94*, Sept. 1994, pp. 1310–1318.

[8] M. R. Sahid, N. A. Azli, N. D. Muhamad, "Study on the Performance of the Boost Power Factor Correction (PFC) circuit with Variable Inductor Current Sense Resistor values," *IEEE International Conference on Power Electronics and Drives,* November 17-20, 2003, pp. 1160-1109.

[9] I. Daut, R. Ali, S. Taib, "Design of a Single-Phase Rectifier with Improved Power Factor and Low THD using Boost Converter Technique," *American Journal of Applied Sciences,* vol. 3, no. 7, 2006, pp. 1902-1904.

[10] J. Sebastian, M. Jaureguizar, J. Uceda, J. "An overview of power factor correction in single-phase off-line power supply systems," *20th International Conference on Industrial Electronics, Control and Instrumentation,* 5-9 Sep 1994, vol. 3, pp. 1688-1693.

[11] M. O'Loughlin, "Advantages Using a Boost-Follower In a Power Factor Corrected (PFC) Pre-Regulator," Texas Instruments, Inc., www.ti.com.

[12] F. Yan, "PFC Electronic Ballast For Xenon Short Arc Lamps," *Proceedings of the IEEE International Conference on Power Electronics and Drive Systems, 1999.* vol. 1, pp: 501-505.

[13] M. H. Ohsato, S. Inarida, G. Kimura, M. Shioya, T. Kawaguchi, "New Type Of Ballast For HID Lamps Using Series Resonant Circuit," *Proceedings of the 1992 International Conference on Industrial Electronics, Control, Instrumentation, and Automation, 1992. 'Power Electronics and Motion Control'.,*9-13 Nov 1992 vol.1, pp: 191-195.

[14] C. H. Lee, G. B. Joung, G. H. Cho, "A Unity Power Factor High Frequency Parallel Resonant Electronic Ballast," *Industry Applications Society Annual Meeting,* 7-12 Oct 1990, vol. 2, pp. 1149-1156.

[15] P. O. Jeannin, D. Frey, J.-C. Podvin, J.-P. Ferrieux, J. B. Rivet, "1 MHz Power Factor Correction Boost Converter with SiC Schottky Diode," *IEEE Industry Applications Society Annual Meeting,* October 3-7, 2004, pp. 1267-1272.

[16] "Selection Guide of SiC Schottky Diode in CCM PFC Applications," August 2006, www.cree.com/power.

[17] S. Hodge Jr., "SiC Schottky Diodes in Power Factor Correction," *Power Electronics Technology,* August 2004, pp. 14-18.

[18] H. Zhang, L. M. Tolbert, B. Ozpineci, M. S. Chinthavali, "Power Losses and Thermal Modeling of a 4H-SiC VJFET Inverter," *IEEE Industry Applications Society Annual Meeting*, October 2-6, 2005, Hong Kong, China, pp. 2630-2634.

[19] J. Cardesín, J. García, J. Ribas, J. M. Alonso, A. J. Calleja, E. L. Corominas, M. Rico-Secades, M. Dalla, "Low-Cost PFC Electronic Ballast for 250W HID Lamps Operating as Constant Power Source with 400 kHz Switching Frequency," *IEEE 36th Power Electronics Specialists Conference,* 2005, pp. 1130-1135.

[20] Y. Takahashi, M. Kamatra, K. Shimizu, "Efficiency improvement of electronic ballast," *IEEE 32nd Industry Applications Conference,* 5-9 Oct. 1997, vol. 3, pp. 2284-2290.