MODEL SIMULATION AND VERIFICATION OF A VERTICAL DOUBLE IMPLANTED (DIMOS) TRANSISTOR IN 4H-SIC

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Abstract

Silicon-based switching devices have reached the theoretical limitations for high power and high temperature applications whereas silicon carbide (SiC) has emerged as an alternate material system to overcome the limitations and can be used in extreme environment. In this paper, a vertical DIMOS transistor structure, a switching device in 4H-SiC material system, is presented. The model takes into account various short channel effects in the DIMOS channel region as well as velocity saturation and exact device geometry in the drift region. Simulations for exact device geometry have been conducted using ATLAS device simulator. A good agreement between the ATLAS simulation and analytical model evaluation for vertical DIMOS is demonstrated. Device structure and model parameters can be adjusted to obtain an optimum device to be used in system level applications.

Key Words

SiC, vertical DIMOS, power device, model verification.

I. Introduction

In recent years, silicon carbide (SiC) has received increased attention because of its potential for a wide variety of high power applications [1-4]. SiC has the properties of high electric breakdown field ($3.5x10^6$ V/cm), high electron saturated drift velocity ($2x10^7$ cm/sec), high melting point (2830 ^oC), and high thermal conductivity (4.9 W/cm-°K), which give this material great potential in high power device applications. A summary of SiC material parameters is shown in Table I. Due to the high breakdown field of SiC, the drift region can be made eight to ten times thinner than those of silicon high voltage devices. Thus the SiC devices can be made smaller and more compact requiring smaller cooling system. The features of SiC make it an attractive material for high power and high temperature applications and lead to significant savings in cost and space in packaging and cooling systems for many aircraft, shipboard, and hybrid vehicle applications.

TABLE I
COMPARISON OF SI AND SIC MATERIAL PROPERTIES [4]

Properties	Si	6H-SiC	4H-SiC
***Band gap** (eV)*	1.11	2.9	3.2
Dielectric constant	11.8	9.7	9.7
***Breakdown field** (V/cm)*	$6x10^5$	$35x10^5$	$35x10^5$
***Saturated velocity** (cm/sec)*	$1x10^7$	$2x10^7$	$2x10^7$
***Electron mobility (in bulk)** (cm^2/V-sec)*	1350	380	800
Hole mobility (in bulk) (cm^2/V-sec)	450	95	120
***Thermal conductivity** (W/cm-^oK)*	1.5	4.9	4.9
***Melting point** (^oC)*	1420	2830	2830

SiC has more than one hundred poly-types [3]. Among those, 4H-SiC is preferred over 6H-SiC because the electron mobility in 4H is approximately twice that of 6H in the direction perpendicular to *c*-axis and almost ten times in the direction parallel to *c*-axis. Thus, 4H-SiC is suitable for vertical device structure.

The dc-dc converters and the ac drives are extensively used in power electronics, power systems, traction drives, and hybrid electric vehicle (HEV) applications, where diodes and MOSFETs are used as switching devices. The switching devices have to carry huge current at the 'on' state and have to sustain large blocking voltage at the 'off' state. The performance of the Si-based switches is approaching the theoretical limits in high power applications due to its intrinsic material properties. SiC is an alternate material system that can be used to overcome the limitations of the Si-based switching devices and can be used in extreme environment.

The first Schottky diode in SiC was marketed by Cree Research Inc. High-voltage (1.75kV) Schottky diodes with a low on resistance (5 $m\Omega$-cm^2) were reported with Ti/4H-SiC [5]. The highest value of blocking voltage is 6.2kV for 100 Acm^{-2} using 4H-SiC p-n junction of mesa

structure [6]. Although there is no commercially available power MOSFETs in SiC material system, Cree has demonstrated various switching devices in SiC [7]. A group from Purdue University proposed a DIMOS in 6H-SiC with a breakdown voltage of 760V [8].

This paper presents a vertical MOS transistor structure in 4H-SiC material system for power electronic applications. Preliminary results for both the analytical and numerical simulations presented in this paper demonstrate the feasibilities of developing a power MOSFET with high voltage and current rating.

II. Processing and Applications

An application specific optimum SiC power MOSFETs is being developed for hybrid electric vehicles applications [9]. The system level benefits of SiC power electronics on hybrid electric vehicle (HEV) applications was also studied [10]. Considering the SiC material processing limitations and feedback from the system level application group, an application specific SiC power MOSFET structure has been proposed.

Good ohmic contact is essential for the Schottky diode formation. As a part of the research, Schottky diodes were formed using a metal contact with dopped SiC samples.

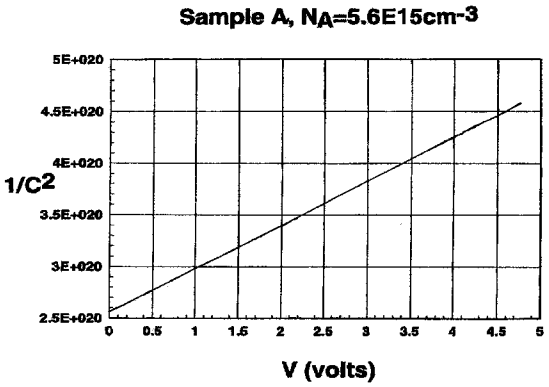

Figure 1: C-V plot of sample A

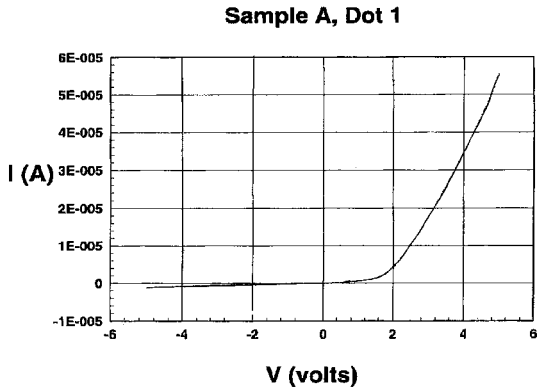

Figure 2: I-V Characteristic of sample A

The doping densities as well as the current voltage characteristics were measured for four test samples. C-V plot and I-V characteristics for sample-A are shown in Figure 1 and Figure 2, respectively. All p-type contacts are Al-Ni and n-type contacts are Au-As-Ni alloy. Based on the results obtained from the C-V and I-V plots, Au-As-Ni alloy makes a very good contact for n-SiC. Extensive literature search shows that Au-As-Ni contacts are novel approach for SiC device applications. The measured values of the doping densities are: sample-A: $5.6e15cm^{-3}$, sample-B: $1.02e16cm^{-3}$, sample-C: $8.6e17cm^{-3}$ and sample-D: $1.3e18cm^{-3}$.

An increase in efficiency and reduction of mass and volume in heat sink for dc-dc power supply and traction drive with SiC have been reported by this group [9]. The simulation results showed an increase in the converter efficiency and a decrease in the heat sink mass and volume. About 5-10% increase in efficiency was obtained for the traction drive. It was observed that at 20kHz operating frequency, conduction losses dominate over the switching losses where at 100kHz switching losses dominate over conduction losses. For either frequency operation the SiC inverter requires a smaller heat sink. For the traction drive, the all-SiC inverter requires heat sink one-third the size required by the all-Si inverter.

III. Device Structure

A vertical double Implanted MOS transistor in 4H-SiC has been considered to verify the model in SiC material system. The cross sectional view of a DIMOS is shown in Figure 3. Since the diffusion process in SiC is ineffective, ion implantation is the only way to form *p*-body and *n*+ region for the vertical structure and double diffusion is not suitable for SiC device fabrications. The *n*- drift region is usually doped lightly ($5x10^{14}cm^{-3}$ for this

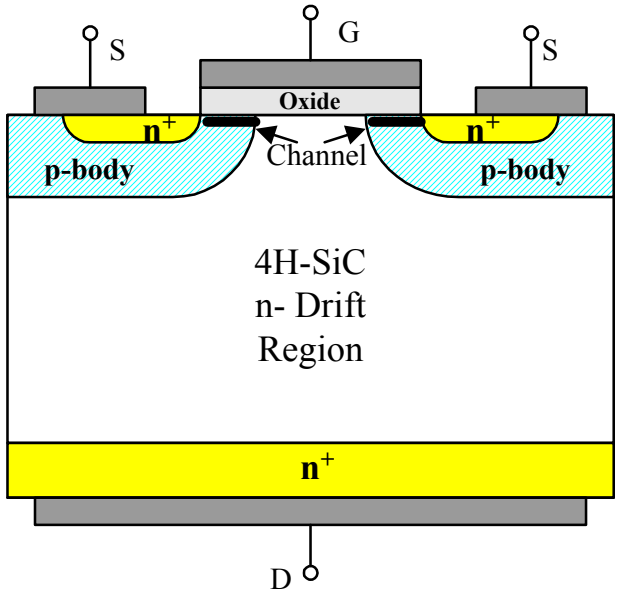

Figure 3: Schematic Cross section of Vertical DIMOS.

device) to reduce the losses in the drift region. The *n*+ regions were doped with ($1.5x10^{20}cm^{-3}$) Nitrogen; *p*-body regions were formed with ($4x10^{17}cm^{-3}$) Boron implantations. The channel length and width were 10µm and 200µm, respectively. The oxide thickness was 500Å and drift region thickness was 40µm. The *p*-bodies were separated by 18µm.

IV. Model

The Double Implanted Metal-oxide Semi-conductor (DIMOS) field effect transistor has been frequently used in high voltage power electronics applications [11-12]. The performance of a DIMOS device is limited by the quasi-saturation behavior [13] in its characteristics. It is shown that such effect is due to carrier velocity saturation because of the high electric field, low impurity concentration in drift layer, and narrow *p*-body spacing [14]. Figure 4 shows the details of device structure identifying different regions of operation. Here, W_t is the total vertical height, W_j is the height of the *p*-body, W_d is the width of the depletion region, L is the channel length formed under the gate and inside the *p*-body, L_{diff} is the separation of the p-bodies, L_p is the length of *p*-body, α is the angle of slope of the drift region narrowing.

A detailed study has been made on the vertical DIMOS, and an analytical model has been developed [15]. The model was developed from regional analyses of carrier transport in the channel and drift regions. The channel is defined by the compensation between the *p*-body and *n*-source lateral diffusion. The current voltage characteristic in the triode region is given by,

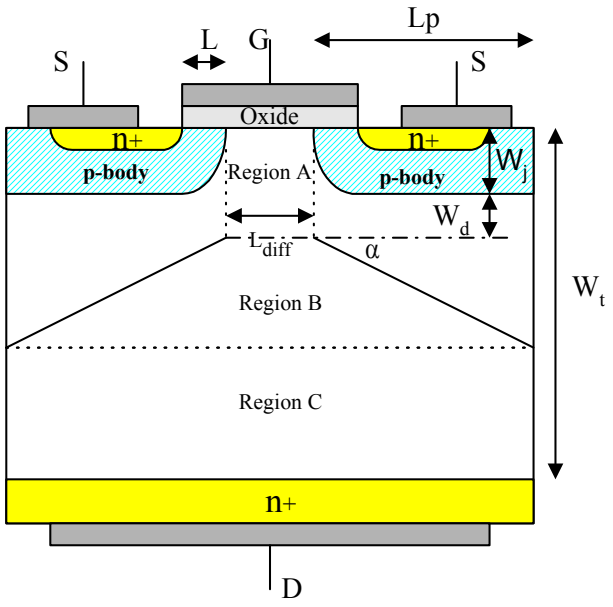

Figure 4: DIMOS structure for Modeling.

$$I_{ch} = \frac{W\mu_{neff}}{2L\left[1+(\mu_{neff}/2v_{sat}L)V_{ch}\right]}V_{ch}\left[2C_{ox}(V_{GS}-V_T)-(C_{ox}+C_{do})V_{ch}\right] \quad (1)$$

The drift region has been divided into three parts: an accumulation region A, a drift region B with a varying cross section area, and drift region C with constant cross section. Voltage for these regions are given by,

$$V_A = \int_0^{W_j+W_d} E_y dy = \frac{I_D(W_j+W_d)}{W(L_{diff}qN_d\mu_{neff}) - I_D/E_C} \quad (2)$$

$$V_B = \frac{I_D}{WqN_d\mu_{neff}\cot\alpha}\log\left[\frac{WqN_d\mu_{neff}(L_{diff}+L_P)-I_D/E_C}{WqN_dL_{diff}\mu_{neff}-I_D/E_C}\right] \quad (3)$$

$$V_C = \frac{I_D(W_t-W_j-W_d-L_P\tan\alpha)}{W(L_{diff}+L_P)qN_d\mu_{neff} - I_D/E_C} \quad (4)$$

Total drift region voltage $V_{drift} = V_A + V_B + V_C$ and voltage across the drain to source $V_{DS} = V_{drift} + V_{ch}$. For a given current I_D, which equals to I_{ch} of the channel region, must be solved by an iterative method due to the implicit nature of the voltages and currents. The current/voltage characteristics of the analytical model have been evaluated (Figure 5) using 4H-SiC material parameters.

V. Model Verification

The model is further realized in a two-dimensional device simulator (ATLAS). A practical device structure for vertical DIMOS for 4H-SiC material systems has been simulated. The simulated results, with a device width of 200µm, of the output characteristics are shown in Figure 6.

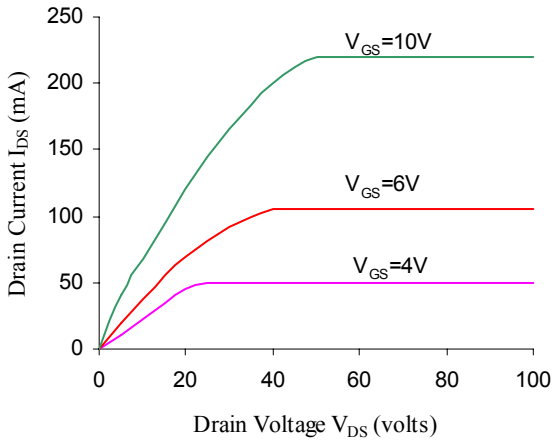

Figure 5: Output characteristics using the model.

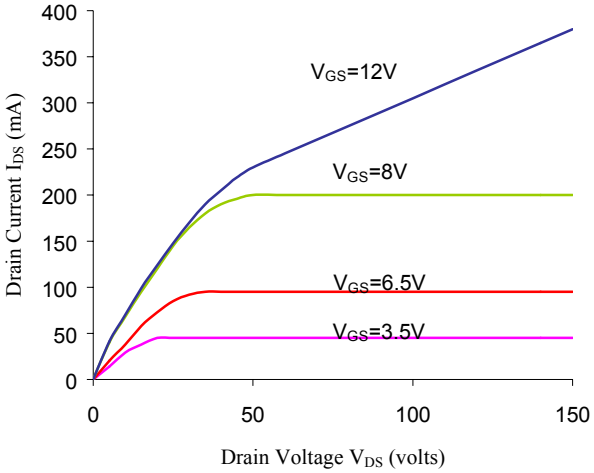

Figure 6: Current-Voltage characteristic obtained from device simulator (ATLAS)

VI. Results and Discussions

The output currents of the vertical MOSFET obtained from the analytical model remains in the saturation region for the device parameters' values used in computations. A clear quasi-saturation effect has been observed for numerical simulations. As long as the drain currents enter into the saturation region before the velocity saturation occurs, the gate voltage has control over the drain currents. However, the gate loses its control over the drain currents if velocity saturation of the carrier occurs before the drain current. It has also been observed that quasi-saturation effect occurs at higher gate voltage for larger *p*-body separations and higher drift layer doping densities. From the analytical model, a drain current of 220 mA is obtained for a gate voltage of 10 V, whereas a device simulator obtained a drain current of 200 mA for a gate voltage of 8 V. So, there is a good agreement between the results of the model and simulated device structure.

VII. Conclusions

SiC is an attractive material for high power and high temperature applications. A novel approach for ohmic contact to SiC has been demonstrated. An analytical model for DIMOS has been verified for 4H-SiC material system. Quasi-saturation effect in DIMOS is also observed. The quasi-saturation effects imposed on the *p*-body spacing and drift region doping help to achieve a device structure for the desired current level and breakdown voltage.

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References

[1] M. Bhatnagar and B.J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for Power Devices," *IEEE Trans. on Electron Devices*, 40(3), pp. 645-655, March 1993.

[2] K. Shenai, R.S. Scott and B.J. Baliga, "Optimum Semiconductors for High Power Electronics," *IEEE Trans. on Electron Devices*, 36(9), pp. 1811-1823, September. 1989.

[3] H. Morkoc, S. Strite, G.B. Gao, M.E. Lin, B. Sverdlov, and M. Burns, "Large-band-gap SiC, III-V Nitride, and II-V ZnSe-based Semiconductor Device Technologies," *Journal of Applied Physics*, 76 (3), pp. 1363-1397, 1 August 1994.

[4] C. Weitzel, J. palmour, C. Carter, K. Moore, K. Nordquist, S. Allen, C. Thero, and Bhatnagar, "Silicon Carbide High-Power Devices", *IEEE Trans. on Electron Devices*, 43(10), pp. 1732-1741, October 1996.

[5] A. Itoh, T. Kimoto, and H. Matsunami, "Excellent Reverse Blocking Characteristics of High-Voltage 4H-SiC Schottky Rectifiers with Boron-Implanted Edge Termination," *IEEE Electron Devices Letters*, no. 17, pp. 139-141, 1996.

[6] Y. Sugawara, K.Asano, R. Singh, and J.W. Palmour, "6.2 kV 4H-SiC pin Diode with low Forward Voltage Drop", *Material Science Forum*, vols 338-342, pp. 1371-1374, 2000.

[7] D.B. Slater, "Development of a high temperature SiC CMOS Technology", SBIR abstract, Cree Research, Inc. Durham, NC, 1997.

[8] J.N. Shenoy, J.A.Cooper, and M.R. Melloch, "High-Voltage Double-Implanted Power MOSFET's in 6H-SiC," *IEEE Electron Devices Letters*, vol. 18, no. 3, pp. 93-95, 1997.

[9] M. Hasanuzzaman and Syed K. Islam, "Analytical Modeling of Vertical Double-Implanted Power MOSFET (DIMOS) in 4H-SiC," *Proceedings of Conneticut Symposium on Microelectronics & Optoelectronics,* Connecticut, March 2002.

[10] Burak Ozpineci, Leon M. Tolbert, Syed K. Islam, Tim J. Theiss, "A Parametric Device Study for SiC Diodes in Vehicular Applications," *Proceedings of IEEE Vehicular Technology Conference (VTC02)*, Vancouver, Canada, September 24-29, 2002, pp. 1495-1499.

[11] B.J. Baliga, "Trends in Power Semiconductor Devices," *IEEE Trans. On Electron Devices*, 43(10), pp. 1717-1731, October 1996.

[12] D.A. Grant and J. Gower, *Power MOSFETs: Theory and Application,* John Wiley & Sons, New York 1989, pp. 377-382.

[13] Krishna Shenai, "Effect of P-Base Sheet and Contact Resistances on Static Current-Voltage Characteristics of Scaled Low-Voltage Vertical Power DMOSET's," *IEEE Electron Devices Letters*, no. 6, pp. 270-272, 1991.

[14] M. Darwish, "Study of the Quasi-Saturation Effect in VDMOS Transistors," *IEEE Trans. on Electron Devices*, vol. ED-33, no.11, pp. 1710-1716, 1986.

[15] M. Andersson and P. Kuivalainen, "Physical Modelling of Vertical DMOS Power Transistors for Circuit Simulation," *Physica Scripta*. Vol. T54, pp. 157-158, 1994.