Cascaded H-bridge Multilevel Inverter Drives Operating under Faulty Condition with AI-Based Fault Diagnosis and Reconfiguration

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***Abstract*-The ability of cascaded H-bridge multilevel inverter drives (MLID) to operate under faulty condition including AI-based fault diagnosis and reconfiguration system is proposed in this paper. Output phase voltages of a MLID can be used as valuable information to diagnose faults and their locations. It is difficult to diagnose a MLID system using a mathematical model because MLID systems consist of many switching devices and their system complexity has a nonlinear factor. Therefore, a neural network (NN) classification is applied to the fault diagnosis of a MLID system. Multilayer perceptron (MLP) networks are used to identify the type and location of occurring faults. The principal component analysis (PCA) is utilized in the feature extraction process to reduce the NN input size. A lower dimensional input space will also usually reduce the time necessary to train a NN, and the reduced noise may improve the mapping performance. The genetic algorithm (GA) is also applied to select the valuable principal components to train the NN.**

A reconfiguration technique is also proposed. The proposed system is validated with simulation and experimental results. The proposed fault diagnostic system requires about 6 cycles (~100 *ms* at 60 Hz) to clear an open circuit and about 9 cycles (~150 ms at 60 Hz) to clear a short circuit fault. The experiment and simulation results are in good agreement with each other, and the results show that the proposed system performs satisfactorily to detect the fault type, fault location, and reconfiguration.

***Index Terms*—Fault diagnosis, fault tolerance, genetic algorithm, multilevel inverter, neural network, power electronics**.

I. INTRODUCTION

Industry has begun to demand higher power ratings, and multilevel inverter drives have become a solution for high power applications in recent years. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Two topologies of multilevel inverters for electric drive application have been discussed in [1]. The cascaded MLID is a general fit for large automotive all-electric drives because of the high VA rating possible and because it uses several dc voltage sources which would be available from batteries or fuel cells [1].

A possible structure of a three-phase cascaded multilevel inverter drive for an electric vehicle is illustrated in Fig. 1. The series of H-bridges makes for modularized layout and packaging; as a result, this will enable the manufacturing process to be done more quickly and cheaply. Also, the

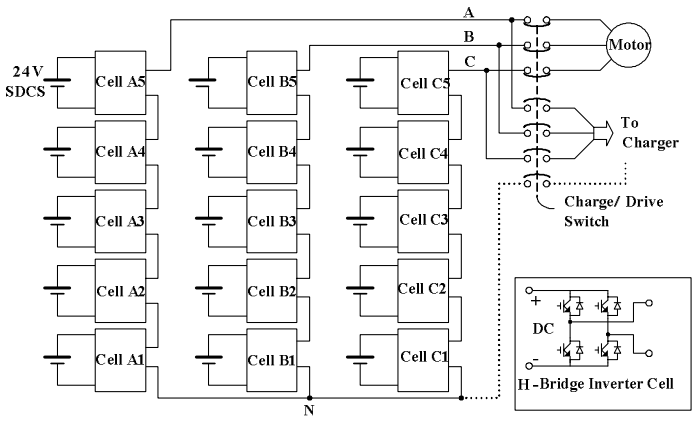


Fig. 1. Three-phase wye-connection structure for electric vehicle motor drive.

reliability analysis reported in [2] indicates that the fault-tolerance of cascaded MLID has the best life cycle cost. However, if a fault (open or short circuit) occurs at a semiconductor power switch in a cell, it will cause an unbalanced output voltage and current, while the traction motor is operating. The unbalanced voltage and current may result in vital damage to the traction motor if the traction motor is run in this state for a long time.

Generally, the passive protection devices will disconnect the power sources or gate drive signals from the multilevel inverter system whenever a fault occurs, stopping the operated process. Although a cascaded MLID has the ability to tolerate a fault for some cycles, it would be better if we can detect the fault and its location; then, switching patterns and the modulation index of other active cells of the MLID can be adjusted to maintain the operation under balanced load condition. Of course, the MLID can not be operated at full rated power. The amount of reduction in capacity that can be tolerated depends upon the application; however, in most cases a reduction in capacity is more preferable than a complete shutdown.

A study on fault diagnosis in drives begins with a conventional PWM voltage source inverter (VSI) system [3-5]. Then, artificial intelligent (AI) techniques such as fuzzy-logic (FL) and neural network (NN) have been applied in condition monitoring and diagnosis [6-8]. Furthermore, a new topology with fault-tolerant ability that improves the reliability of multilevel converters is proposed in [9]. A method for

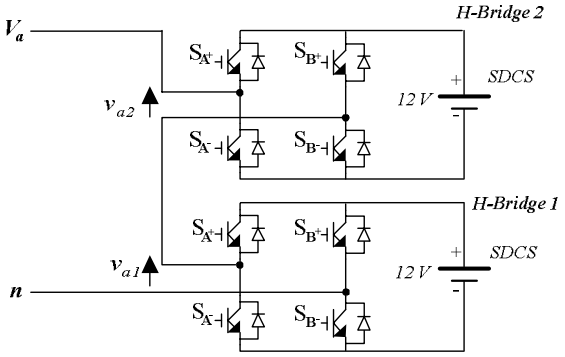
operating cascaded multilevel inverters when one or more power H-bridge cells are damaged has been proposed in [2, 10]. The method is based on the use of additional magnetic contactors in each power H-bridge cell to bypass the faulty cell.

One can see from the concise literature survey that the knowledge and information of fault behaviors in the system is important to improve system design, protection, and fault tolerant control. Thus far, limited research has focused on MLID fault diagnosis and reconfiguration. Therefore, a MLID diagnostic system is proposed in this paper that only requires measurement of the MLID's voltage waveforms and does not require measurement of currents.

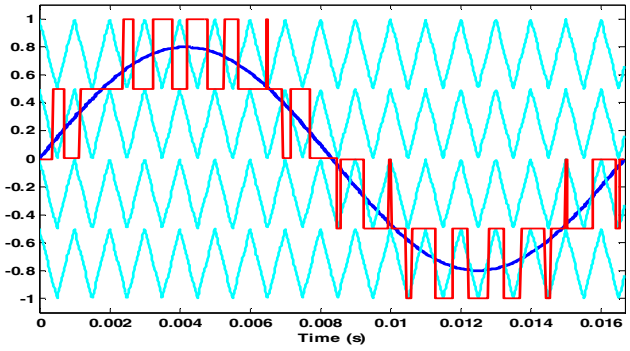
II. Diagnostic Signals

Before continuing discussion, it should be emphasized that the multilevel carrier-based sinusoidal PWM is used for controlling gate drive signals for the cascaded MLID. Fig. 2 shows that the output voltages can be controlled by controlling the modulation index (m_a). To expediently understand, the two separate dc sources (SDCS) cascaded MLID structure is used as an example in this section.

The selection of diagnostic signals is very important because the neural network could learn from unrelated data to classify faults which would result in improper classification. Simulation results (using power simulation (PSIM) from Powersim Inc.) of input motor current waveforms during an open circuit fault at different locations of the MLID (shown in Fig. 2 (a)) are illustrated in Fig. 3 and Fig. 4. As can be seen in Fig. 3 and Fig. 4, the input motor currents can classify open circuit faults at the same power cell by tracking current polarity (see Fig. 4); however, it is difficult to classify the faults at different power cells; the current waveform for a fault of S_{A+} in H-bridge 2 (Fig. 3) looks identical to that for a fault of S_{A+} in H-bridge 1 (Fig. 4 (a)). As a result, the detection of fault locations could not be achieved with only using input motor current signals. Also, the current signal is load dependent: the load variation may lead to misclassification; for instance, light load operation as reported in [11].



(a)



(b)

Fig. 2. (a) Single-phase multilevel-inverter system; (b) Multilevel carrier-based sinusoidal PWM showing carrier bands, modulation waveform, and inverter output waveform (m_a = 0.8/1.0).

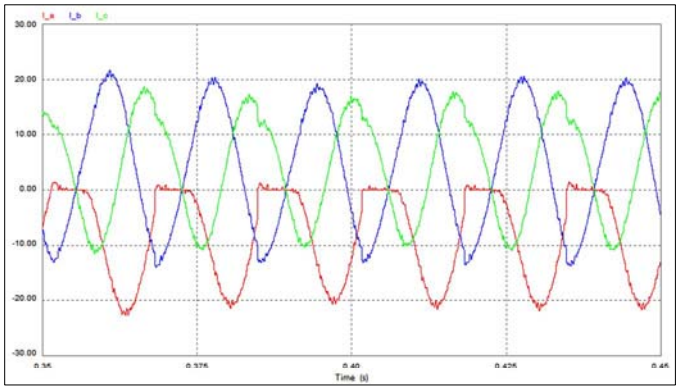
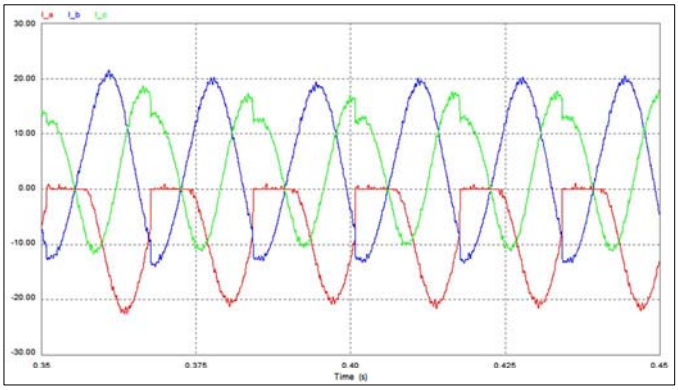
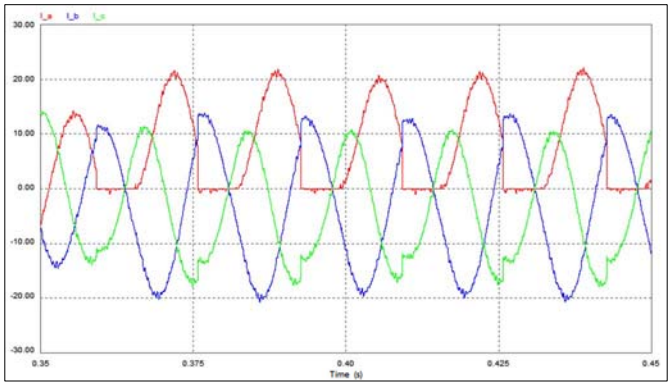


Fig. 3. Input motor currents during open circuit fault at switch S_{A+} of H-bridge 2.



(a)

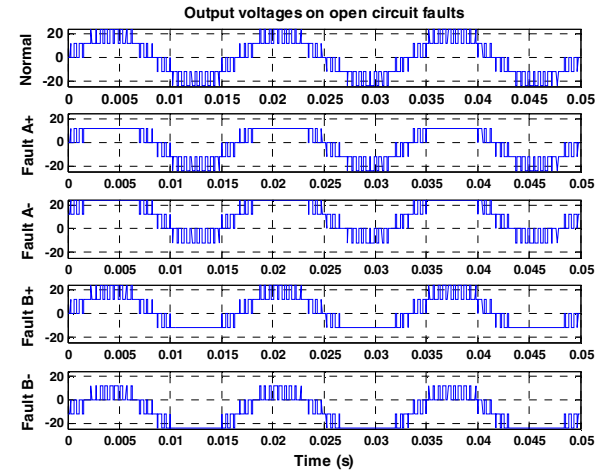


(b)

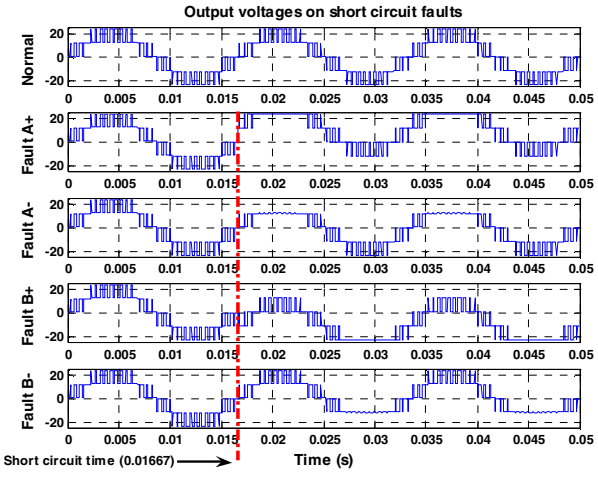
Fig. 4. Input motor currents during open circuit fault at H-bridge 1: (a) switch S_{A+}, (b) switch S_{B+}.

Auspiciously, Fig. 2 indicates that an output phase PWM voltage is related to turn-on and turn-off time of associated switches; hence, a faulty switch can not generate a desired output voltage. The output voltage for a particular switch is zero if the switch has a short circuit fault, whereas the output voltage is about V_{dc} of SDCS if the switch has an open circuit fault. For this reason, the output phase voltage can convey valuable information to diagnose the faults and their locations. The simulation results of output voltages are shown for an MLID with open circuit faults and short circuit faults in Fig. 5. One can see that all fault features in both open circuit and short circuit cases could be visually distinguished.

Also, experimental results of output voltage signals of open circuit faults in each location of two SDCS MLID (Fig. 2) with multilevel carrier-based sinusoidal PWM gate drive signals are shown in Fig. 6 (H-bridge 1) and Fig. 7 (H-bridge 2). Output voltage signals are obviously related to the fault locations. Also, the output voltages of a MLID can also be used to diagnose the fault types (open and short circuit); therefore, we will attempt to diagnose the fault types and fault locations in a cascaded MLID from its output voltage waveform.

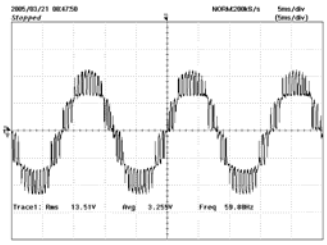


(a)

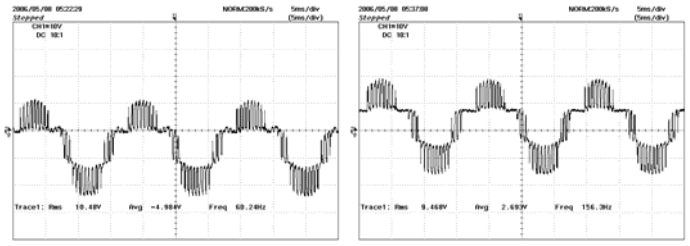


(b)

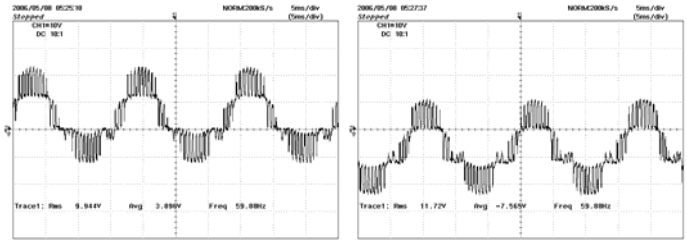
Fig. 5. Simulation of output voltages signals (a) open circuit faults, (b) short circuit faults showing fault features at S_{A+}, S_{A-}, S_{B+}, and S_{B-} of H-bridge 2 with modulation index = 0.8 out of 1.0.



(a)

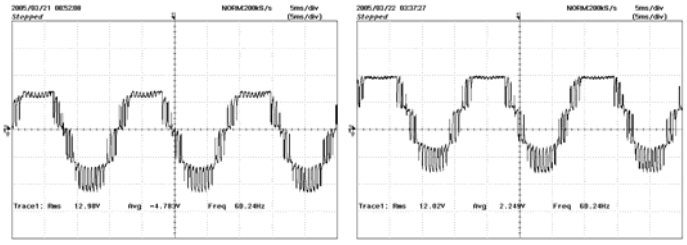


(b) (c)

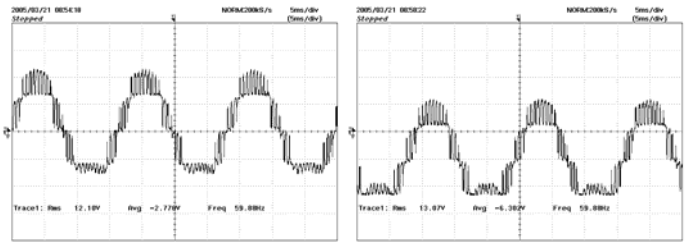


(d) (e)

Fig. 6. Experiment of fault features at (a) normal, (b) S_{A+} fault, (c) S_{A-} fault, (d) S_{B+} fault, and (e) S_{B-} fault of H-bridge 1 with modulation index = 0.8 out of 1.0.



(a) (b)



(c) (d)

Fig. 7. Experiment of fault features at (a) S_{A+} fault, (b) S_{A-} fault, (c) S_{B+} fault, and (d) S_{B-} fault of H-bridge 2 with modulation index = 0.8 out of 1.0.

III. Fault Diagnostic Methodology

It is possible that artificial intelligent (AI) based techniques can be applied in condition monitoring and diagnosis. AI-based condition monitoring and diagnosis have several advantages. For instance, AI-based techniques do not require any mathematical models; therefore, the engineering time and development time could be significantly reduced [12]. The methodology of fault diagnostic system using AI has been reported in [13-15] and will not be repeated here. The discussion of AI presented in this section will be brief, providing only the indispensable notion to elucidate the fundamental AI-based approach applied to a fault diagnosis system in a MLID.

First, the feature extraction of the output voltage signals is performed by using FFT; then, the principal component analysis (PCA) is used in the feature extraction process. PCA offers a lower dimensional input space which will also usually reduce the time necessary to train a neural network, and the reduced noise (by keeping only valuable principal components (PCs)) may improve the mapping performance [14]. Next, genetic algorithm (GA) is applied to search for the best combination of PCs to train the neural network as explained in [15]. The output of GA is the best combination of PCs which provide the weight and bias matrix of neural networks used for classification task. After that, the weight and bias matrix of the neural networks will be implemented in Simulink interfacing with FFT and PCA subsystem as shown in Fig. 8. It should be mentioned that PCA and GA process will perform off-line to achieve the best combination of PCs.

Before continuing discussion, it should be mentioned that the methodology of fault diagnosis presented in [14-15] can be applied to any other cascaded H-bridges MLID. However, some minor processes are different such as neural network structure, input/output data set, and principal component (PC) selection. Since the simulation and experiment validation will be performed with 11-level MLID, the fault diagnostic processes for the 11-level MLID are explained in the following.

A. Neural Network Structure

The fault diagnostic diagram for an 11-level MLID with 5 SDCS is depicted in Fig. 8. The neural network classification process consists of two networks: open circuit network and short circuit network. The training time and required memory for implementation are reduced with the segregated neural network as reported in [16, 17]. Moreover, in this particular case, the short circuit data set includes the loss of separate dc source (SDCS) condition due to the fuse protection because the fuse may blow before the fault is detected; therefore, the short circuit neural network may contain more complexity than the open circuit neural network. Also, the neural networks may be assigned to have the ability to provide "do not know" conditions. The multilayer feedforward perceptron (MLP) networks are used in both open circuit and short circuit neural networks. The neural network architecture is based upon GA selection as discussed in [15]. The input neurons depend on GA selection; however, the one hidden layer with 4 hidden nodes and 6 output nodes are assigned.

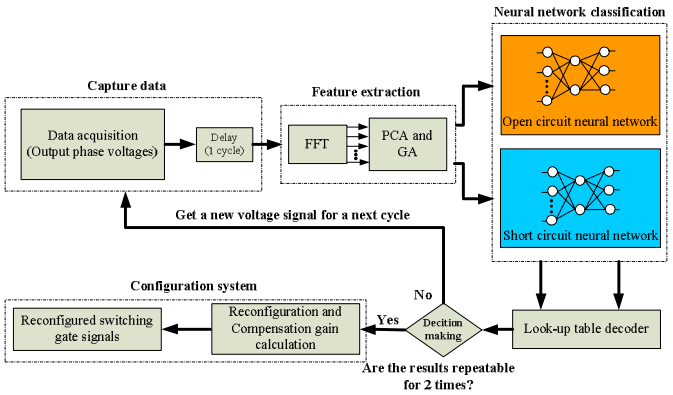


Fig. 8. Fault diagnostic diagram for 11-level MLID with 5 SDCS.

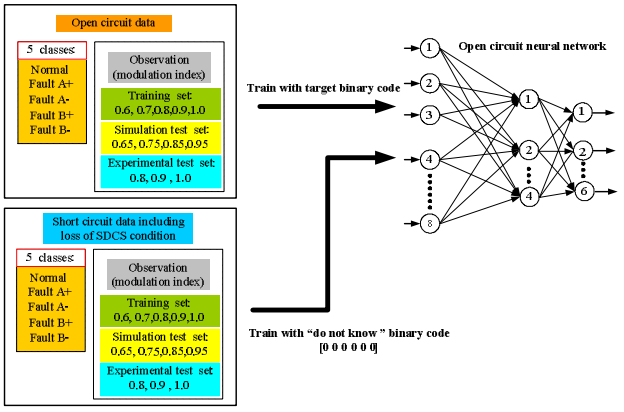


Fig. 9. Training and testing data set diagram.

B. Input/Output Data

The input/output data set diagram for 11-level MLID is illustrated in Fig. 9. We can see that the set of original input data set at each MLID operation point (modulation index) contains five fault classes: normal, Fault A+, A-, B+, and B-. Modulation indices (m_a) are observations changing with desired load. In this particular case, m_a is varied from 0.6 to 1.0 with 0.05 intervals. The original data are divided into two subsets: Open circuit and short circuit. Also, each subset is separated to one training set and two testing sets as shown in Fig. 9. Both open circuit and short circuit neural networks are trained with both open and short circuit training sets. However, the open circuit neural network will be trained with short circuit training set with "do not know" target binary and vice versa with the short circuit neural network as depicted in Fig. 9.

Target binary variables are also illustrated in Table I. Six binary bits are used to code the input/output mapping. The first two bits (counting from the right bits 0 and 1) are utilized to code the faulty switches, the 3rd bit from the right (bit 2) is used to code the fault type, and the last three bits (bits 3, 4, and 5) are used to code which cell has faulted. Also, the code [1 1 1 1 1 1] is used to represent the normal condition, whereas the code [0 0 0 0 0 0] is used to characterize the "do not know" condition. Therefore, the six output neurons are used for particular 11-level MLID. For instance, if the neural network provides [0 1 1 0 0 1] as the outputs, we can decode the fault

TABLE I.
TARGET BINARY CODE FOR 11-LEVEL MLID.

Condition		Number of binary bits and their description					
		Faulty cell			*Fault type*	*Faulty switch*	
		5	4	3	2	1	0
Normal		1	1	1	1	1	1
Faulty cells	1	0	0	1	-	-	-
	2	0	1	0	-	-	-
	3	0	1	1	-	-	-
	4	1	0	0	-	-	-
	5	1	0	1	-	-	-
Fault types	open	-	-	-	0	-	-
	short	-	-	-	1	-	-
Faulty switches	Fault A+	-	-	-	-	0	0
	Fault A-	-	-	-	-	0	1
	Fault B+	-	-	-	-	1	0
	Fault B-	-	-	-	-	1	1
"Do not know"		0	0	0	0	0	0

TABLE II.
PRINCIPAL COMPONENTS SELECTED BY GA FOR 11-LEVEL MLID.

Neural networks	Description	Outputs from *gatool*
Open circuit	*Final point*	*1 2 3 4 5 6 7 8 9 10 11 12 13 14* 1 1 1 0 1 0 1 1 0 0 0 0 1 1 *PC 15-40 are all 0* 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	Fval	0.205
Short circuit with loss of SDCS conditions	*Final point*	*1 2 3 4 5 6 7 8 9 10 11 12 13 14* 0 1 1 1 1 0 1 1 1 0 1 1 1 1 *PC 15-40 are all 0* 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	Fval	0.773

type and location as cell 3 is faulty with open circuit fault at switch S_A-. This decoder paradigm can be implemented in Simulink model by using 2-D dimension look-up table as shown in Fig. 8.

The output binaries provided by the neural networks are also required to give the same classification results for two consecutive times with the same input voltage signal. If the network provides the different classification results, the reconfiguration process will not perform, and then a new cycle of the voltage signal is required for another classification process. This process provides more confidence of the classification result before taking an action. Also, the detection process will allow the diagnostic system to acquire the output voltage signal only two times for short circuit cases and three times for open circuit cases. This means if the detection process can not give repeatable results, an operator will be notified, and then emergency action will be performed.

C. Principal Component Selection

By using the methodology proposed in [15], the principal components (PCs) selected by genetic algorithm (GA) are represented in Table II. As can be seen, 8 PCs are selected for open circuit neural network, whereas 11 PCs are chosen for short circuit neural networks. Also, the same PCs (*1, 2, 3, 5, 7, 8, 13, and 14*) as presented in [15] are selected for open circuit fault neural network. Conversely, the GA chooses different PCs (*2, 3, 4, 5, 7, 8, 9, 11, 12, 13, and 14*) for short circuit neural networks. It should be noted that the training data for short circuit neural network also includes the short circuit fault for loss of SDCS conditions. Interestingly, we know that PC 1 corresponds to the dc component of MLID's output voltages, and this dc component will naturally increase during faulty conditions as explained in [14]. However, GA did not select PC 1 for short circuit neural network. This result suggests that the PC 1 is not so important for short circuit neural network which includes training data of short circuit fault during loss of SDCS conditions. Therefore, the neural network architecture for open circuit neural network has 8 input neurons, 4 hidden neurons and 6 output neurons, whereas the short circuit neural network architecture has 11 input neurons, 4 hidden neurons and 6 output neurons.

IV. SIMULATION AND EXPERIMENT SETUP

A. Simulation Setup

Two simulation programs are used in the simulation setup: Matlab-Simulink and PSIM. Matlab-Simulink is used to implement feature extraction (FFT and PCA), neural network classification, and reconfiguration. A reconfiguration is corrective method to continuously operate a MLID after the faults are detected. The reconfiguration technique used in this research has been proposed in [18]. PSIM is used to implement the MLID power circuit. The reason for using PSIM is that it is a circuit-based simulation software and it conveniently interfaces with Matlab-Simulink via the toolbox called Simcouple [19]. The simulation validation based on Simulink is illustrated in Fig. 10. It should be noted that the same Simulink model is used in both simulation and experiment.

B. Experimental Setup

The experimental setup is represented in Fig. 11. A three-phase wye-connected cascaded multilevel inverter using 100 V, 70 A MOSFETs as the switching devices is used to produce the output voltage signals. The MLID supplies an induction motor (1/3 hp) coupled with a dc generator (1/3 hp) as a load of the induction motor. The Opal RT-Lab system [20] is utilized to generate gate drive signals and interfaces with the gate drive board. The switching angles are calculated by using Simulink model based on multilevel carrier-based sinusoidal PWM with 2 kHz switching frequency. A separate individual power supply acting as SDCS is supplied to each cell of the MLID, consisting of 5 cells per phase as shown in Fig. 1. Open and short circuit fault occurrences are created by physically controlling the switches in the fault creating circuit. A Yokogawa DL 1540c is used to measure output voltage signals as ASCII files. Voltage spectrum is calculated and transferred to the Opal-RT target machine.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Open Circuit Case

The simulation and experimental results are shown in Fig. 12. The faulty power cell (S_{A+}) was placed at cell 2 on phase A

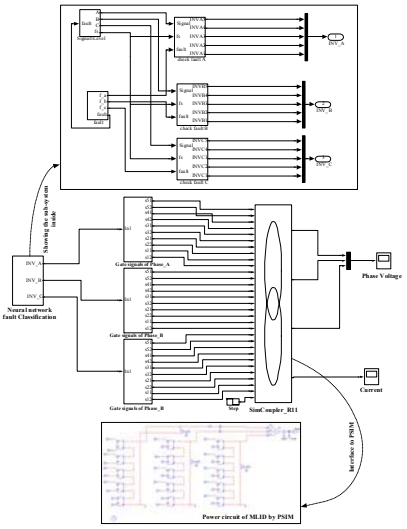


Fig. 10. The fault diagnostic system interfaced with PSIM performing power circuit of a MLID.

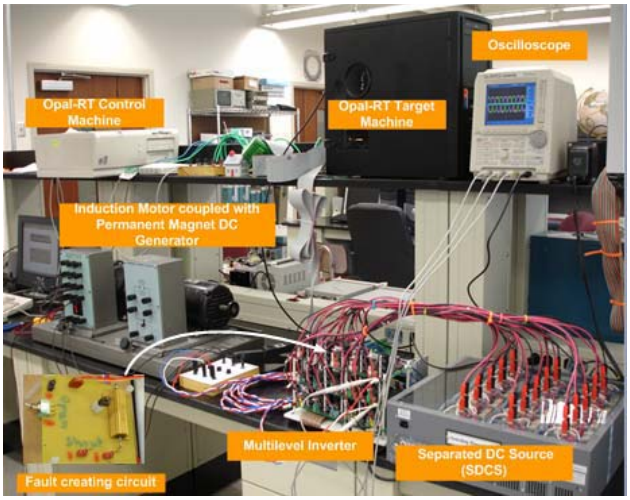
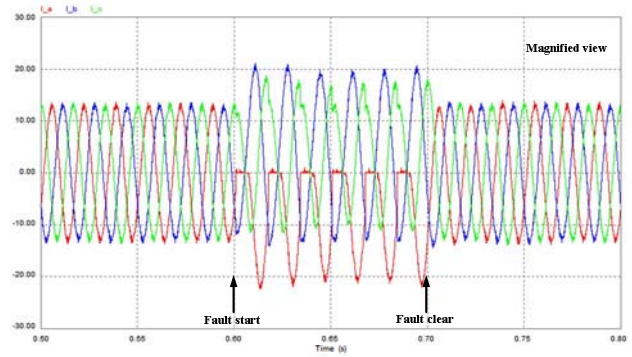


Fig. 11. Experimental setup.

(see Fig. 1), and the multilevel inverter drive was operating at 0.8/1.0 modulation index before the fault occurs. We can see that the simulation and experimental results agree with each other. The fault diagnostic system requires about 6 cycles (~100 *ms* at 60 Hz) to clear the open circuit fault. Obviously, the open circuit fault causes unbalanced output voltage (V_{an}) of the MLID during the fault interval, and the average current on phase A (I_a) has negative polarity during the fault interval.

B. Short Circuit Case

The faulty power cell (S_{A+}) of short circuit case was placed at power cell 3 on phase A (see Fig. 1), and the multilevel inverter drive was operating at 0.8/1.0 modulation index before the fault occurs. The simulation results of a short circuit fault at cell 3 switch S_{A+} are represented in Fig. 13. The fault diagnostic system also requires about 6 cycles to clear the short circuit fault. Obviously, the output voltage (V_{an}) of the MLID is unbalanced during the fault interval (lost negative voltage at phase A), and the average current on phase A (I_a) has positive polarity during the fault interval. The peak of the fault current



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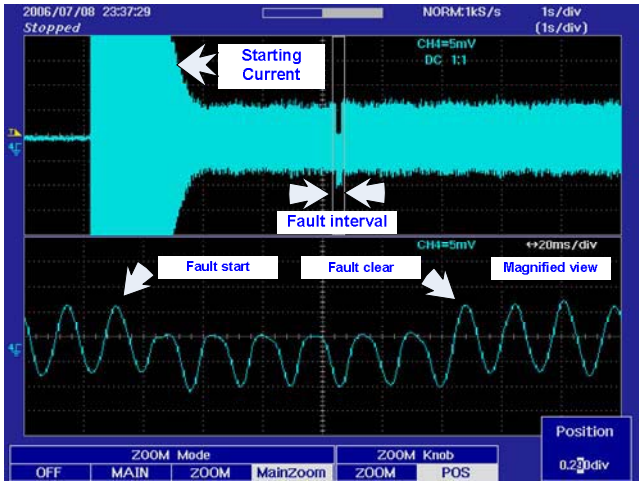


(b)

Fig. 12. Results of the open circuit fault at S_{A+}, cell 2 of the MLID during operation at m_a = 0.8/1.0: (a) Simulation of current waveforms, (b) Experimental result showing line current (I_a) at the faulty phase.

increases about 1.5 times compared with the normal operation. It should be noted that practically, the fuse protecting the SDCS may blow (disconnect the SDCS from a MLID) before the diagnostic system performs fault clearing so that the output phase-voltage will be zero. This behavior of output phase-voltage signals should be taken into account for training the neural network as explained in section III.

The proposed diagnostic system can also detect a short fault under the loss of SDCS condition as the faulty cell condition as shown in Fig. 14. The clearing time for this particular case is about 9 cycles. Also, we found that the neural network can detect which cell has a fault and whether the switch was connected to the positive bus (S_{A+} or S_{B+}) or the negative bus (S_{A-} or S_{B-}). However, the neural network could not determine which specific switch (S_{A+} or S_{B+}) or (S_{A-} or S_{B-}) had failed. Nevertheless, the proposed corrective action taken as explained in [18] can still solve this problem because the fault occurrences at switch S_{A+} and S_{B+} has the same corrective action taken. The faults at S_{A-} or S_{B-} also have the same corrective action taken as clearly explained in [18].

The clearing time of a short circuit fault under the loss of SDCS at faulty cell condition is longer than the open circuit and short circuit faults by about 3 cycles. This result suggests that using only the output voltage signals in the loss of SDCS

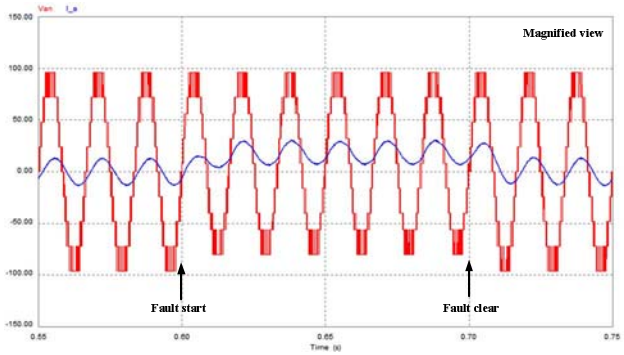
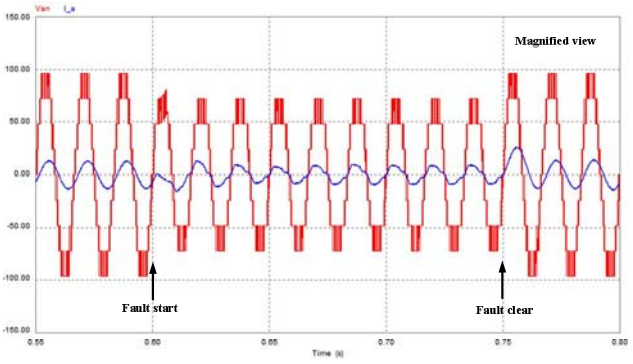
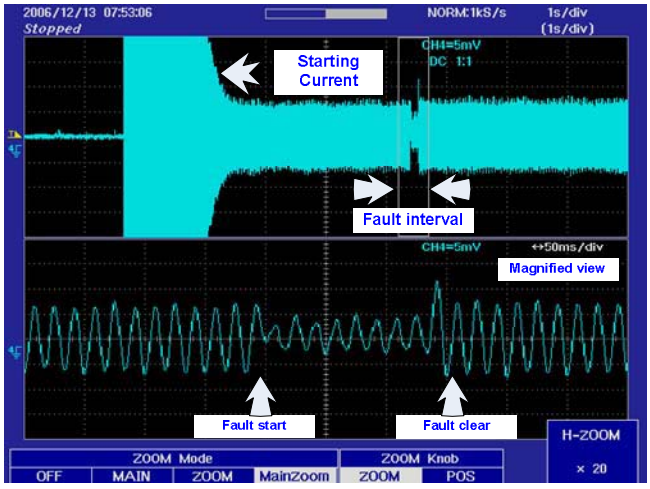


Fig. 13. Simulation results of the short circuit fault at S_{A+}, cell 3 of the MLID during operated at m_a = 0.8/1.0.



(a)



(b)

Fig. 14. Results of the short circuit fault at S_{A+}, cell 3 under loss of SDCS condition at the faulty cell of the MLID during operated at m_a = 0.8/1.0: (a) simulation, (b) experiment showing line current (I_a) at the faulty phase.

case may not adequately provide the unique feature to detect the faults. Therefore, the current signals can be used to determine the different neural network because Fig. 4 shows that the current polarity of the faulty cell can be used to classify the faults at positive or negative dc bus.

VI. Performance Validation

The performance investigation of the proposed diagnostic and reconfiguration system is also evaluated. The objective of this performance investigation is to evaluate the fault clearing

Table III.
Performance Validation.

Fault Types	Multilevel inverter drive at different operating points					
	Current (A)	m_a	Frequency	Fault clearing time (ms)		
				Average	Min	Max
Open circuit fault at Switch S_{B+} of Cell 3	1.56	1.0/1.0	80 Hz	95.8	87.5	112.5
	2.83	0.9/1.0	60 Hz	100	83.3	133.3
	2.26	0.8/1.0	30 Hz	117.2	100	166.6
	2.82	0.6/1.0	15 Hz	150	133.3	200
Loss of gate drive fault at Switch S_{A+} of Cell 3	1.56	1.0/1.0	80 Hz	96.25	87.5	112.5
	2.83	0.9/1.0	60 Hz	100	83.3	116.6
	2.26	0.8/1.0	30 Hz	126.7	100	166.6
	2.82	0.6/1.0	15 Hz	166.6	133.3	266.6
Short circuit at switch S_{A-} of Cell 2	1.56	1.0/1.0	80 Hz	145.8	137.5	162.5
	2.83	0.9/1.0	60 Hz	150	133.3	166.7
	2.26	0.8/1.0	30 Hz	166.7	133.3	200
	2.82	0.6/1.0	15 Hz	200	133.3	333.3

times. The procedure used for this particular investigation is that the MLID was operating at different load and fault conditions and each condition was performed five times. The average, maximum, and minimum clearing time consumed by the proposed system are reported in Table III. As can be seen, the proposed system can detect and reconfigure at different fault types and loads. The current waveforms of the MLID operating under several load conditions are illustrated in Fig. 15 and Fig 16. The consumed time of classification and reconfiguration algorithm can be estimated by subtracting the one cycle delay time required by FFT function. The average consumed time of the algorithm is about 84 ms. We know that the cascaded MLID can tolerate a few cycles of faults; therefore, the detection and reconfiguration system may not need to be very fast execution.

It should be noted that this proposed system was implemented in Opal-RT system. The clearing time can be shorter than this if the proposed system is implemented as a single chip using an FPGA or DSP. However, the proposed system can detect the fault and can correctly reconfigure the malfunctioning MLID. This shows that the proposed diagnostic and reconfiguration paradigm can be applied to MLID applications. Also, by using the proposed system, the reliability of the MLID system can be increased.

VII. Conclusion

The ability of cascaded H-bridge multilevel inverter drives (MLID) to operate under faulty condition with AI-based fault diagnosis and reconfiguration system has been proposed. The proposed fault diagnostic paradigm has been validated in both simulation and experiment.

The fault diagnostic system requires about 6 cycles (~100 *ms* at 60 Hz) to clear the open circuit fault and about 9 cycles (~150 *ms* at 60 Hz) to clear short circuit fault with loss of SDCD. The experiment and simulation results in both open circuit fault and short circuit fault with loss of SDCS are in good agreement with each other. The proposed system can detect the fault and can correctly reconfigure the malfunctioning MLID. The results show that the proposed diagnostic and reconfiguration paradigm can be applied to MLID applications. Also, by using the proposed system, the reliability of the MLID system can be increased.

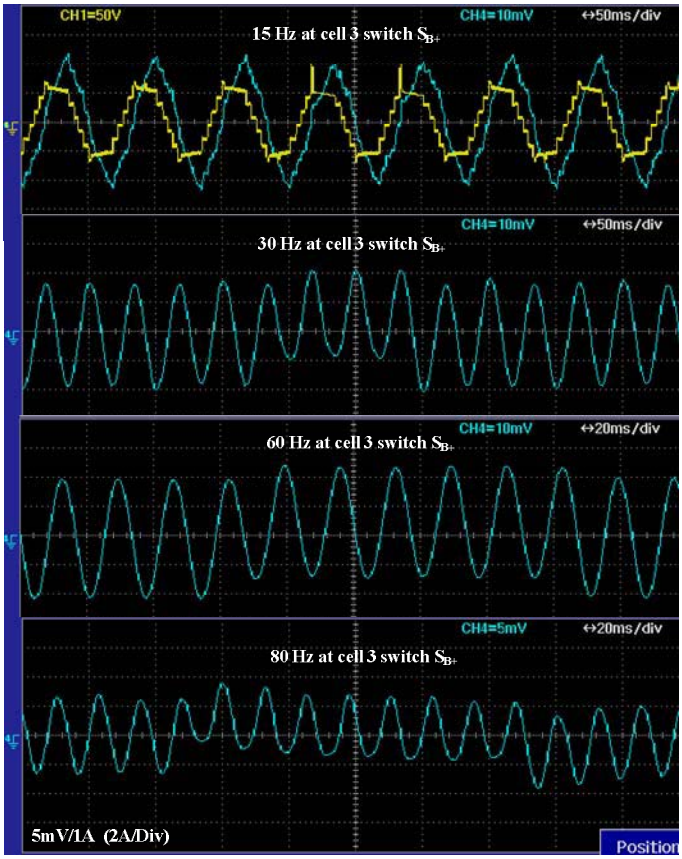


Fig. 15. Operation under open circuit fault condition with different frequencies.

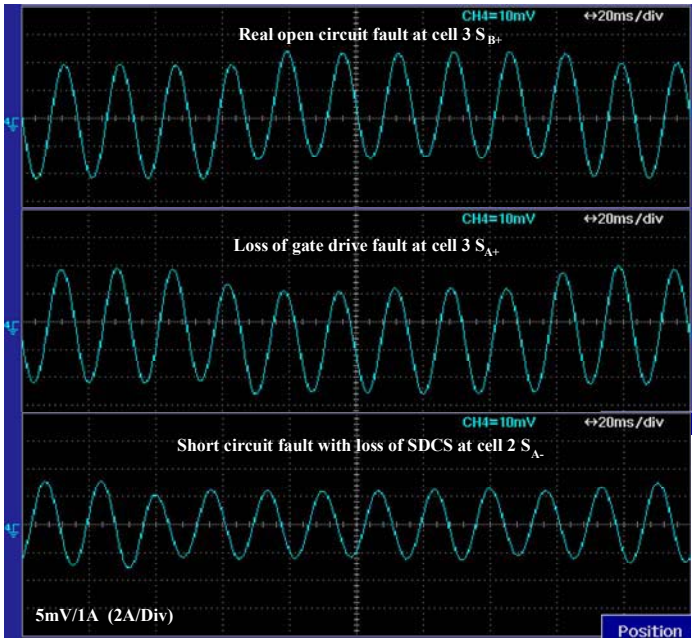


Fig. 16. Operation under different fault type at 60 Hz.

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