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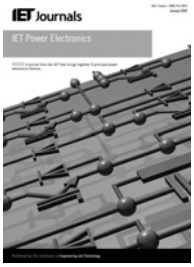

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Silicon-on-insulator-based high-voltage, high-temperature integrated circuit gate driver for silicon carbide-based power field effect transistors

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Abstract: Silicon carbide (SiC)-based field effect transistors (FETs) are gaining popularity as switching elements in power electronic circuits designed for high-temperature environments like hybrid electric vehicle, aircraft, well logging, geothermal power generation etc. Like any other power switches, SiC-based power devices also need gate driver circuits to interface them with the logic units. The placement of the gate driver circuit next to the power switch is optimal for minimising system complexity. Successful operation of the gate driver circuit in a harsh environment, especially with minimal or no heat sink and without liquid cooling, can increase the power-to-volume ratio as well as the power-to-weight ratio for power conversion modules such as a DC–DC converter, inverter etc. A silicon-on-insulator (SOI)-based high-voltage, high-temperature integrated circuit (IC) gate driver for SiC power FETs has been designed and fabricated using a commercially available 0.8-μm, 2-poly and 3-metal bipolar-complementary metal oxide semiconductor (CMOS)-double diffused metal oxide semiconductor (DMOS) process. The prototype circuit's maximum gate drive supply can be 40 V with peak 2.3-A sourcing/sinking current driving capability. Owing to the wide driving range, this gate driver IC can be used to drive a wide variety of SiC FET switches (both normally OFF metal oxide semiconductor field effect transistor (MOSFET) and normally ON junction field effect transistor (JFET)). The switching frequency is 20 kHz and the duty cycle can be varied from 0 to 100%. The circuit has been successfully tested with SiC power MOSFETs and JFETs without any heat sink and cooling mechanism. During these tests, SiC switches were kept at room temperature and ambient temperature of the driver circuit was increased to 200°C. The circuit underwent numerous temperature cycles with negligible performance degradation.

1 Introduction

Automobile industries are developing hybrid electric vehicles (HEVs) to achieve better fuel efficiency [1]. Increasing gasoline cost and the potential shortage of supply in the future are creating an escalating demand for the development of electrical vehicles that have much higher efficiency compared to the traditional internal combustion engines. Electric vehicles need different power electronic modules (DC–DC converter, inverter etc.) for bidirectional power conversion between the energy storage units (battery or ultracapacitor) and the traction system [2, 3].

A typical arrangement of a series/parallel HEV is shown in Fig. 1. The ambient temperature under the hood of the car is usually above 150°C and it can even reach 200°C near the engine [4]. To minimise the cost and to improve the efficiency of HEVs, there is an urgent necessity for miniaturisation and weight reduction of power converter modules. To achieve this goal, electronic circuits capable of

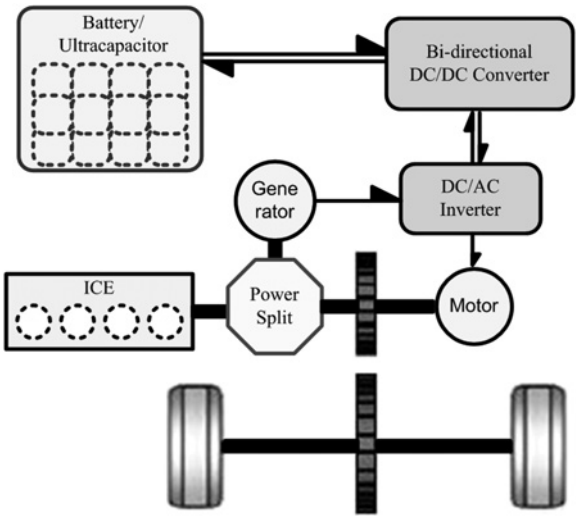

Figure 1 *Typical topological arrangement of series/parallel HEV*

operating at higher ambient temperatures (175°C and above) with minimal thermal management are in great demand. Typically, the heat sink occupies one-third of the volume of the converter and weighs much more than the actual electronics [5]. Current HEV technologies require a separate 70°C cooling loop for commercially available power electronic circuits that are mostly rated for 85°C ambient temperature. Future goal of the automotive industry is to use same 105°C cooling loop that is used for engine to cool the electronics under the hood. By removing the extra cooling unit and by reducing the size of the heat sink, an order of magnitude savings in overall mass and volume of the power electronic modules can be achieved.

Silicon-based switching devices have approached the theoretical limits for high-power and high-temperature applications. Silicon carbide (SiC), which is a wide bandgap material, has emerged as an alternative semiconductor to overcome the limitations of silicon. SiC device operation at up to 500°C has been reported in the literature [5], whereas Si-based devices can only operate at a maximum junction temperature of 150°C [5, 6]. Hence SiC-based power switches are expected to be the switch of choice for power electronic circuits in harsh environments where the ambient temperature can exceed 200°C. In all power electronic modules (DC–DC converter, inverter etc.), gate drivers are essential components to control the turning ON and OFF of power switches. Placing the gate driver circuit next to the power switch can improve the performance by reducing the parasitic inductances associated with long wires. Long interconnects are also a potential source of failure, especially in a harsh environment. These converter modules are likely to be placed under the hood of the car. Hence, the ambient temperature of the gate driver integrated circuit (IC) can also be as high as 175°C. A gate driver IC capable of operating at elevated temperatures (≥175°C) can contribute to the reduction of weight and volume of the power conversion modules as well as improve the reliability.

This work presents a robust high-temperature gate driver IC for SiC field effect transistor (FET) switches that are expected to be used in power electronic modules for extreme environment applications like HEVs. An earlier version of this circuit was presented in [7]. The prototype of this high-temperature, high-voltage gate driver IC has been developed using bipolar-CMOS-DMOS (BCD) on silicon-on-insulator (SOI) technology. This circuit has been successfully tested at 200°C ambient temperature for multiple thermal cycles without any heat sink or cooling mechanism. SiC power MOSFETs from Cree and SiC power JFETs from SemiSouth were driven by this gate driver IC. Simulation and experimental results are presented here to demonstrate the effectiveness of the gate driver IC.

2 High-temperature gate driver circuit

Different types of gate driver circuits for insulated gate bipolar transistor (IGBT) and FET-based power switches have been proposed in the literature [8–12]. None of these reported gate drivers, however, operate above 125°C ambient temperature. Bulk Si-based processes used to fabricate these prior art gate drivers suffer from leakage current at higher temperatures. Owing to this leakage current, power consumption of an IC may increase dramatically, making the die temperature much higher than the ambient. Thus junction leakage is a major concern for the reliability of electronic circuits at high temperature. Almost all the commercial gate drivers that are fabricated using bulk CMOS processes have limited operating temperature range.

SOI technology, however, is more attractive for high-temperature applications because of its low leakage current. The dielectric isolation between neighbouring devices and between channel and substrate reduces the leakage path associated with the drain and the source p–n junctions [13]. For SOI-based devices, threshold voltage variation with temperature is also smaller compared to Si-based bulk devices [14]. SOI also provides improved latch-up immunity, which ultimately increases the reliability of the circuit operation at higher temperature [13]. Modern day processes offer the opportunity of integrating high-voltage devices along with low-voltage devices on SOI substrates. Such a process that combines the advantage of high-voltage devices with SOI technology has been chosen for the design and implementation of the proposed high-voltage, high-temperature gate driver circuit.

A low-loss high-frequency half-bridge gate driver circuit on SOI for driving MOSFET switches was presented in [15]. However, there was no mention of the temperature capability of that circuit. In this work, a similar circuit topology has been used with necessary modifications as

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required for high-temperature operation and large drive signal generation for the SiC FET switches (MOSFET, JFET) under consideration.

3 Gate driver circuit

Fig. 2 shows the block diagram level circuit topology of the gate driver designed in this work. This circuit has six distinct building blocks, namely high-voltage half-bridge output stage (transistor pair M_H and M_L), low-side and high-side buffers, bootstrap capacitor-based charge pump, low-side to high-side level shifter (M_S, M_R, R_S and R_R), dead zone generator and latch controller. The high- and low-side buffers drive the gates of the high-side and low-side transistors in the half-bridge output stage, respectively. The bootstrap capacitor (C_B)-based charge pump establishes a voltage above the available highest rail voltage, which works as a floating battery for the level shifter, SR latch and high-side buffer. The high-voltage level shifter converts the incoming digital input signal from the low-side voltage level (V_{DD}) to the high-side voltage level (V_{DDH}). The purpose of the pulse generator block is to generate the appropriate timing pulses (S and R) to turn ON and OFF the high-side transistor. The dead zone generator generates two non-overlapping copies of the logic-level input signal. The dead time provided between these two copies ensures the complementary turning ON and OFF of the transistors in the output stage.

3.1 Half-bridge high-voltage output stage

The half-bridge output stage connects the gate terminal of the power FET to one of the two rail voltages. The rail voltages (V_{DDH} and V_{SS}) are set depending on the gate voltage requirement of the power switch that the driver IC is controlling. The key factors that should be considered when choosing the half-bridge topology are reverse breakdown voltage, ON resistance and switching speed. The topology used in this circuit, as shown in Fig. 2, consists of two high-voltage n-channel metal oxide semiconductor (NMOS) transistors (laterally diffused metal oxide semiconductor (LDMOS)) stacked together. The NMOS transistor has lower ON resistance and higher switching speed when compared to its p-channel metal oxide semiconductor (PMOS) counterpart. Since the peak-to-peak output voltage is large, it needs to switch fast to minimise switching losses. Gate voltage for the top NMOS device is either set at V_{SS} (when M_L is ON and M_H is OFF) or at $V_{OP} + V_{DD} - V_{D1} - V_{ML\text{-}ON}$ (when M_L is OFF and M_H is ON), where V_{D1} is the forward voltage drop across D_1, $V_{ML\text{-}ON}$ is the ON voltage of the M_L NMOS and V_{OP} is the output voltage generated by the circuit. To generate a voltage above the highest rail voltage, a bootstrap capacitor-based charge pump is used [15, 16].

3.2 Bootstrap capacitor-based charge pump

The bootstrap circuit, consisting of diode (D_1) and bootstrap capacitor (C_B), supplies a voltage level higher than the highest voltage made available to the chip. Fig. 3 shows the circuit operation of the charge pump. When the output is low such that V_{OP} is tied to V_{SS}, the bootstrap capacitor is charged to $V_{DD} - V_{D1} - V_{ML\text{-}ON}$ as shown in Fig. 3*a*. In the next phase (Fig. 3*b*) when the top-side NMOS (M_H) is turned ON, the output V_{OP} starts to increase making the diode D_1 reversed biased, and the voltage across the capacitor starts working as a floating battery with V_{OP} as the floating reference. This voltage is required for the high-side buffer, SR latch and level shifter in order to generate the required gate signal (V_{GH}) for the M_H transistor. The V_{OP} and $V_{OP\text{-}PLUS}$ voltages work as the floating rail voltages for the high-side circuitry. This circuit takes 60 ns to be fully operating due to charging of this bootstrap capacitor. The value of C_B is typically on the order of nanofarads. In this prototype, a 1.25-nF capacitor was included on the chip, integrated with the gate driver circuit. Provisions were also provided for the connection of an off-chip bootstrap capacitor. The on-chip bootstrap capacitor was implemented using metal-oxide-semiconductor capacitor

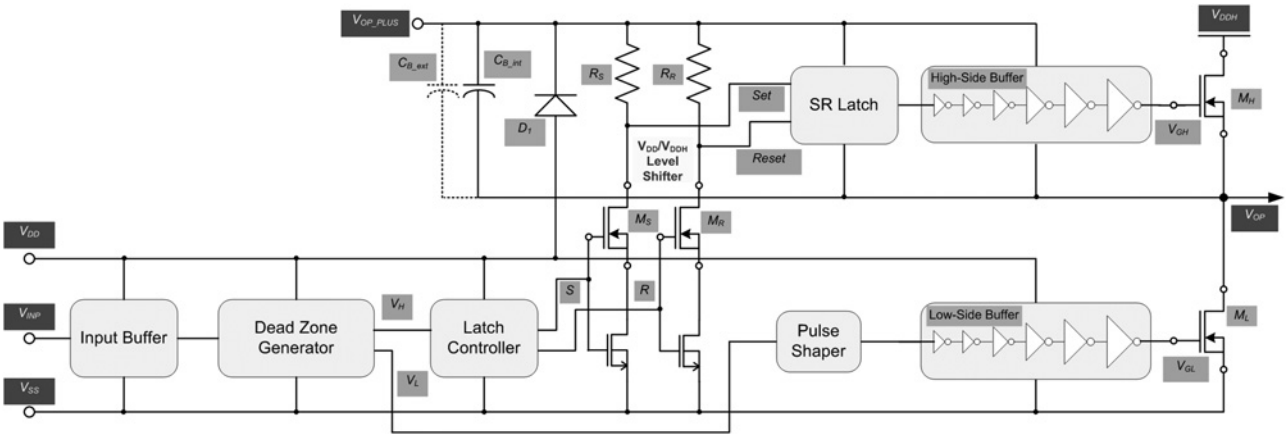

Figure 2 *Schematic of the high-voltage, high-temperature IC gate driver*

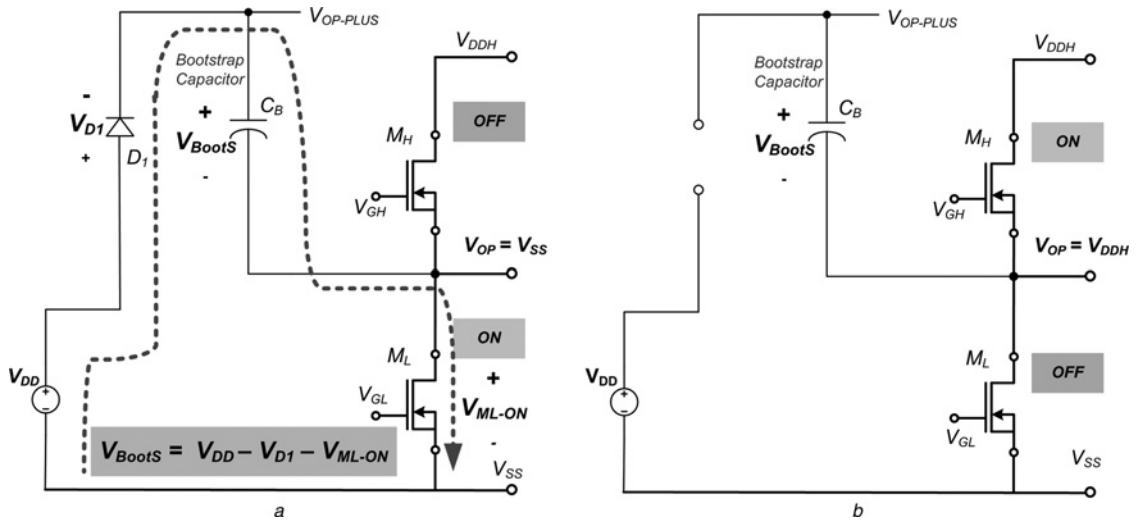

Figure 3 *Bootstrap capacitor-based charge pump operation*

a Charging the capacitor
b Voltage across the capacitor working as a floating battery

(MOSCAP). Total area taken by this capacitor is 0.73 mm^2, which is almost 15% of the total chip size. Capacitance per unit area of MOSCAP is almost two times the same of polysilicon-oxide-polysilicon capacitor, which was the other option available in the SOI process used for this work.

3.3 Dead zone generator

To reduce the power consumption of the chip and to ensure the reliability of the circuit, it is very important to maintain complementary turning ON and OFF of the two high-voltage NMOS transistors in the output stage. Overlapping turning ON of both the transistors will create a short circuit between the rail voltages (V_{DDH} and V_{SS}) resulting in large short circuit or 'crowbar' current. This large current will increase the die temperature much higher than the ambient temperature. To ensure a break-before-make type operation, a dead zone generator and a pulse shaper circuit are included in this design. These two circuits inject a dead time between the gate drive signals (V_{GH} and V_{GL}) for the NMOS transistors M_L and M_H in the output stage.

Fig. 4 shows the schematic of the dead zone generator that uses similar circuit topology to that of a complementary clock generator with the addition of delay components. This circuit

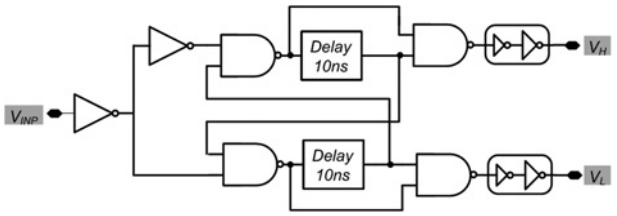

Figure 4 *Dead zone generator circuit*

generates two non-overlapping complementary copies (V_H and V_L) of the buffered input signal. Since the pulse trains generated by this circuit pass through different circuit components, an additional 'pulse shaper' circuit is used to further modify the low-side gate signal to ensure complementary switching.

3.4 Latch controller

The latch controller unit takes the V_H signal as the input and generates two pulses (S and R in Fig. 5) with very short duration (10 ns) at the rising and falling edges of the incoming input signal. These signals are used to set and reset the SR latch. The S pulse sets the latch to $V_{OP\text{-}PLUS}$. Latch output is passed through the non-inverting high-side buffer to boost its current driving capability. The output of the buffer controls the gate of the high-side NMOS (M_H). The duration of the S and R pulses is designed to be the minimum time required to turn ON the high-voltage M_S and M_R NMOS transistors in the level shifter. This ensures the minimum power dissipation in the R_S and R_R resistors.

3.5 Level shifting of control signal

The target peak-to-peak gate voltage of this driver is higher than 30 V. Hence, the incoming 5-V logic signal needs to be level shifted to the high-voltage level. A level-shifting circuit was added to convert the low-voltage level control signal to the desired high-voltage level to generate the gate voltage (V_{GH}) for the M_H transistor. The high-side transistor's source is connected to the output terminal. Therefore its gate voltage needs to be either at V_{OP} (to turn it OFF) or at $V_{OP\text{-}PLUS} = V_{OP} + V_{DD} - V_{D1} - V_{ML\text{-}ON}$ (to turn it ON). Two high-voltage NMOS transistors (M_S and M_R) along with two resistors R_S and R_R perform this level shifting operation. They turn ON

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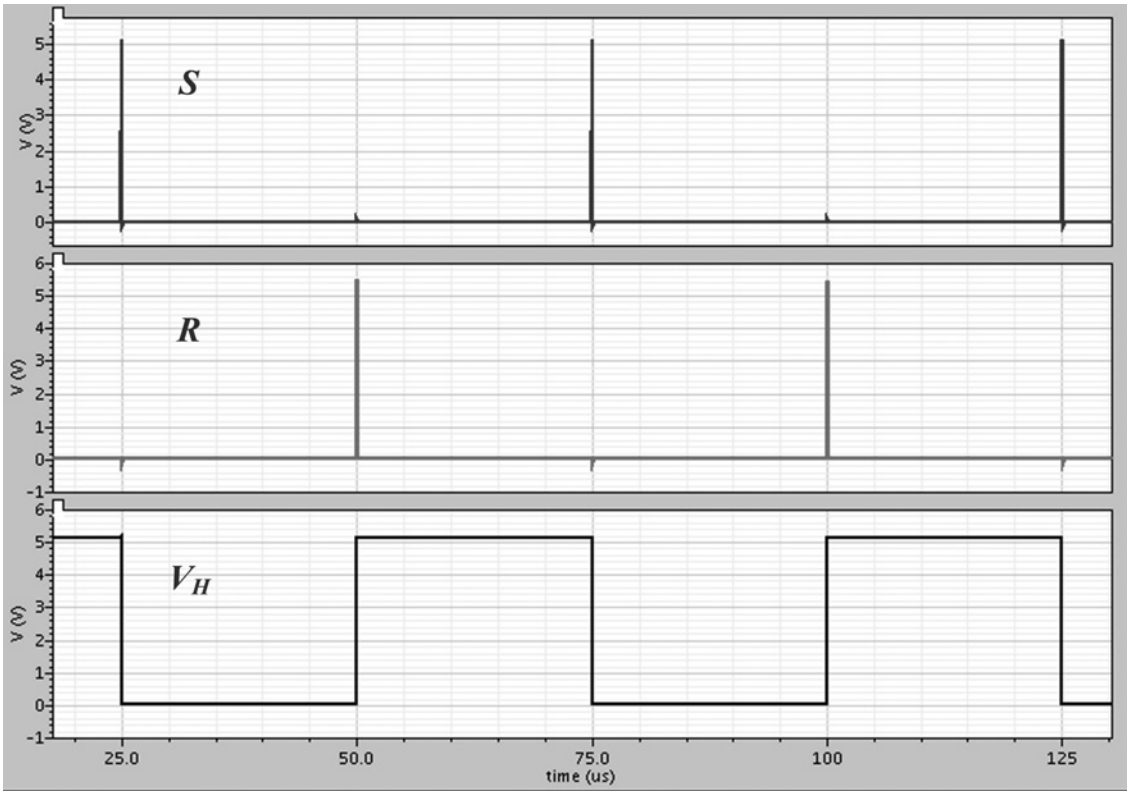

Figure 5 *S and R pulses generated by the latch controller circuit from incoming V_H signal*

alternately for very short duration, allowing short current pulses to flow through the resistors from the high to low side. The voltage drops across R_S and R_R work as the '*set*' and '*reset*' signals for the active-low *SR* latch, which in turn generates the gate signal for the high-side transistor, M_H.

3.6 High- and low-side buffers

Both transistors of the half-bridge stage are comprised of a large number of parallel-connected high-voltage transistors. Equivalent width of each of these transistors is 28 000 μm, which presents large capacitive loads to the signals coming from the latch and the pulse shaper. Multi-stage non-inverting buffers consisting of a series of amplifying inverters are used to generate the gate signals with sufficient drive strength for the large gate capacitances of the M_L and M_H transistors. To minimise the delay through these buffers, the size of each stage was made approximately '*e*' (the base of natural logarithm) times larger than its previous stage, forming the exponential 'horn' pattern [17].

4 Design and fabrication

Schematic level simulations were performed over a wide temperature range from −40 to 175°C. The circuit was simulated with a capacitive load of 10 nF in series with 10 Ω resistance to resemble the actual load condition (gate of SiC FET power switches). From the simulation it was confirmed that there is no leakage current through the transistors in the output stage during the switching instances. All the simulations were performed using foundry-provided model parameters. Bond wire and package parasitic inductances and resistances were also taken into consideration during the simulation.

A prototype of the high-temperature gate driver IC was designed and fabricated using a commercially available 0.8-μm, 3-metal and 2-poly BCD on SOI process. Fig. 6 shows the chip micro-photograph. The gate driver circuit occupies an area of 5 mm^2 (2.24 mm × 2.24 mm) including bootstrap capacitor, bonding pads and electrostatic discharge (ESD) protection. The two high-voltage NMOS devices of the half-bridge output stage

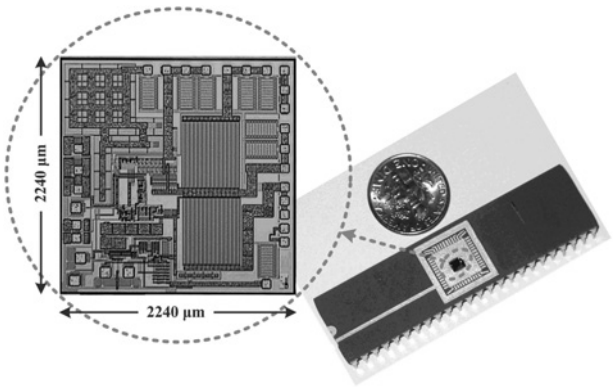

Figure 6 *Micro-photograph of the high-temperature gate driver IC in comparison with a dime*

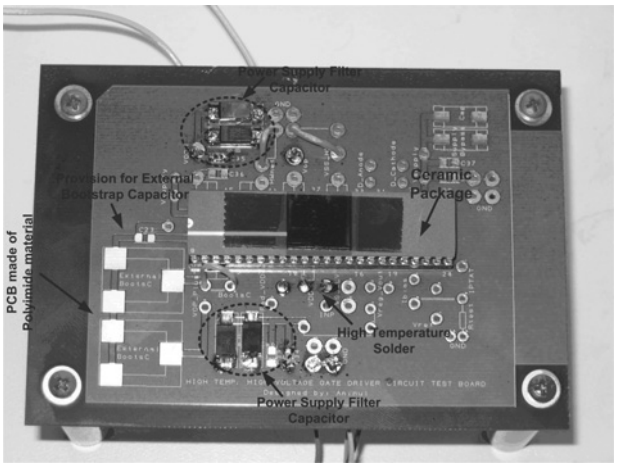

Figure 7 *High-temperature test boards made of polyimide material*

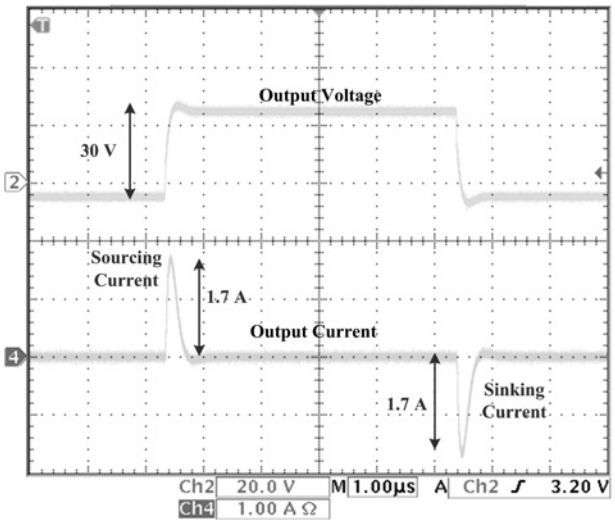

Figure 8 *Circuit's drive signals at 175°C with 10 nF capacitive load (time scale: 1 µs/division)*

occupy a major portion of the chip area. They are sized ($W/L = 28\,000\ \mu m/1.6\ \mu m$) to provide large peak current as needed to obtain acceptable rise and fall times. Each of these NMOS transistors is comprised of seven hundred 45-V NMOS devices (each with $W = 40\ \mu m$) connected in parallel. The layout of the high-voltage devices resembles a 'race-track' structure [18]. Multiple pad connections are used for the power supply and output nodes to minimise the parasitic bond wire inductance.

A critical failure mechanism that becomes more severe at higher temperature is electromigration. In this process current flow over time gradually displaces microscopic metal traces on interconnects with high current density, and eventually leads to an open-circuit condition [19]. To avoid this phenomenon, all the critical metal interconnects in gate driver circuit were made wide enough to reduce the current density through them.

Bare dies were bonded in ceramic packages for high-temperature testing. A double-layer printed circuit board (PCB) was designed to mount the chip and power supply filter networks. Fig. 7 shows one of the test boards that was used for this testing. These boards were fabricated using polyimide material, which can withstand temperatures higher than 200°C. High-temperature solder was used to connect all the components to the PCB. All the connection wires to the PCB used during testing have insulation made of Teflon so that they can safely operate at 200°C.

5 Measurement results

The chip was first tested with series-connected 10-Ω and 10-nF load at different ambient temperatures by placing the test board inside a temperature chamber. Fig. 8 shows the 30-V peak-to-peak (−5 to 25 V), 20-kHz gate pulse signal generated by the chip at 175°C ambient temperature with the above-mentioned load condition and without any cooling mechanism. The drive current wave shape is also shown in Fig. 8. At room temperature, the peak sourcing and sinking current were 1.8 A. At 175°C these peaks dropped down to 1.7 A.

This chip was also tested for 40 V peak-to-peak (−10 to 30 V) gate pulse with 10 nF capacitive load. At 125°C ambient temperature the peak sourcing/sinking currents were 2.3 A. Above 125°C temperature, the Tantalum capacitors (rated for 175°C) used in the test board for power supply filtering became resistive, drawing leakage current. Consequently, the rail-to-rail voltage of the circuit was reduced to 30 V to continue the test up to 175°C. Readings were taken 15 min after the temperature of the chamber reaches the target temperature to ensure that the chip temperature is same as the ambient temperature (inside the oven).

Next a SiC power MOSFET (1200 V, 10 A) prototype, developed by Cree was tested with this gate driver chip. An 80-Ω load (in series with the drain terminal) was used with the SiC MOSFET in a common-source configuration, and the bus voltage was set at 320 V. A 4-A peak load current was passing through the MOSFET when it was turned ON by the gate driver chip. 20 V peak-to-peak (+15 to −5 V) drive signal was applied to the gate terminal of the SiC MOSFET through a 10-Ω current limiting resistor. The test board was placed inside the temperature chamber, and the SiC MOSFET was kept outside the chamber as it was not packaged for high-temperature applications. Starting from room temperature, the chip was tested up to 200°C. Switching frequency was set at 20 kHz and the duty cycle was 10%. Fig. 9 shows the schematic of the test set-up for the SiC power switches (MOSFET and JFET).

Fig. 10 shows the gate voltage, gate drive current, MOSFET drain terminal voltage and load current waveforms at 200°C. The temperature of the chamber was

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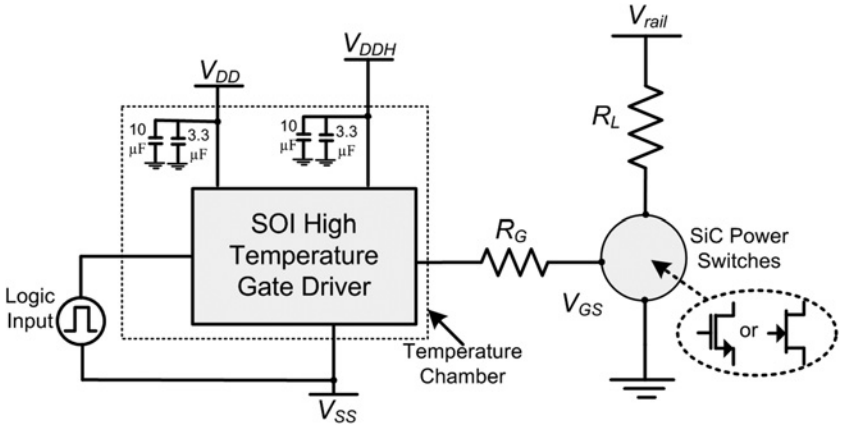

Figure 9 *Schematic of test set-up for MOSFET ($V_{DDH} = 15$ V, $V_{SS} = -5$ V) and for normally ON JFET ($V_{DDH} = 3.4$ V, $V_{SS} = -31.6$ V)*

For both tests $V_{DD} = 5$ V and $R_G = 10\ \Omega$

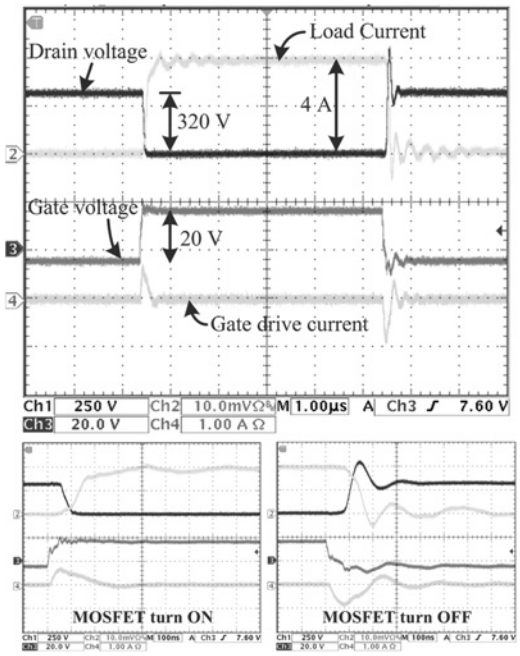

Figure 10 *Prototype circuit's test results at 200°C when driving SiC MOSFET*

raised from room temperature to 200°C in five steps (85, 125, 150, 175 and 200°C). Fig. 10 also shows the time scale magnified version of the MOSFET switching edges. The ringing effect observed in the wave shapes was due to the added parasitic inductances of the connecting wires that ran from inside the temperature chamber to the outside. In all, 10–90% rise time and 90–10% fall time for both the gate drive voltage signal and MOSFET drain voltage at each temperature level are recorded in Table 1. These readings showed that this high-temperature gate driver circuit maintains a fairly constant driving strength over the entire test temperature range.

This gate driver circuit was also tested with SiC normally ON JFET (1200 V, 10 A) sample from SemiSouth. The prototype gate driver circuit was used to generate a 35-V peak-to-peak (−31.6 to 3.4 V) gate signal to control the JFET, which was connected to a 160 V bus through a 40-Ω load resistor. Fig. 11 shows these test results at room temperature. This driver IC was also tested up to 200°C with the JFET where the bus voltage was set to a relatively low voltage (50 V). The duty cycle of the gate drive signal was also varied from 0 to 100% in 1% increment.

Table 1 Rise time and fall time at different ambient temperatures

Ambient temperature, (°C)	Drain voltage, (V_{DS})		Gate voltage, (V_{GS})	
	t_{rise}, ns	t_{fall}, ns	t_{rise}, ns	t_{fall}, ns
25	24.1	40.9	42.3	55.6
85	20.9	39.3	42.8	55.6
125	24.8	41.2	43.5	61.1
150	23.5	39.2	43.9	63.7
175	25.2	41.9	43.7	65.5
200	25.1	41.5	43.5	63.3

None of the circuit components used in this driver circuit requires continuous biasing current. Hence power loss inside the chip is very small, which helps to keep the increase in die temperature over ambient at a very low level. At room temperature, power loss in the prototype driver circuit is measured to be 4.89 mW while driving the SiC MOSFET and 101 mW for SiC normally ON JFET. With the increase of operating temperature, higher power losses in the driver circuit were observed especially when it was driving the JFET. At 175°C ambient temperature, power losses in the chip increased to 6.31 and 180 mW for MOSFET and JFET, respectively.

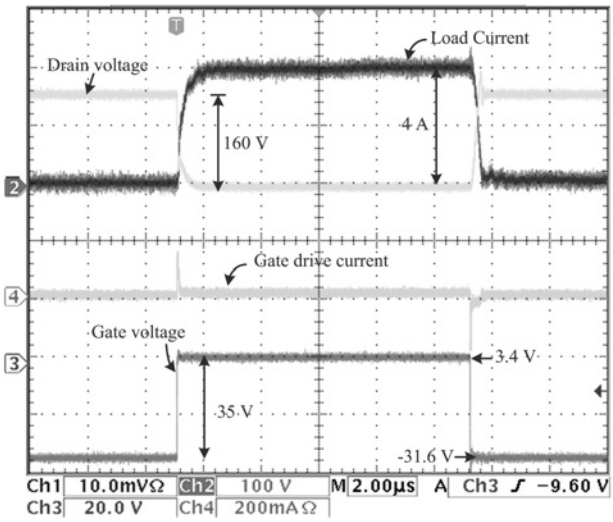

Figure 11 *Prototype circuit's test results at room temperature when driving SiC normally ON JFET*

6 Conclusions

The high-temperature, high-voltage IC gate driver presented in this paper is a preliminary research effort to design SiC-based high-temperature DC–DC converter and three-phase inverter modules for HEVs. This driver IC will be placed adjacent to the SiC switches, and the whole converter module will be placed under the hood where the ambient temperature may rise to 175°C. The prototype chip has been successfully tested up to 200°C ambient temperature without cooling techniques. It was tested generating a 40-V peak-to-peak gate drive voltage and maximum sourcing and sinking currents of 2.3 A. The rise and fall times of the gate drive signals generated by the chip for SiC MOSFET remain fairly constant over a wide temperature range of 25–200°C. This SOI-based driver IC can also be used in other power electronics modules where SiC power switches are needed with ambient temperature higher than 125°C, beyond the maximum operating range of bulk Si-based gate drivers. This SOI-based high-temperature gate driver IC will extend to the system level the advantages of high-temperature capabilities provided by wide bandgap power devices such as SiC-based power FETs.

7 Acknowledgment

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