

A High-Temperature, High-Voltage Linear Regulator in 0.8- μm BCD-on-SOI

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Abstract

The sale of hybrid electric vehicles (HEVs) has increased 10 fold from the year 2001 to 2008 [1]. Thus, high temperature electronics for HEV applications are desired in the engine compartment, power train, and brakes where the ambient temperature normally exceeds 150°C. Power converters (i.e. DC-DC converter, DC-AC inverter) inside the HEVs require Gate-Driver ICs to control the power switches. A Gate-Driver IC needs a step-down voltage regulator to convert the unregulated high input DC voltage (V_{DDH}) to a regulated nominal CMOS voltage (i.e. 5 V), this step-down voltage regulator will supply voltage to the low-side buffer (pre-driver) and other digital and analog circuits inside Gate-Driver ICs. A linear voltage regulator is employed to accomplish this task; however, very few publications on high temperature voltage regulators are available. This research presents a high temperature linear voltage regulator designed and fabricated on a commercially available 0.8- μm BCD-on-SOI process. SOI processes offer 3 orders of magnitude smaller junction leakage current than bulk-CMOS processes at temperatures beyond 150°C. In addition, a pole swap compensation technique is utilized to achieve stability over a wide range (4 decades) of load current. The error amplifier inside the regulator is designed using an inversion coefficient methodology, and a temperature stable current reference is used to bias the error amplifier. The linear regulator provides an output voltage of 5.3 V at room temperature and can supply a maximum load current of 200 mA.

Keywords-high temperature electronics, voltage regulator, inversion coefficient, temperature stable current reference, pole swap technique

I. INTRODUCTION

The application of high temperature electronics could be found among well logging, aerospace, nuclear and automotive industries. This research targets automotive applications, specifically for the hybrid electric vehicles (HEVs) which require high performance automotive electronics to achieve high output power, better fuel efficiency and clean exhaust [2]. The power converter modules (DC-DC converters and DC-AC inverter) for automotive application are normally placed under the hood, where the ambient temperature is around 150°C to 200°C. Inside the power converter module of HEVs, the gate driver ICs controls power switches' "on" and "off" operation [3]. Nowadays, most of the power switches (i.e. IGBT, Power MOSFET, and JFET) are made of silicon material. However, the silicon power switch suffers device property limitations on breakdown voltage, operating temperature, current density and switching losses. Therefore, the power switches made of wide-bandgap material such as SiC and GaN could be employed to replace silicon power switches in the near future.

Gate driver ICs in automotive applications require step-down voltage regulators to power the

low voltage circuitry, including the digital blocks and low-side buffer. A linear voltage regulator is normally used in this application rather than a switching-mode voltage regulator because of its chip area utilization efficiency, less complex design, low noise, and it does not require a high temperature off-chip inductor. In addition, high temperature voltage regulator designs for automotive applications are required to be reliable at elevated temperature. SOI fabrication processes are more suitable for analog circuits operated at elevated temperature compared to bulk-CMOS fabrication processes due to the reduced junction leakage current. As shown in Figure 1, bulk-CMOS analog ICs will suffer significant

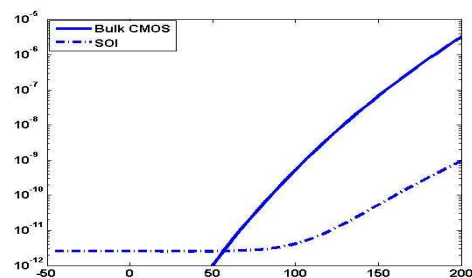


Fig. 1. Simulation of leakage current in Bulk-CMOS and SOI Process

performance degradation at elevated temperatures due to the effect of leakage current[4]. In addition to the fabrication process technology, circuit design techniques need to be addressed for high temperature IC design. An important concept for maintaining the linearity of the circuit over temperature is to minimize the temperature coefficient of the biasing current. Stability and matching are also very crucial for amplifiers, voltage regulators, ADCs and oscillators operating at elevated temperature [5]. The goal of this research is to develop a voltage regulator capable of supplying a stable DC voltage at elevated temperature. This work utilizes the high temperature analog IC design techniques and methodologies to design an error amplifier and temperature stable current reference that are critical analog blocks for a high temperature linear voltage regulator.

The high temperature linear voltage regulator is introduced in section II. The design methodology for the error amplifier is discussed in section III. Section IV presents the temperature stable current reference. Frequency analysis of the linear voltage regulator and the pole swap technique are explained in section V. Finally, simulation results are presented in section VI.

II. HIGH TEMPERATURE LINEAR VOLTAGE REGULATOR

Figure 2 shows the block diagram of a high temperature linear voltage regulator. This circuit consists of a pre-regulator, bandgap voltage reference (BGR), temperature stable current reference and a voltage regulator as shown in Figure 3. The pre-regulator will reduce the V_{DDH} voltage into two separate supply voltages, 9 V and 5.6 V. The 9-V supply is connected to the cascode current mirror load of error amplifier and reference current generation circuit (IREF2). The 5.6-V supply is connected to the bandgap voltage reference, reference current generation circuit (IREF1) and the input pair of the error amplifier. With the lowered supply voltage, use of high voltage devices (DMOS) can be minimized. Regular MOSFETs are 3 times smaller than the DMOSFETs. In addition to increasing the chip area efficiency, a lower V_{DDH} will help prevent issues related to exceeding the gate-source breakdown voltage. The pre-regulation scheme also helps enhance rejection of the supply noise on the V_{DDH} rail.

Inside the pre-regulator, a 45 V high-voltage transistor (n-type DMOS) is employed to provide the bias current needed for the BGR, temperature stable current reference, and error amplifier. The BGR

circuit provides the reference voltage to the non-inverting terminal of the error amplifier. V_{ref} is designed to be 2.2 V; hence, the feedback factor β is about 0.4.

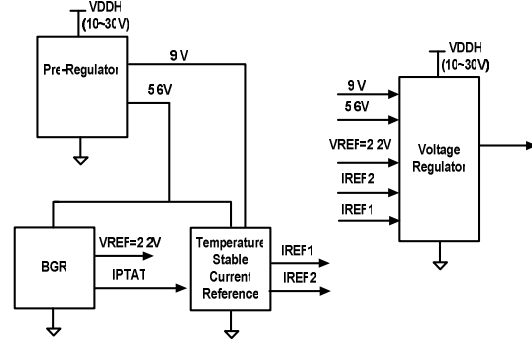


Figure 2. Block diagram of high temperature linear voltage regulator

The load regulation of the regulator is inversely proportional to the feedback factor. If the feedback factor can be maximized, the load regulation will be improved. When the output voltage of the regulator must be greater than the typical BGR output of about 1.25 V, then the feedback factor of the regulator, β , must be less than 1. The V_{ref} of the BGR can be expressed as

$$V_{ref} = 2V_{BE} + 2 \frac{R_2}{R_1} V_T \ln(K) \quad (1)$$

where V_T is thermal voltage, K is the number of diodes in parallel, R_1 and R_2 are the resistors in the PTAT leg and the output reference voltage leg of the BGR circuit. The second term of Equation (1) can be used to cancel the temperature coefficient (TC) of the diode, which exhibits a negative TC. BGRs are widely employed in designing voltage regulators. A Zener diode could be another option for implementing a reference voltage (if available in the target fabrication process), but its temperature dependent voltage makes it undesirable for high or wide temperature applications. For this reason, a BGR is utilized in the design.

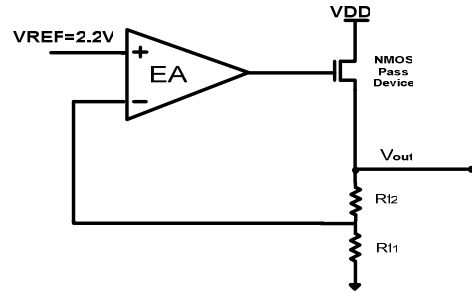


Figure 3. Block diagram of linear voltage regulator in Figure 2

Figure 3 depicts the block diagram of the voltage regulator. A high voltage n-type DMOS is utilized as a pass transistor. The error amplifier, the feedback resistor and the pass transistor form a negative feedback loop. The output voltage can be expressed as

$$V_{out} = V_{ref} \cdot \left(1 + \frac{R_{f2}}{R_{f1}}\right) \quad (2)$$

A high temperature linear voltage regulator requires a high performance error amplifier. A temperature stable biasing current will prevent the power consumption of the error amplifier from increasing needlessly over temperature, and preserve its stability. The design of a high performance wide temperature range error amplifier depends on the availability of a stable current reference [6].

III. INVERSION COEFFICIENT DESIGN METHODOLOGY

An Error Amplifier (Operational Transconductance Amplifier) is the fundamental building block for linear voltage regulators. Its higher open-loop gain will enhance the overall performance of a linear regulator. The lower quiescent current consumption of the OTA is very important for improving the current efficiency of the linear regulator and reducing the power dissipation. [9,10] presented high temperature linear voltage regulators in SOI and BiCMOS processes, respectively. However, both [9, 10] lack treatments in addressing the design methodology of an OTA at high temperature. This work presents a high temperature OTA design based on the inversion coefficient design methodology. The inversion coefficient can offer the circuit designer a meaningful insight in selecting MOSFETs operating in weak, moderate, and strong inversion. Optimization of the circuit performance is easily achieved by utilizing the inversion coefficient [11, 13]. In [13], moderate inversion optimizes the tradeoff between gain, speed and power consumption. Unfortunately, traditional BSIM3V3 models do not characterize moderate inversion operation well. BSIM3V3 can show a 40% error in moderate inversion operation. However, the EKV 2.6 model offers more accurate modeling in moderate inversion operation [12]. The BCD-on-SOI process technology used in this work employs EKV models; hence, inversion coefficient methodology is utilized in designing the error amplifier. The fixed normalized inversion coefficient(IC), can be defined as

$$IC = \frac{I_D}{2n_0\mu_0 C_{ox}' V_T^2 \left(\frac{W}{L}\right)} \quad (3)$$

where I_D is drain current, n_0 is the sub-threshold slope factor, μ_0 is the mobility, C_{ox}' is gate oxide capacitance, V_T is the thermal voltage, W and L represents the width and the length of the transistor, respectively. Figure 4 shows the simulation result of NMOS ($W=48 \mu\text{m}$, $L = 2 \mu\text{m}$) transconductance efficiency versus. inversion coefficient from -45°C to 175°C . Figure 5 shows the simulation result of PMOS ($W = 96 \mu\text{m}$, $L = 2 \mu\text{m}$) transconductance efficiency versus. inversion coefficient from -45°C to 175°C . From Figures 4 and 5, inversion coefficient represents all regions of operation of a MOSFET: the weak inversion (WI) region represents inversion coefficient less than 0.1; the moderate inversion (MI) lies between inversion coefficient ranging 1 to 10 and the strong inversion (SI) indicates inversion coefficient greater than 10.

Figure 6 shows the schematic of a PMOS input pair folded cascode OTA. This topology has been selected as the error amplifier in this work. The PMOS input pair offers wider ICMR (Input Common-Mode Range) and empirically lower flicker noise than its NMOS counterpart [14]. By utilizing a cascode current mirror load at the output node, the folded cascode OTA has higher CMRR, PSRR and dc gain than simple Miller OTA topology. The DC voltage gain of a folded cascode OTA can be express as

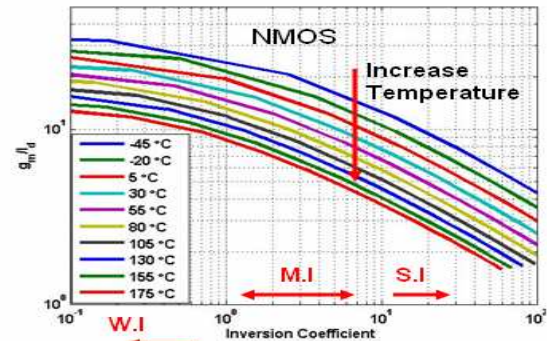


Figure 4. NMOS transconductance efficiency vs. inversion coefficient

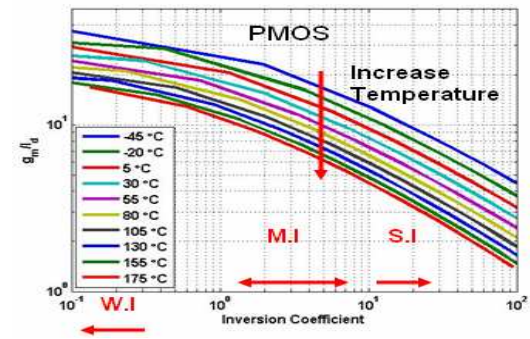


Figure 5. PMOS transconductance efficiency vs. inversion coefficient

$$A_v(T) \cong \left(\frac{g_{m_in}(T)}{I_{d_in}} \right) \cdot (V_{A_pcas}(T) // V_{A_ncas}(T)) \quad (4)$$

where subscript “in” represents the transconductance of input differential pair, V_{A_pcas} represents the early voltage of the PMOS cascode current mirror. given by

$$V_{A_pcas}(T) \cong \left(\frac{g_{m_M9}(T)}{I_{d_M9}} \right) (V_{A_M9}(T) V_{A_M11}(T)) \quad (5)$$

and V_{A_ncas} represents early voltage of NMOS cascode current mirror,

$$V_{A_ncas}(T) \cong \left(\frac{g_{m_M7}(T)}{I_{d_M7}} \right) \left(\frac{V_{A_M7}(T) V_{A_M5}(T) V_{A_M3}(T)}{2V_{A_M3}(T) + V_{A_M5}(T)} \right) \quad (6)$$

Figure 7 and Figure 8 show the transconductance efficiency versus. normalized current of the NMOS and the PMOS transistors, respectively. From these figures we can observe that the g_m/I_d parameter decreases when biasing current increases. This indicates that the devices are moving toward the strong inversion region, resulting in higher power consumption than when biased in moderate inversion. In this work, both the input pair and the cascode current mirror are both biased in the moderate inversion region to keep power consumption low at elevated temperature,. Table 1 gives the aspect ratio, the inversion coefficient and the transconductance efficiency of the amplifier at 175°C. From Table 1, all devices of OTA are operating within the moderate inversion region. Alternatively, lower power consumption can be achieved by biasing the transistors in weak inversion, but at the expense of significantly reduced bandwidth. In addition, intrinsic device voltage gain, $g_m r_o$, does not include the temperature dependent effects of g_m and r_o . By means of the inversion coefficient methodology, the temperature dependence of the voltage gain of the amplifier can be more readily understood.

Notice that the input differential pair and the cascode current mirror load do not share the same supply voltage as in a conventional folded cascode OTA. The PMOS input pair connects to the 5.6-V supply from the pre-regulator. The cascode current mirror requires higher supply voltage from the pre-regulator to increase the output voltage swing. The higher the output voltage swing, the more current can be sourced from the pass transistor. The voltage variation at output node may swing from $2V_{DS_SAT}$ to $(9V - 2V_{SD_SAT})$. HV (25-V) NDMOS (M6, M7) are needed to avoid device breakdown due to excess voltage stress on drain-source terminal (5.5 V).

Transistors M1-M5 and M8-M11 are regular MOSFET devices.

IV. TEMPERATURE STABLE CURRENT REFERENCE

A temperature stable current reference is needed for enhancing the performance of the OTA at elevated temperatures. Theoretically, the best current reference would be a constant current; if the current reference can be kept constant over temperature, the power dissipation of the OTA will be independent of temperature. In [9, 10], their regulators have quiescent current at 2.7 mA and 2 mA, respectively. The higher quiescent current would degrade the current efficiency of the voltage regulator and dissipate more heat at high temperature. This voltage regulator consumes a total of 0.6 mA quiescent current at 175°C. Approximately 20% of the quiescent current is consumed by the OTA and the temperature stable current reference, and 45% is consumed by the pass transistor of the regulator.

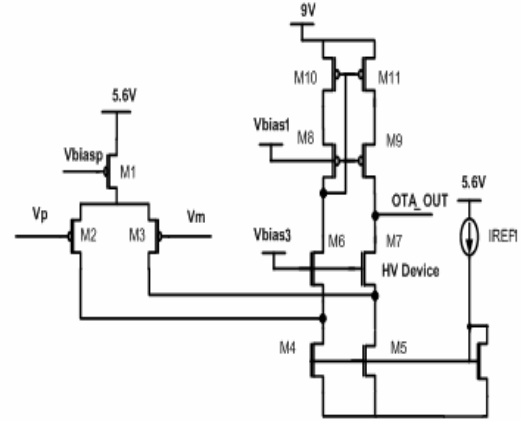


Figure 6. Folded-Cascode Amplifier

Table.1. Aspect ratio, transconductance efficiency and inversion coefficient of OTA at 175°C

Transistor	W/L (μm)	I.C	g_m/I_d
M1(PMOS)	100/2	~4.75(M.I)	~7
M2, M3(PMOS)	200/5	~3(M.I)	~6.5
M4, M5(NMOS)	48/2	~3.25(M.I)	~5
M6, M7 (HV NDMOS)	20/1.3	~5.5(M.I)	~10
M8-M11(PMOS)	96/2	~2.5(M.I)	~7

Several temperature stable current reference design topologies have been proposed and published. This work is targeted to reduce the usage of off-chip

component. High temperature off-chip passive components are more costly than typical passive components (<125°C). In addition, off-chip passive device add extra PCB real estate overhead.

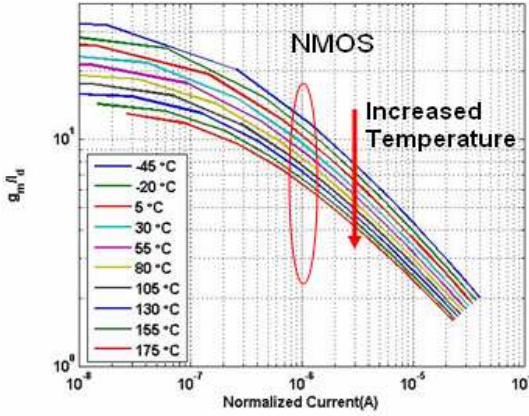


Figure 7. NMOS transconductance efficiency vs. Normalized Current

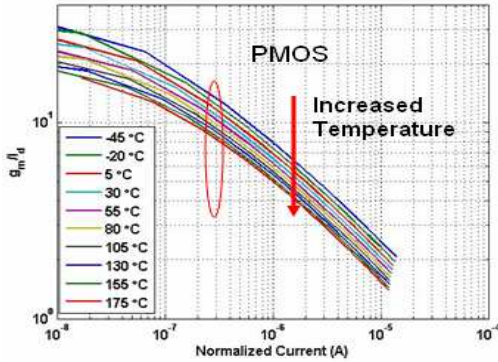


Figure 8. PMOS transconductance efficiency vs. Normalized Current

SOI process technology minimizes the leakage current and extends the operating temperature beyond 125°C. Nevertheless, the circuit design techniques need to be chosen in order to minimize the temperature coefficient of the biasing current over the wide temperature range and reduce the complexity of the design approach.

This work includes a temperature stable current reference circuit, shown in Figure 9, which uses a PTAT current and CTAT (Complementary To Absolutely Temperature) current [15]. The CTAT current can be obtained from a diode. The voltage variation with respect to temperature of a diode is $-1.2\text{mV}/^\circ\text{C}$. Summation of PTAT current and CTAT current will generate a temperature stable current. Two separate supply voltages (5.6 V and 9 V) are connected to the input differential pair of the OTA and the current mirror load, respectively. Therefore two separate temperature stable current reference

circuits are required. The lower voltage current reference (IREF1) is designed to bias the input pair of the OTA. The effective temperature coefficient of the low voltage current reference is about 75 ppm/°C. The effective temperature coefficient can be expressed as

$$TCI_{ref} = -TCR + \frac{1}{V_T \ln(N)K + V_{BE}} \left(\frac{\partial V_{BE}}{\partial T} + \frac{\partial V_T}{\partial T} \cdot 2 \cdot K \right) \quad (7)$$

Where N is the number of diode used in the PTAT leg, R_1 and R_2 represent the resistors in the PTAT and CTAT legs, respectively. The ratio of the resistor R_2/R_1 is defined as K . If the temperature coefficients of the resistors R_1 and R_2 are known theoretically by optimizing the ratio of K and N , the zero temperature coefficient temperature stable current reference can be achieved. Figure 10 shows the simulation results of the temperature stable current reference. The effective temperature coefficient of the high voltage current reference (IREF2) is just under 230 ppm/°C.

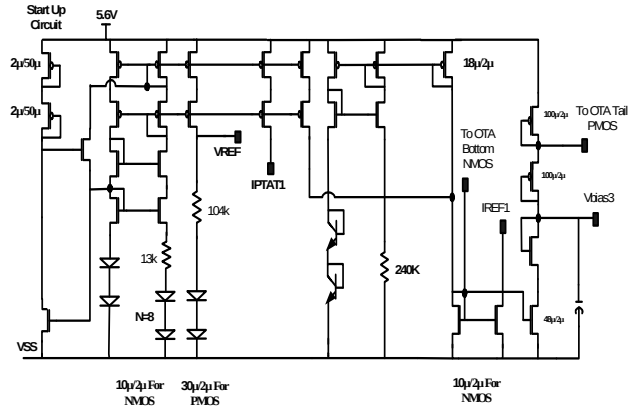


Figure 9. Schematic of Temperature stable current reference (IREF1)

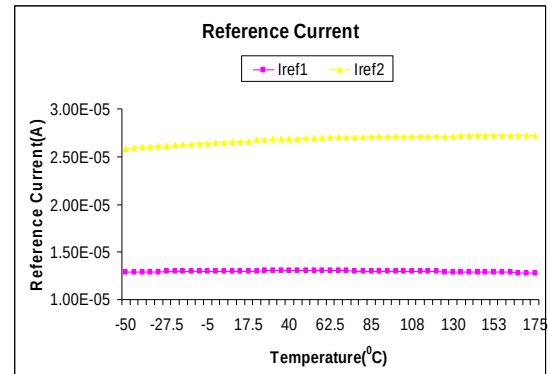


Figure 10. Temperature stable current reference (IREF1/IREF2)

V. FREQUENCY RESPONSE ANALYSIS

For linear voltage regulators, negative feedback is applied to regulate the output voltage variation

according to the load current switching; therefore, the stability of a negative feedback amplifier is a very important issue for the overall system performance. An unstable negative feedback amplifier tends to oscillate so a compensation technique is needed to guarantee stability.

The feedback loop of the regulator is intentionally broken for AC/Frequency analysis. Due to the NMOS pass transistor utilized in the design, there is no signal inversion, and a RHP zero is avoided. The pass transistor stage can be seen as a common-drain amplifier (voltage buffer) where the V_{ref} is connected to the non-inverting (positive) terminal of the PMOS folded-cascode OTA and V_{fb} is connected to the inverting (negative) terminal.

The transfer function of the system can be derived from the simplified block diagram shown in Figure.11. The complete linear voltage regulator can be broken into three stages. The first stage is the OTA stage, and the voltage gain of OTA stage is represented by

$$Av_{OTA} = g_{m_OTA} \times \left(R_{o_OTA} // \left(\frac{1}{sC_{para1}} \right) \right) \quad (8)$$

where g_{m_OTA} represents the transconductance of the OTA, R_{o_OTA} is the output resistance of the OTA, and C_{para1} is the parasitic capacitance at the output of the OTA. This parasitic capacitance and output resistance R_{o_OTA} form the pole P_1 , which can be expressed as

$$P_1 \cong \frac{1}{2\pi R_{o_OTA} C_{para1}} \quad (9)$$

The second stage is a voltage buffer stage [16], which is added for frequency compensation purposes. Without this voltage buffer, in frequency domain, the output resistance of the OTA and the parasitic capacitance (C_{gs}) of the pass transistor will create a low frequency pole which lies close to the regulator's output pole. The voltage gain of the voltage buffer is expressed as

$$Av_{buffer} = g_{m_buffer} \times \left(R_{o_buffer} // \left(\frac{1}{sC_{para2}} \right) \right) \quad (10)$$

where g_{m_buffer} represents the transconductance of the voltage buffer, R_{o_buffer} is the output resistance seen from the voltage buffer (common drain amplifier) that is equal to $(g_{m_buffer})^{-1}$, and C_{para2} is the parasitic capacitance seen at the gate terminal of the pass transistor. This parasitic capacitance is proportional to the C_{ox} of the pass transistor. Typically,

$$C_{para2} \cong \frac{2}{3} C_{ox_pass}, \text{ and } C_{para2} \cong 40 \cdot C_{para1}$$

because of the size of the pass transistor is approximately a factor of 40 times larger than the transistor of the voltage buffer. P_2 can be expressed as

$$P_2 \cong \frac{g_{m_buffer}}{2\pi C_{para2}} \cong \frac{\sqrt{2\beta_{buffer}(I_{d_buffer} + 0.02 \cdot I_{Load})}}{2\pi(40)C_{para1}} \quad (11)$$

The third stage is the pass transistor. This transistor needs to be large enough to source hundreds of milliamps during heavy loading conditions. A 45-V high voltage n-type DMOSFET is employed as the pass transistor ($W = 24,000 \mu m$, $L = 1.5 \mu m$). The drain terminal of the pass device is connected to V_{DDH} , which varies from 10 V to 30 V. The source terminal of the pass device is the output of the regulator. The voltage gain of the pass transistor stage is expressed as

$$Av_{pass} = g_{m_pass} \times \left(R_{o_pass} // (R_{f1} + R_{f2}) // R_{load} // (R_{esr} + \frac{1}{sC_{out}}) \right) \quad (12)$$

where g_{m_pass} represents the transconductance of the pass transistor, R_{o_pass} is the output resistance looking into the source terminal of the pass device, R_{f1} and R_{f2} is the feedback resistor, R_{esr} is the electrical series resistance of the output capacitor C_{out} , and C_{out} represents the output capacitor. Resistance R_{load} is a function of the loading condition (heavy/light load) and the equation contains one pole P_{out} and one zero Z_{esr} . Therefore, the regulator system contains 3 poles and one zero.

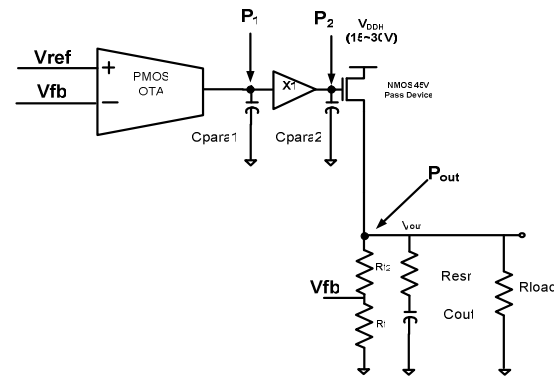


Figure 11. Simplified block diagram for AC/Frequency analysis

A. POLE SWAP TECHNIQUE

From Figure.11. The location of pole P_1 lies at the output of the OTA. The frequency of P_1 is approximately at 3 KHz. When the regulator is

operating at a heavy loading condition (~ 100 mA), P_1 is the dominant pole and P_{out} is the second pole inside the unity gain frequency. Figure 12(a) illustrates the pole and zero locations when the regulator is in a heavy loading condition. Z_{esr} compensates P_{out} , resulting in a phase margin increase and pole P_2 is proportionally to load current, pushing P_2 outside of the unity gain frequency.

When the regulator is operating at a light loading condition (about 50 μ A), P_{out} becomes the dominant pole because P_{out} is proportional to load current. As a result, P_{out} is located at a low frequency (~ 80 Hz) and P_1 (3 KHz) becomes the second pole inside the unity gain frequency (see Figure 12(b)). When Z_{esr} compensates for P_1 , the unity gain bandwidth under light loading conditions moves down to approximately 70 KHz. This pole swap technique will enhance transient response time (extended closed loop bandwidth) due to the dominant pole not being fixed at a certain frequency. As the load current magnitude increases, the unity gain bandwidth becomes wider. The large output capacitor can also help to reduce the voltage droop during load current switching. In addition, an increase in the value of output capacitor and its ESR can also enhance the stability of the regulator by moving P_{out} and Z_{esr} to a lower frequency (Z_{esr} moves closer to P_1). AC simulation (Bode Plot) of light / heavy loading conditions across temperature needs to be performed to ensure that the system is stable. Figure 13 shows the phase margin (PM) of the high temperature linear voltage regulator as a function of load current. The PM increases with increased temperature during heavy loading conditions.

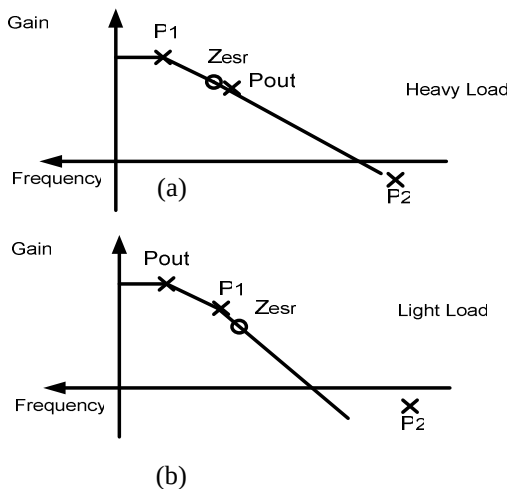


Figure 12. (a) Pole and Zero location during heavily load (b) Pole and zero location during light load

VI. LAYOUT AND SIMULATION RESULTS

Figure 14 shows the layout of the high temperature linear voltage regulator. The core area of the voltage regulator is 3.24 mm^2 ($1,800 \mu\text{m} \times 1,800 \mu\text{m}$). To alleviate electron migration at high temperatures, metal interconnections were drawn 1.5X wider than the foundry's design rules required. Each individual sub block is surrounded by trench and the chip was packaged in Kyocera DIP40 ceramic package.

Figure 15 shows the simulation result of the high temperature linear voltage regulator that supplies 5.3V rail to the gate-drive circuit at 175°C . The low-side buffer draws 125 mA dynamic current.

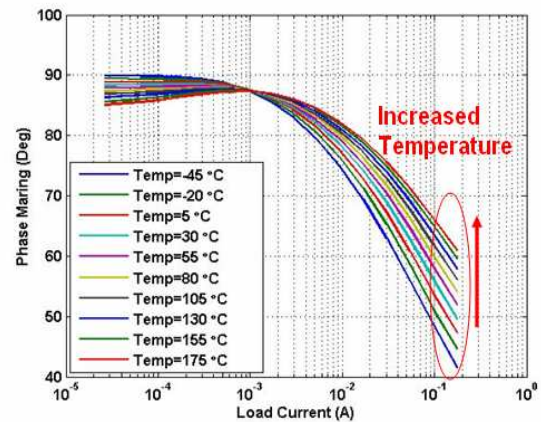


Figure 13. Phase Margin as function of load current

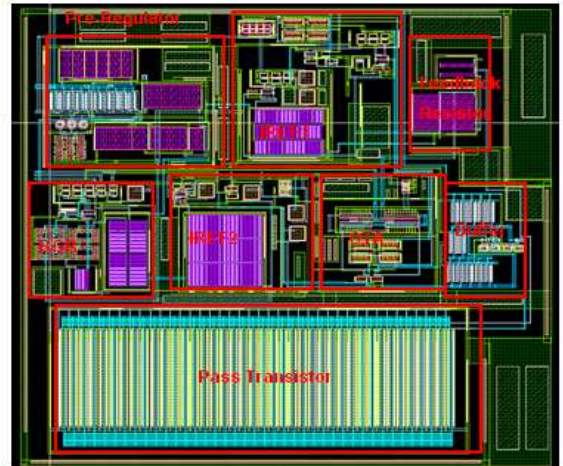


Figure 14. Layout of high temperature linear voltage regulator

VII. CONCLUSIONS

A high-temperature and high-voltage linear voltage regulator chip has been designed and fabricated. A detail description of the high temperature design techniques and the

implementation of the high temperature/voltage linear voltage regulator in BCD-on-SOI process are presented in this paper. This high temperature/voltage linear voltage regulator provides a 5.3 V rail to the low-side buffer of gate-drive circuit [2]. The voltage regulator consumes a total of 0.6 mA quiescent current during zero load current condition at 175°C, the lower quiescent current can improve the efficiencies of both the regulator and the gate-driver. The pole swap techniques proposed in this work can extend the range of the system stability to 4 decades of the load current (tens of μA to 200 mA) variations, this is especially important in this research since the worst case load current profile is an impulse current waveform, see Figure 15. This current impulse comes from the switching "on" transition of the low-side buffer of the gate driver; the peak-to-peak current of this current impulse may reach 200 mA in only 10 ns. In addition, a temperature stable current reference stabilizes the gain of the OTA across temperature; line regulation of the voltage regulator is also preserved.

This voltage regulator circuit can be integrated with the gate driver ICs that are required inside the power converter modules of a HEV. The voltage regulator can also be utilized in other high temperature electronics (i.e. sensors, data converters, and oscillators) where typical bulk-CMOS regulators can not provide regulated output voltage beyond 125°C.

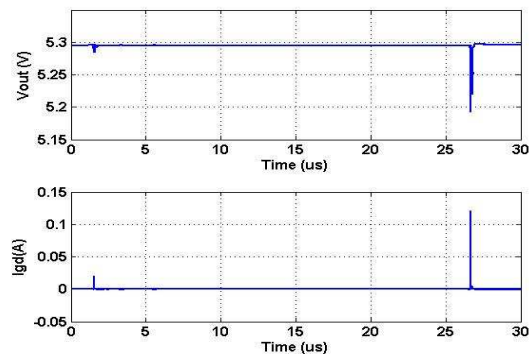


Figure 15. Simulation of high temperature linear voltage regulator at 175°C

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