Silicon-on-Insulator Based High-Temperature Electronics for Automotive Applications

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***Abstract*- In recent years increasing demand for hybrid electric vehicle has generated the need for reliable and low-cost high-temperature electronics which can operate at the extreme temperatures that exists under the hood. A high-voltage and high-temperature gate-driver integrated circuit for SiC FET switches is designed and implemented in a 0.8-micron Silicon-on-Insulator high-voltage process. First prototype chip has been successfully tested up to 200ºC ambient temperature without any heat sink or cooling mechanism. This gate-driver chip is intended to drive SiC power FETs of the DC-DC converters in a hybrid electric vehicle. The converter modules along with the gate-driver chip will be placed very close to the engine where the temperature can reach up to 175ºC. Successful operation of the chip at this temperature with or without minimal heat sink and without liquid cooling will help achieve greater power-to-volume as well as power-to-weight ratios for the power electronics module. A second prototype has also been designed with more robust features.**

I. INTRODUCTION

Fuel cell vehicles (FCV) are widely considered to be the future replacement of the internal combustion engine vehicles (ICEV). This replacement could save 60% of the primary energy consumption, and can reduce the CO_2 emission by 55% [1]. But FCVs are not yet in a position to challenge ICE for performance, cost, fuel storage, and large scale manufacturability [1]. On the other hand hybrid electric vehicles (HEV) are gaining more attention for their better performance and fuel economy compared to ICEVs. HEVs are attracting significant investment of effort and time from the auto manufacturers and researchers, for their successful commercialization. Transition from ICEV to HEV means switching from mechanical and hydraulic systems to electromechanical systems.

A typical arrangement of a hybrid fuel cell vehicle is shown in Fig. 1 [2]. Developments in hybrid automobile industry have generated an enormous need for different power electronic modules (such as DC/DC converters and DC/AC inverters) capable of working at elevated temperatures. Integration of power converters and smart power devices into the drive train requires semiconductor devices capable of working at 175°C to 200°C [3]. In 1977 the average electronics per automotive was of worth $110 [4], whereas in 2003 this figure jumped to $1510 in spite of the price reduction in the semiconductor manufacturing [5]. Applications of high-temperature electronics in automotive systems will continue to grow with their increased availability and reduction in price. It is predicted that by 2013 each automotive will contain on the average $2285 worth of electronics within its frame [5].

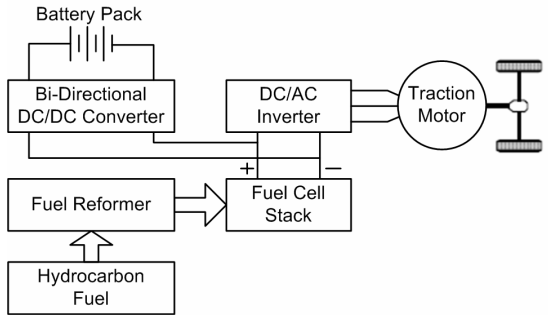

Fig. 1. Typical topological arrangement of a hybrid fuel cell vehicle drive train [2].

A summary of high-temperature automotive electronics requirement published by DaimlerChrysler, Eaton Corporation, and Auburn University is reproduced in Table I [6]. For most part of the cavity under the hood the temperature is more than 150°C. Typically the junction temperatures for integrated circuits are 10°C to 15°C higher than the ambient temperature. For power devices this can even reach 25°C above the ambient temperature. Hence electronics used in automotive especially those placed close to the engine need to be able to work at temperatures above 175°C.

The alternatives to high-temperature devices are thermal management systems which add weight and volume resulting in reduced power-to-volume and power-to-weight ratios. These thermal management approaches introduce additional overhead that can negatively offset the desired benefits of the electronics relative to the overall system operation. The additional overhead in the form of longer wires, extra connectors, and/or cooling system can add undesired size and weight to the system, as well as increased potential for failure [7]. By removing the heat sink and long interconnects, order of magnitude savings in overall mass and volume of the power

TABLE I

AUTOMOTIVE MAXIMUM TEMPERATURE RANGES [6]

On-Engine	150-200°C
In-Transmission	150-200°C
On Wheel-ABS sensors	150-250°C
Cylinder pressure	200-300°C
Exhaust sensing	Up to 850°C, ambient 300°C

electronic modules can be achieved

This work presents a Silicon-On-Insulator (SOI-) based high-temperature gate driver integrated circuit for automotive applications. In all power electronic circuitries, a gate driver is an essential component for controlling the turning "on" and "off" of the power switches. In HEVs or FCVs power converter modules along with the drivers are required to be placed in close proximity to the engine to reduce the cabling length. Hence, the ambient temperature of the gate-driver IC will be more than 150°C. The first gate driver that we designed and fabricated has been successfully tested with a SiC power MOSFET at 20 kHz and up to 200°C without heat sink and cooling mechanism [8]. A second version of the circuit has also been designed for improved reliability and performance. New circuitry has been added to make the gate driver robust and the only external component (bootstrap capacitor) in the first design was made on chip to make it fully integrated. A temperature compensated on-chip voltage regulator has also been included in the new design to minimize the number of required external voltage sources. Simulation results and some initial test results for this new design have been presented in this paper.

II. High Temperature Semiconductor Devices And Process

It is well understood that semiconductor based electronic circuit that can operate at ambient temperature higher than 150°C without external cooling and without or minimal heat sink could greatly benefit a variety of important applications, especially in the automotive, aerospace and energy production industries. But the maximum rated ambient temperature for most bulk silicon based integrated circuits is 85°C [3]. Si-based devices rated for military and automotive applications are marked for only 125°C.

Wide band gap semiconductors because of their larger energy bandgap are capable of electronic functionality at much higher temperatures than silicon. In future, wide band gap semiconductors will be the primary choice for simultaneous realization of high-power and high-temperature applications which cannot be met by much more readily available semiconductor technologies. Silicon Carbide (SiC) - and III-nitride (mainly Gallium Nitride)-based devices are the most widely researched wide bandgap semiconductors to date. SiC device crystals have traditionally have orders of magnitude fewer crystal dislocation defects than GaN [9]. Hence for realization of power switches for high-temperature applications, SiC is considered to be the material of choice. SiC-based devices are expected to be able to operate up to 600°C. However, SiC-based power switches are not yet commercially available. In addition, SiC-based integrated circuit design process will take even longer time to be commercially available.

Silicon MOSFET with reduced leakage current for higher temperature operation is realized with the Silicon-on-Insulator (SOI) structure as shown in Fig. 2. In high-temperature

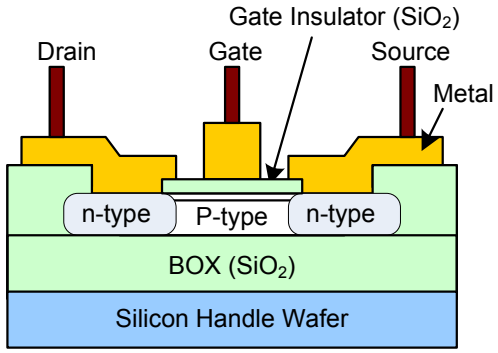

Fig. 2. Conceptual cross section of an n-channel SOI MOSFET.

electronics, junction leakage is a major concern. Bulk CMOS processes suffer from significant leakage current that contributes to higher junction temperature compared to the ambient. Buried insulator layer in SOI structure greatly decreases the leakage path associated with the drain and the source p-n junction diodes, which enables higher temperature operation. The presence of the buried oxide also reduces off-state source-to-drain carrier emission leakage that physically occurs deeper in the p-type substrate of bulk MOSFETs. The threshold voltage variation with temperature is smaller in SOI devices than in bulk devices [10]. SOI also provides improved latch-up immunity, which ultimately increases the reliability of the circuit operation at higher temperature [11]. These make SOI-based circuits capable of operating successfully in the 200°C-300°C temperature range which is well above the range of conventional bulk silicon-based devices. For our work a process that combines the advantage of high-voltage devices with SOI technology was chosen for the design and implementation of the high-temperature gate driver circuit.

III. High-Temperature Gate-Driver Circuit

For FET-based power switches, a number of gate-driver circuit topologies have been proposed in the literature [12]-[15]. Among these only the circuit reported in [15] is capable of operating at a junction temperature up to 200ºC, while others can work only up to 125°C. The authors of [16] have presented a low-loss high-frequency half-bridge gate driver circuit on SOI for driving MOSFET switches. However, there is no mention of the temperature capability of the circuit. In this work, a similar circuit topology has been used with necessary modifications as required for high temperature operation and suitable drive signal generation for the SiC FET switches under consideration.

A simplified schematic of the second prototype gate driver circuit topology implemented in this work is shown in Fig. 3. The half-bridge output stage (comprising of M_1 and M_2) connects the output terminal to one of the two supply rail voltages. The key factors that need to be considered when choosing the half-bridge topology are reverse breakdown voltage, *on*-resistance and switching speed. The topology used in this circuit consists of two NMOS transistors stacked

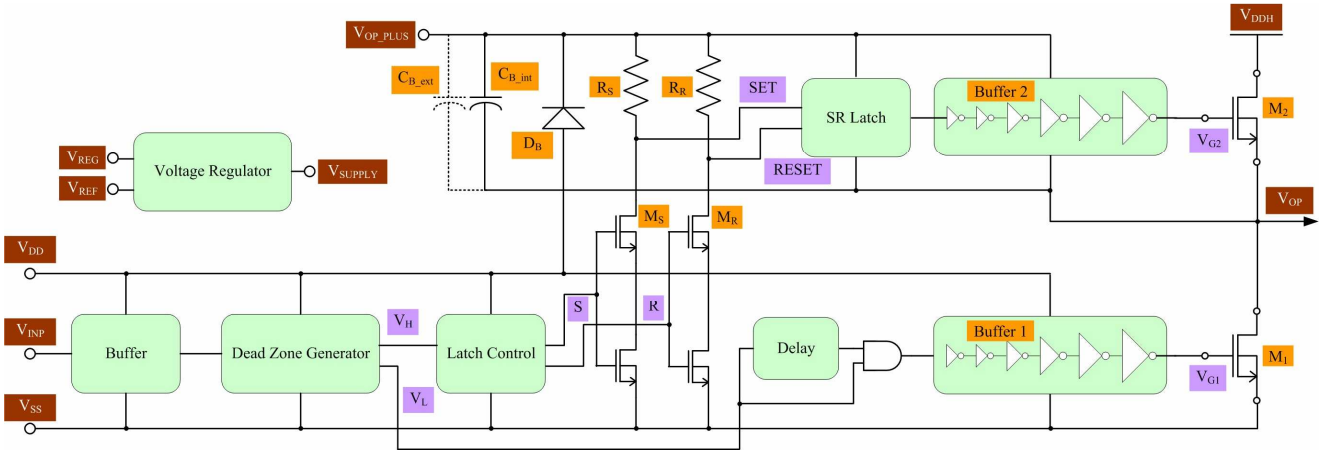

Fig. 3. Simplified schematic of the high-temperature gate driver circuit.

together. NMOS transistor has lower *on*-resistance and higher switching speed compared to its PMOS counterpart.

High voltage n-type DMOSs are used to get larger output voltage swing (up to 45 V). These transistors need to switch fast to minimize switching losses. Gate voltages of these NMOSs are designed to ensure that they do not turn on at the same time. Compared to our first iteration in the new design additional circuitry (dead zone generator and delay) are added to ensure that the NMOS transistors in the output stage are never turned on at the same time to avoid leakage path through them.

To generate a voltage above the highest rail voltage, bootstrap capacitor based charge pump circuit is used [16], [17]. This bootstrap circuit, consists of a diode (D_B) and bootstrap capacitor (C_B), supplies a voltage level higher than the highest rail voltage available (V_{DDH}). This is required for the high-side buffer, the SR latch, and the level shifter in order to generate the required gate signal for the M_2 transistor. The nodes V_{OP} and $V_{OP\text{-}PLUS}$ act as the floating ground and as the positive supply rail for the high-side circuitry, respectively. In this design the bootstrap capacitor (1.25 nF) is included on-chip. Provisions are also kept for adding additional external capacitors. Inclusion of the on-chip capacitor resolves the problem of finding appropriate high temperature off-chip capacitors required for the design of this gate driver circuit.

The new dead zone generator block added in this prototype generates two non-overlapping complementary copies (V_H and V_L) of the buffered input signal which are then further processed to generate appropriate gate signals for the NMOS transistors in the output stage. Latch control circuit takes V_H as its input and generates two pulse trains (S and R), one at the rising edge of V_H and one at its falling edge. The pulse trains in S and R signals have durations of only 10 ns to ensure minimum current flow through the R_s and R_R resistors as shown in Fig. 3.

These S and R signals alternately turns “on” and “off” the M_S and M_R high voltage NMOSs to allow flow of current through the R_S and R_R resistors for very short duration of time to minimize the power consumption of the driver circuit. Flow of current through these resistors causes a voltage drop across them which acts as the ‘SET’ and ‘RESET’ signals. The SR latch used here is an active-low latch which is controlled by the ‘SET’ and ‘RESET’ signals. This latch output is used to generate the high side gate signal V_{G2}. The V_L output of the dead zone generator is further processed by the delay circuit combined with the AND gate to make necessary timing adjustment in V_L. This adjustment is needed for unequal delay associated with the circuits generating the high-side and low-side gate signals from V_H and V_L.

Both transistors of the half-bridge stage are comprised of a large number of parallel-connected high voltage DMOS devices. Hence, these transistors have large gate capacitance, requiring large transient currents to drive them. To meet this requirement, multi-stage buffers with gradually increasing sizes (exponential horn) are added to drive the high- and low-side transistors.

An important failure mechanism that becomes more prominent at elevated temperature is electromigration. In this process current flow over time gradually displaces microscopic metal traces on an interconnect, eventually leading to failure [18]. To alleviate this problem all the metal interconnects were made oversized to reduce the current density through them. Multiple pad connections are used for the power supply and output nodes to minimize the parasitic bond wire inductance.

IV. On Chip High Temperature Voltage Regulator

An on-chip voltage regulator capable of generating fairly constant voltage over a wide temperature range (-50°C to 200°C) has been added in the new design to generate the low biasing voltage (V_{DD}) from the larger supply voltage (V_{DDH}). High voltage supply to the chip (V_{DDH}) can be any voltage between 15 V to 30 V depending on the required gate signal of the SiC power switch that this gate driver circuit will drive. Hence the major challenge for this design was to handle this wide input voltage variation at such high voltage level. A simplified schematic of the voltage regulator (low-dropout type) topology used in this work is shown in Fig. 4. This circuit has two distinct building blocks. The first block is a bandgap

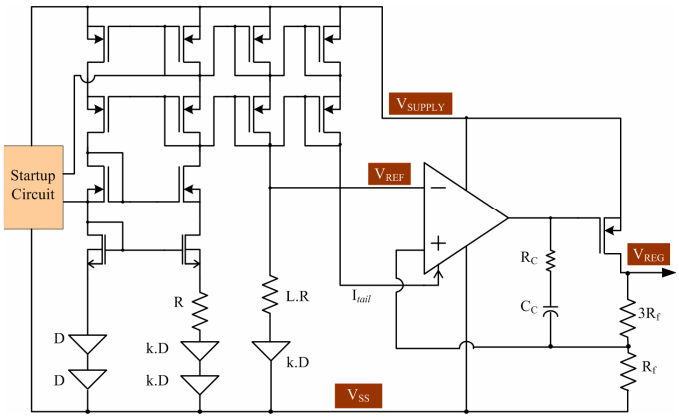

Fig. 4. On chip voltage regulator circuit schematic.

reference (BGR) circuit which generates a constant reference voltage over wide temperature variation. The second block is an error amplifier. A simple single stage differential pair has been used to keep the power consumption at low level. A RC compensation circuit was added for improving the phase margin of the regulator circuit. A Temperature insensitive constant voltage generated by the bandgap reference (BGR) circuit is used as the reference voltage for the differential pair amplifier. We have used stacked diode in the BGR circuit to get better matching of these devices. Temperature coefficient (TC) of the bandgap reference is set to zero by proper compensation of positive TC of the thermal voltage with the negative TC of the diode forward voltage in the circuit. Simulation shows that at any fixed temperature the voltage variation in response to input voltage variation form 15 V to 30 V is less then 200 mV. With any fixed supply voltage this variation is less than 110 mV for temperature variation from -50°C to 200°C. Simulations were also conducted with the voltage regulator providing the biasing voltage (V_{DD}) to the gate driver circuit. The power consumption of the regulator circuit with the temperature variation and for different V_{DDH} is shown in Fig. 5. The maximum power consumption by the regulator circuit for 30 V input signal at 175°C is 18 mW.

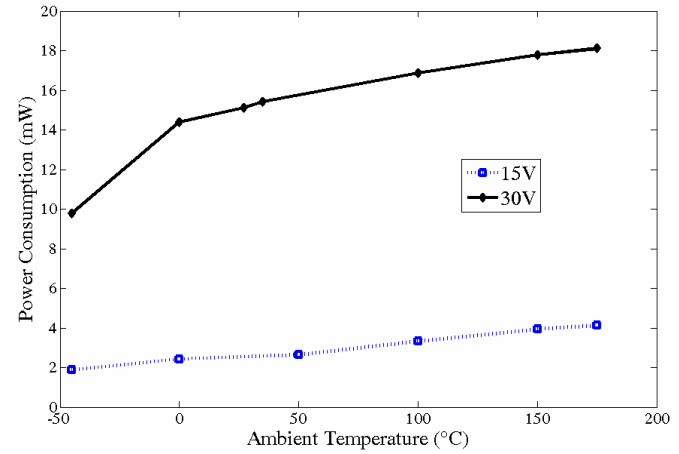

Fig. 5. Power consumption of the regulator circuit with the variation of the temperature (up to 175°C) for supply voltage of 15 V and 30 V.

V. Simulation Results

For the new design, schematic level simulations were performed over temperature from −40°C up to 175°C. The circuit was simulated with a capacitive load of 10 nF in series with 10 Ω resistance to resemble the load condition (gate of SiC FET power switches). Fig. 6 shows the output current provided to the capacitive load along with the current flowing through the M_2 and M_1 transistors. Simulation result shows that a current through only one of these two transistors at any particular time, which flows only during the switching instances. This ensures complementary turn “on” and “off” of the half-bridge stage transistors. This will also reduce the power dissipation through these devices and keep the junction temperature closer to the ambient temperature.

VI. Measurement Results

Fig. 7 shows the micro-photograph of the first prototype in comparison with a dime. Gate driver circuit occupies a die area of 3.6 mm^2 (2,240 µm × 1,600 µm) including the pads and the ESD protection circuits. The two high-voltage NMOS devices of the half-bridge output stage occupy a major portion of the chip area. They are sized (W/L = 24000 µm/1.6 µm) to provide large peak current as needed to obtain acceptable rise and fall times. Each of these NMOS transistors is comprised of six hundred 45 V NMOS devices (W = 40 µm) connected in parallel. The high-voltage devices are well isolated from the low-voltage devices through a thick dielectric layer. The layout of the high-voltage devices resembles a “race-track” structure [19].

The chip was bonded in ceramic package which is capable of operating above 200ºC. Test boards made of polyimide material are used for high temperature testing of the prototype chip. High temperature solder and wires with Teflon jacket are used for reliable testing of the chip at or above 200°c. Fig. 8 shows one of these test boards.

The first prototype gate driver circuit was tested at different temperatures while driving a 1200 V, 10 A SiC MOSFET. Test board was placed inside an environmental chamber and

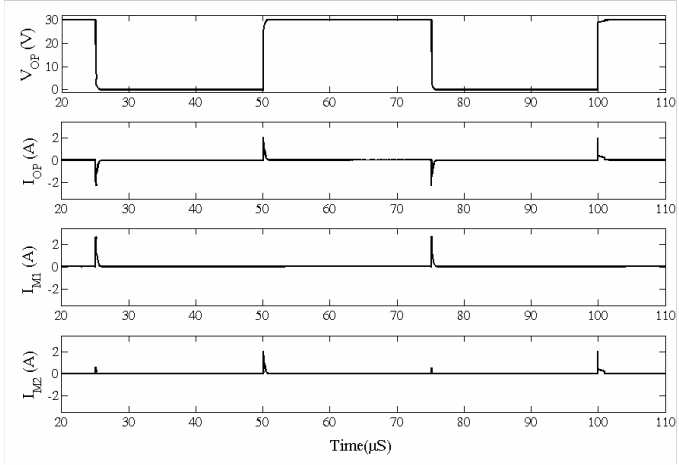

Fig. 6. Output voltage and current supplied by the driver circuit and currents through M_2 and M_1 MOSFETs in the half bridge output stage.

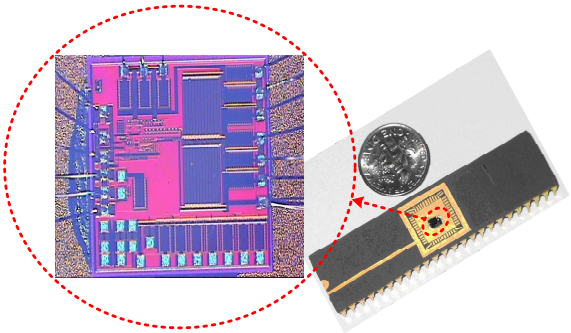

Fig. 7. Micrograph of the gate driver circuit (first prototype) showing the size of the die compared with a dime.

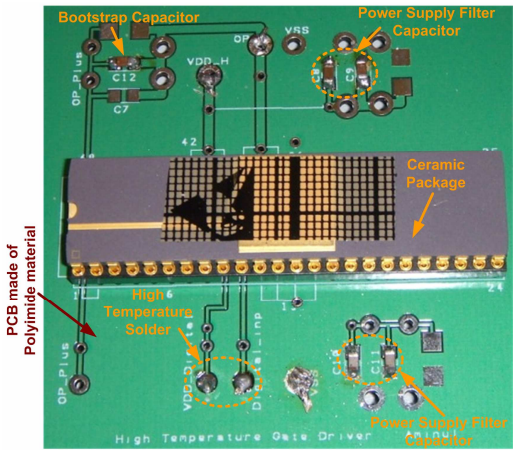

Fig. 8. High temperature test board used to test the prototype circuit up to 200°C.

temperature was raised from room temperature to 200°C. Fig. 9 shows the logic level input signal (blue) to the chip, gate signal generated by the prototype circuit (red), and load voltage at the drain terminal of the SiC MOSFET (green) at 200°C. The SiC MOFET was carrying 5 A peak current while turned on by the driver circuit. At 200°C the rise-time and fall-time were observed to be 107 ns and 162 ns respectively. In the second prototype driving capability has been further increase to reduce these switching times. Until now we have tested the second generation of the gate driver circuit up to 190°C with more reliable performance compared to the first generation. The voltage regulator added in this version has also been successfully tested up to 150°C with switching current load. Fig. 10 shows the regulator output with 15 V and 30 V input signal at different temperatures. For 30 V input signal the temperature coefficient of the regulator output voltage was observed to be 525 ppm/°C. Inset in Fig. 10 shows the reference voltage generated by the bandgap reference circuit for 15 V and 30 V input signal. A 80 mV variation was observed for ambient temperature change of 125°C.

VII. Conclusions

For high temperature applications where conventional silicon-based devices failed to deliver optimum performance, wide bandgap materials especially SiC presents itself as the best option. For efficient and effective integration of wide bandgap power devices into the power electronic modules, SOI-based integrated circuits are needed to interface them with the control units. The high-temperature and high-voltage gate-driver circuit presented in this paper is part of a research effort to design a heat-sink-less DC-DC converter module for hybrid electric vehicles that can be placed close to the engine. The performance of the first prototype looks promising. Simulation results and initial tests of the second prototype show better reliability and improved performance compared to the first one. Test results of the second version will be presented in future publications.

Acknowledgment

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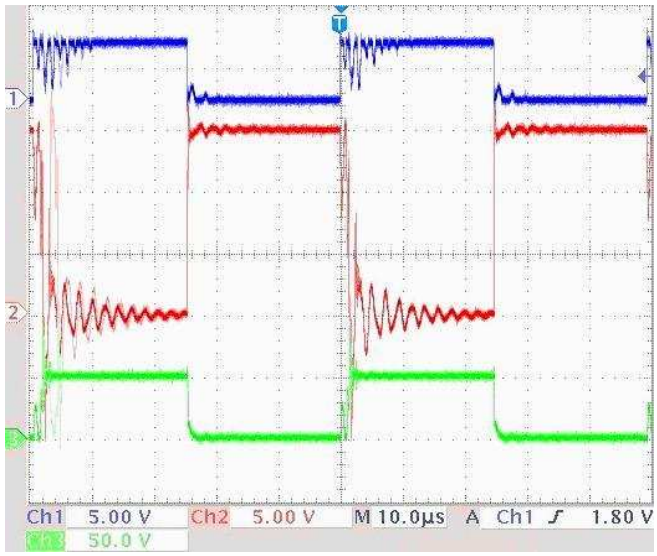

Fig. 9. Logic level input signal (blue), gate signal generated by the circuit (red), and load voltage at the drain terminal of the SiC MOSFET (green) at 200°C ambient temperature without heat sink and any cooling mechanism.

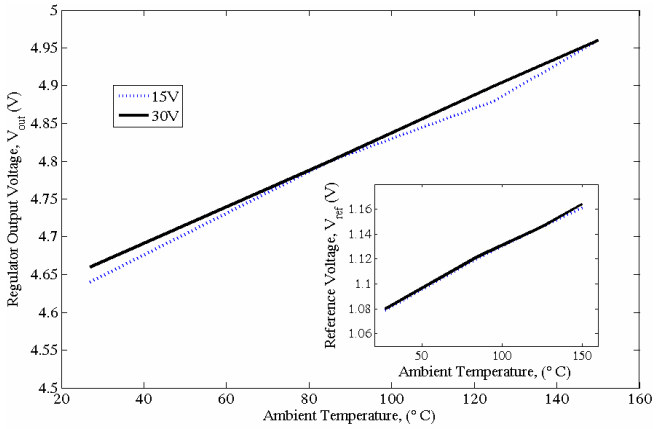

Fig. 10. Regulator output in response to supply voltage variation at different temperatures.

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