

# Design and Characterization of a Three-Phase Multichip SiC JFET Module

Fan Xu\*  
[fxu6@utk.edu](mailto:fxu6@utk.edu)

Jing Wang\*  
[jwang50@utk.edu](mailto:jwang50@utk.edu)

Dong Jiang\*  
[djiang4@utk.edu](mailto:djiang4@utk.edu)

Fred Wang\*  
[fred.wang@utk.edu](mailto:fred.wang@utk.edu)

Leon Tolbert\*  
[tolbert@utk.edu](mailto:tolbert@utk.edu)

Timothy J. Hant†  
[jghan@gpe-energy.com](mailto:jghan@gpe-energy.com)

Fred Flett††  
[jentec@designee.net](mailto:jentec@designee.net)

\* Department of Electrical Engineering and Computer Science, The University of Tennessee, USA

† Global Power Electronics, USA

## Abstract

Global Power Electronics (GPE) has developed a SiC JFET based, 200°C, 50 kW three-phase inverter module. This paper evaluates the electrical performance of the module, especially, its switching performance, considering the device characteristics, the package parasitics, and gate drive circuit. Using Maxwell Q3D parameter extractor and Saber circuit simulator, a detailed circuit simulation was conducted. The results show that the switching speed is constrained by the intrinsic behaviour of the SiC JFET, in order to avoid phase-leg shoot-through and excessive gate-source voltage during the fast device turning on and off. Switching performances are aggravated by the package parasitics and their differences for paralleled JFETs. The key parasitics include gate-loop inductance, DC bus inductance, and common source inductance. By proper layout design, such as by separating gate pins, the gate-loop parasitics can be reduced. A gate driver design with selected gate resistance, paralleled gate-source capacitance, and an RCD network is used to demonstrate the improved performance. The module is verified to have low loss, fast switching characteristics under 650 V, 60 A, 200 °C in simulation and 150 °C in experiments.

## 1. Introduction

SiC power semiconductors have been expected to replace conventional Si-based power switching devices owing to their attractive properties such as high breakdown voltage, fast switching, low power losses, and high temperature. Their advanced properties allow them to be used for the power systems need high density, high coolant temperature, and high efficiency applications.

Global Power Electronics (GPE) and its partners have been developed full SiC power modules and three phase inverters [1-2]. In this paper, we present a 200°C, 50 kW three-phase inverter module which is designed for use in switching applications such as AC motor control, motion/servo control, UPS, and photovoltaic systems [3]. With 1200 V, 100 A rating, each switching element consists of four 4.17mm x 4.17 mm 1200 V SiC JFET with two 2.7mm x 2.7 mm anti-parallel SiC Schottky barrier diodes (SBD). All devices are from SiCED [4]. Fig. 1 shows the phase leg circuit with package parasitics (common source inductance is the parasitic inductance both in the main switching loop and the gate loop). The package layout of each phase leg is shown in Fig. 2. All switching components and interconnects are isolated from the heat sink base plate. Fig. 3 is the three-phase module structure. The JFETs used in the module have a nominal pinch-off voltage of -17 V and breakdown voltage of -25 V. The junction temperature is designed to be 200 °C.

In order to evaluate the module switching performance, a double pulse test is conducted both in simulation and experiment for rated DC voltage of 650 V and current of 60 A. Three items are investigated in this paper: 1) turn-on and turn-off speed limitations; 2) impact of package parasitics; 3) impact of gate drive.

## 2. Electrical Performance of the SiC JFET Module

In this section, the electrical performance of the SiC JFET module, especially, its switching performance will be evaluated. The evaluation will consider the device characteristics, the package parasitics, and gate drive circuit.

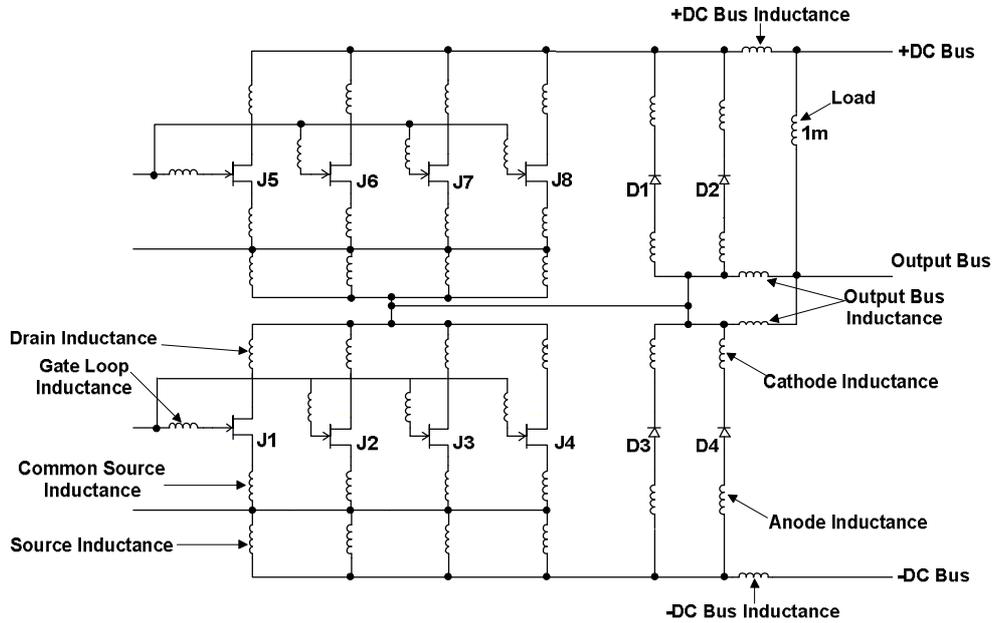


Fig. 1. Single phase-leg circuit with package parasitics.

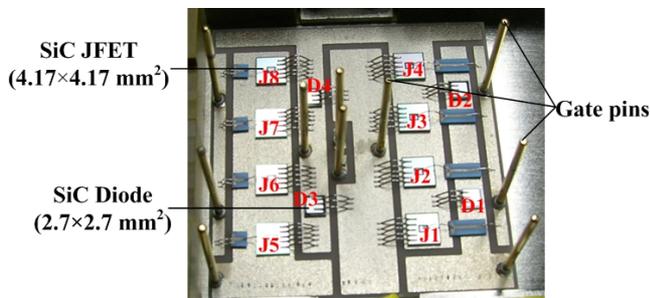


Fig. 2. Phase-leg of the SiC based inverter module.

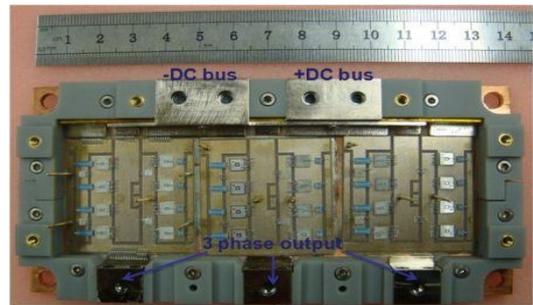


Fig. 3. Module inside structure.

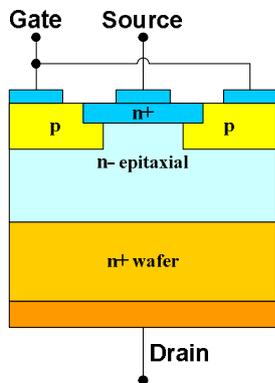


Fig. 4. Vertical structure of JFET.

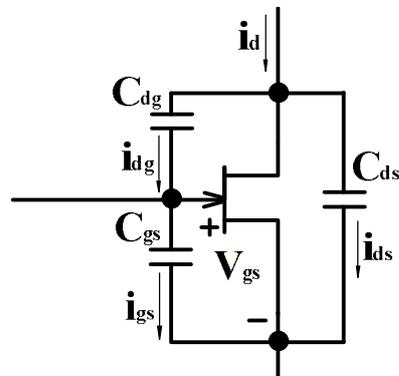


Fig. 5. JFET intrinsic capacitors.

## 2.1. JFET Inside Capacitor

Fig. 4 shows the structure of the SiC JFET. This structure leads to the existence of intrinsic capacitors between device terminals, as shown in the circuit in Fig. 5.

These JFET intrinsic capacitors are a crucial factor in determining the switching speed. For a normally-on JFET, the capacitor  $C_{gs}$  is charged during turn-on transient, and the device will be turned on after the voltage across  $C_{gs}$  exceeds the pinch-off voltage. During turn-off transient,  $C_{gs}$  will discharge to reduce  $V_{gs}$  and the device will be turned off.

The JFET drain and source terminal voltages are changed when other switches are turning on and off. That will charge or discharge JFET inside capacitors due to  $dV/dt$ . As a result,  $V_{gs}$  is changed, which may result in avalanche ( $V_{gs}$  exceeding JFET breakdown voltage) or shoot-through (both high side and low side switches being turned on at the same time). The method to avoid avalanche or shoot-through is to slow down the switching speed to reduce  $dV/dt$ , which will lead to longer switching time and higher switching loss.

## 2.2. Package Parasitics

The package parasitics also impact switching transients. The common source inductance serves as a negative feedback from the main switching loop to the gate loop, as the voltage drop across it counteracts the change of the gate voltage ( $V_{gs}$ ), thus slowing down the switching speed [5-7]. Besides, drain inductance introduces oscillations in  $V_{gs}$ ,  $V_{ds}$ , and drain current ( $I_d$ ) waveforms which will increase switching loss [5].

On the other hand, voltage across the gate loop (gate pins, direct bond copper (DBC), wirebonds connecting gate pads on JFET dies to DBC) and DC bus inductances are also major causes for  $V_{gs}$  to exceed pinch-off voltage.

During low side JFET turning on, the voltage of phase-leg output terminal drops from high voltage to 0 V, and charging current of JFET inside capacitors causes current  $i_g$  appearing in high side JFET's gate loop. Since  $V_{gs} = V_s - V_L$  and  $V_L = L \cdot (di_g/dt)$ , it is possible that  $V_{gs}$  exceeds pinch-off voltage and high side JFET is turned on too (shoot-through), as Fig. 6 shows. Small  $L$  will lead to small  $V_L$  and may help to avoid shoot-through. For 4 paralleled JFETs, the gate loop inductances are 36, 27, 27, 36 nH respectively if only one gate pin is put in the middle of 4 JFETs. Longer distance from gate pin to farthest JFETs leads to larger inductance in their gate loops. However, if two properly spaced gate pins are used, the gate loop inductances will all be balanced and reduced to be 27 nH.

In addition, the JFET inside capacitors are charged by DC voltage through the DC bus, which causes voltage across the DC bus parasitic inductance, as Fig. 7 shows.  $V_{bus}$  makes the high side JFET drain side voltage higher than the DC voltage. Gate voltage will increase too, and shoot-through may happen. As a result, the switching transient needs to be slowed down in order to avoid shoot-through which in turn results in longer switching time and higher switching loss. By reducing the width of DC bus from 520 mil to 130 mil, the bus inductance will be reduced by 5 nH. The reduction of parasitic inductances results in faster switching and less switching loss.

## 2.3. Gate Drive

The turn-off and turn-on external gate resistances ( $R_g$ ) are 2  $\Omega$  and 20  $\Omega$  respectively for each JFET. Fig. 8 shows the bottom 4 JFETs drain currents during the turn-on transient. The 4 paralleled JFETs drain currents are not balanced due to the parameter variation of each JFET and different package parasitics in each JFET loop (drain side, source side and gate drive parasitics of each JFET). The current unbalance will lead to power loss and corresponding thermal stress difference for paralleled JFETs [8]. To balance the current, different turn-on resistances (24  $\Omega$ , 21  $\Omega$ , 19  $\Omega$ , 17.5  $\Omega$ ) are applied to the 4 JFETs. Fig. 9 shows the drain current waveforms after current balancing.

Moreover, in the auxiliary gate drive circuit, a 3 nF capacitor is paralleled between the gate and source of each JFET in order to increase  $C_{gs}$  to eliminate phase-leg shoot-through. An RCD network is also used to prevent JFET from breaking down which is caused by exceeding avalanche voltage [9-10].

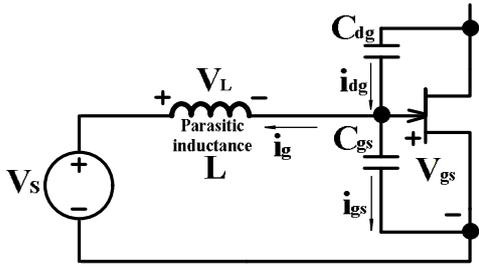


Fig. 6. Gate loop parasitic inductance.

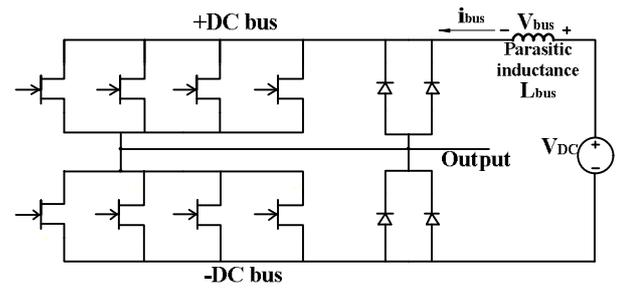


Fig. 7. Phase-leg with DC bus parasitic inductance.

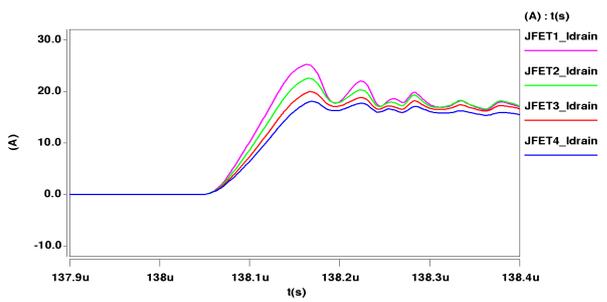


Fig. 8. Unbalanced current during turn-on using identical  $R_g$ .

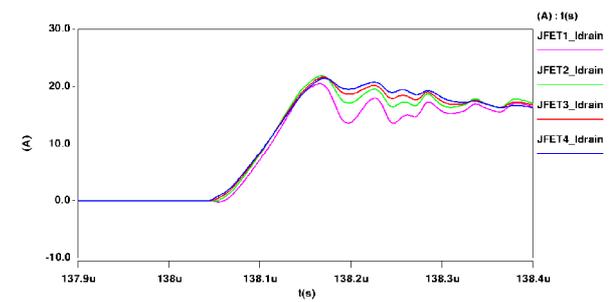


Fig. 9. Balanced current during turn-on using selected  $R_g$ .

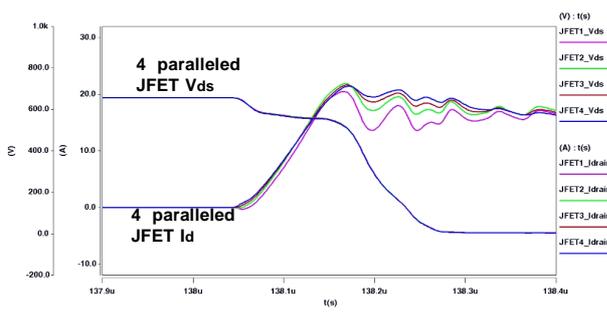


Fig. 10. Simulation turn-on waveforms at 200 °C.

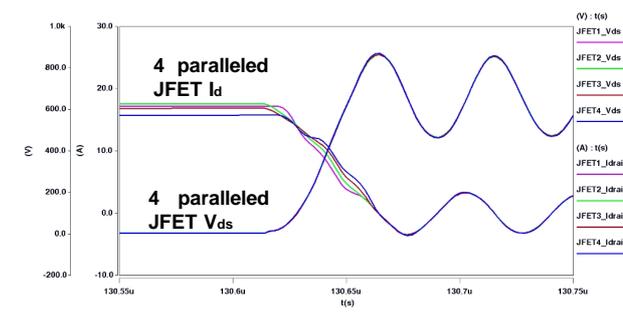


Fig. 11. Simulation turn-off waveforms at 200 °C.

## 2.4. Switching Performance

Figs. 10 and Fig. 11 respectively show the simulation waveforms of turn-on and turn-off transient using the previous described gate drive. Table 1 shows the turn-on and turn-off times and power loss.

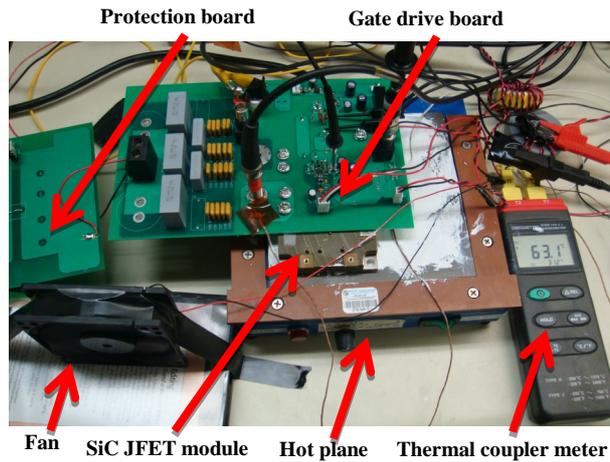
Table 1. Switching Time and Losses of the Module without Chopper Circuit

Turn-on Time	One JFET Turn-on Loss	Turn-off Time	One JFET Turn-off Loss
170 ns	1102.25 $\mu$ J	40 ns	49.75 $\mu$ J

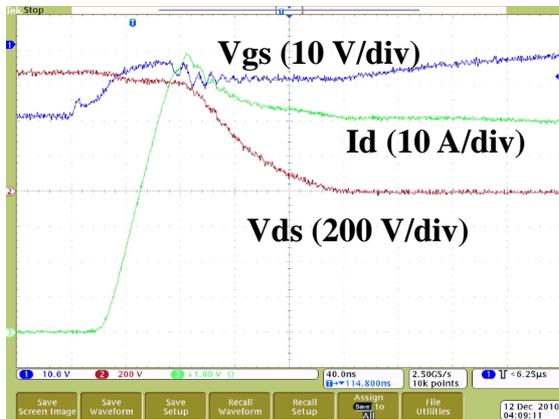
If the chopper circuit with external diodes is used with the high side JFETs, no current can flow through the high side JFETs channels and the shoot-through will not happen. Table 2 shows simulation results of switching time and power loss of the module with external chopper circuit. The turn-on and turn-off resistances are all 0  $\Omega$ . From the results, it is obvious that the module can be operated at fast switching time and low switching loss.

Table 2. Switching Time and Losses of the Module with Chopper Circuit

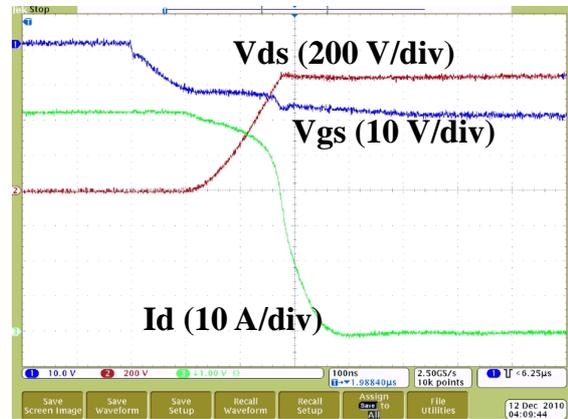
Turn-on Time	One JFET Turn-on Loss	Turn-off Time	One JFET Turn-off Loss
30 ns	89.1 $\mu$ J	40 ns	43.5 $\mu$ J



**Fig. 12.** Testbed for high temperature switching test.



**Fig. 13.** Experimental turn-on waveforms at 150 °C.



**Fig. 14.** Experimental turn-off waveforms at 150 °C.

### 3. Experimental Results

The double pulse test of the module was done at 650 Vdc bus voltage, 60 A load current and 150 °C. Fig. 12 is a photo of the testing setup. Fig. 13 and Fig. 14 show the switching waveforms of the phase-leg. From the test, the switching times are 140 ns for turn-on and 170 ns for turn-off. The turning on and off total power losses are 3.34 mJ and 2.98 mJ respectively, for the 4 paralleled JFETs in the phase-leg.

### 4. Conclusion

This paper evaluates the electrical performance of a SiC JFET based power module in both simulation and experiments when switching at 650 Vdc voltage and 60 A current. The results show that the switching performance of the SiC JFET module is influenced by JFET inside capacitors, package parasitics and gate drive circuit. The improvement of gate pins and DC bus design reduce its package parasitics. Different turn-on resistances are used to balance current. External paralleled capacitor and RCD network are used to keep  $-25V < V_{gs} < -17V$ . Simulation and experimental results show the good switching performances of it.

## 5. Literature

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