Elimination of Harmonics in a Five-Level Diode-Clamped Multilevel Inverter Using Fundamental Modulation

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***Abstract* -- In this study, elimination of harmonics in a five-level diode-clamped multilevel inverter (DCMLI) has been implemented by using fundamental modulation switching. The proposed method eliminates harmonics by generating negative harmonics with switching angles calculated for selective harmonic elimination method. In order to confirm the proposed method, first Matlab/Simulink and PSIM simulation results are given. Then the proposed method is also validated by experiments with Opal-RT controller and a 10 kW three-phase, five-level DCMLI prototype.**

***Index Terms* -- Fundamental switching, harmonic elimination, and multilevel inverter.**

I. INTRODUCTION

The problem of eliminating harmonics in switching inverters has been the focus of research for many years. The current trend of modulation control for multilevel inverters is to output high quality power with high efficiency. For this reason, popular traditional PWM modulation methods are not the best solution for multilevel inverter control due to their high switching frequency. The selective harmonic elimination method has emerged as a promising modulation control method for multilevel inverters. The major difficulty for the selective harmonic elimination method is to solve the equations characterizing harmonics; however, the solutions are not available for the whole modulation index range, and it does not eliminate any number of specified harmonics to satisfy the application requirements. The proposed harmonic elimination method is used to eliminate any number of harmonics and can be applied to DCMLI application requirements.

The diode clamped inverter, particularly the three-level one, has drawn much interest in motor drive applications because it needs only one common voltage source. Also, simple and efficient PWM algorithms have been developed for it, even if it has inherent unbalanced dc-link capacitor voltage problem [1]. However, it would be a limitation to applications beyond four-level diode clamped inverters for the reason of reliability and complexity considering dc-link balancing and the prohibitively high number of clamping diodes [2]. Multilevel PWM has lower *dV/dt* than that experienced in some two-level PWM drives because switching is between several smaller voltage levels [3].

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In this paper, a five-level DCMLI switching at the fundamental frequency is proposed. However, many interesting PWM techniques have been proposed for controlling these inverters. The lower order harmonics are eliminated by choosing the switching angles that do not generate specifically chosen harmonics. In this study, an harmonic elimination technique is presented that allows one to control a multilevel inverter in such a way that it is an efficient low total harmonic distortion (THD) inverter that can be used to interface distributed dc energy sources to a main ac grid or as an interface to a motor drive powered by fuel cells, batteries, or ultra-capacitors.

II. DIODE-CLAMPED MULTILEVEL INVERTER

An *m*-level diode-clamped multilevel inverter typically consists of $m-1$ capacitors on the dc bus and produces *m* levels of the phase voltage [4]. A three-phase five-level structure of a DCMLI is shown in Fig. 1. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by four capacitors into five levels. The voltage across each capacitor is V_{dc}, and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes.

Table 1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage V_0 as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair requires that the other complementary switch be turned off. The complementary switch pairs for phase leg *a* are (S_{a1}, $S_{a'1}$), (S_{a2}, $S_{a'2}$), (S_{a3}, $S_{a'3}$), and (S_{a4}, $S_{a'4}$). Table 1 also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg are always adjacent and in series.

TABLE I
DCMLI VOLTAGE LEVELS AND SWITCHING STATES

Voltage V_a	SWITCH STATE							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_4 = 4Vdc$	1	1	1	1	0	0	0	0
$V_3 = 3Vdc$	0	1	1	1	1	0	0	0
$V_2 = 2Vdc$	0	0	1	1	1	1	0	0
$V_1 = Vdc$	0	0	0	1	1	1	1	0
$V_0 = 0$	0	0	0	0	1	1	1	1

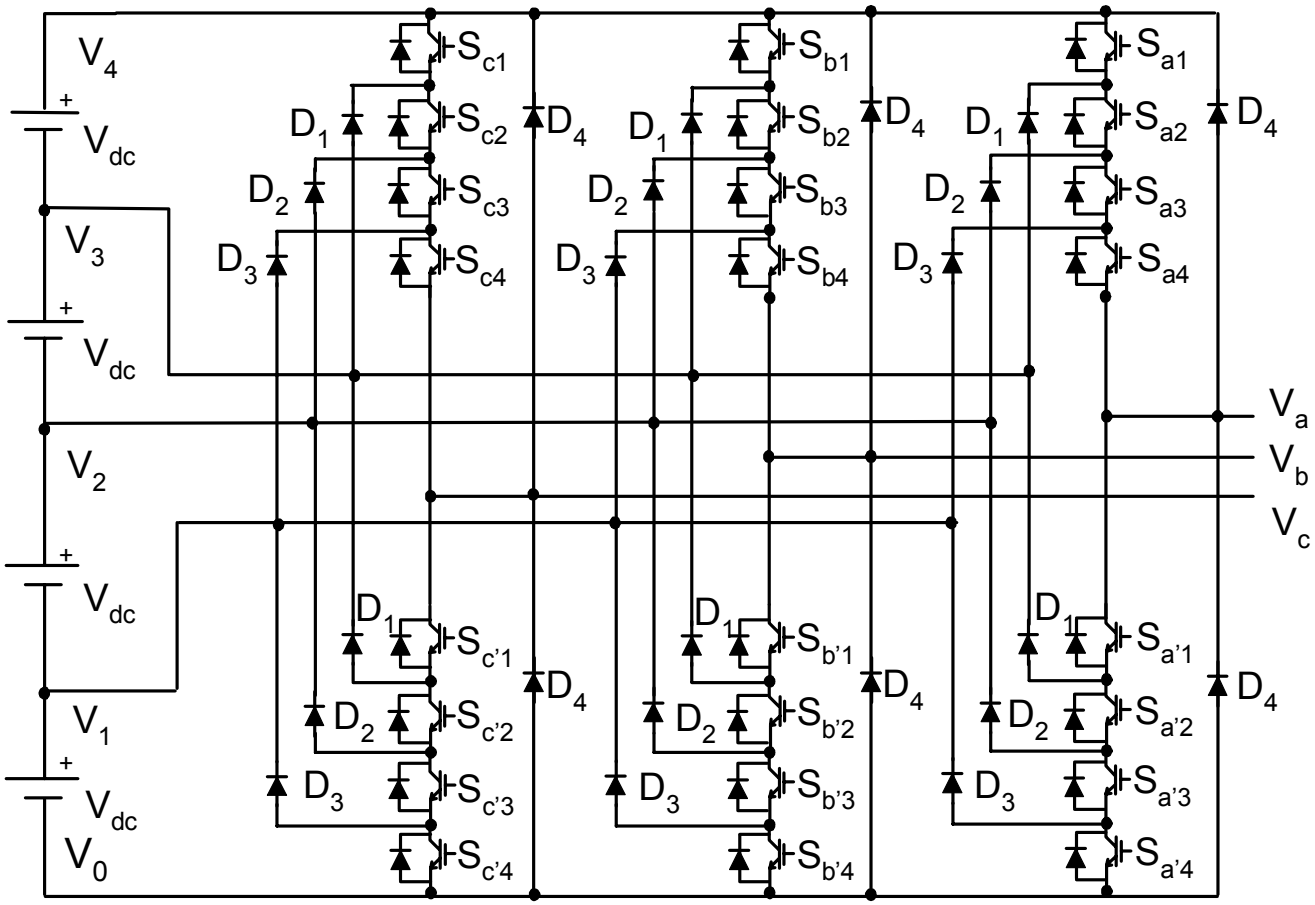


Fig. 1. A three-phase five-level diode-clamped multilevel inverter schematic.

The following are the some advantages and disadvantages of the DCMLI:

Advantages:

- As the number of levels increases the harmonic content of the output waveform decreases the filter size.
- Lower switching losses due to the devices being switched at the fundamental frequency without increasing the harmonic content in the output.
- Reactive power flow can be controlled, as this does not cause unbalance in the capacitor voltages.
- Fast dynamic response.
- Back to back operation is possible.

Disadvantages:

- High number of clamping diodes is required as the number of levels increase.
- Active power transfer causes unbalance in the DC-bus capacitors, this complicates the control of the system.

Fig. 2 shows one of the three line-line voltage waveforms for a five-level DCMLI. The line voltage V_{ab} consists of a phase-leg *a* voltage and a phase-leg *b* voltage. The resulting line voltage is a 9-level staircase waveform. This means that an *m*-level diode-clamped inverter has an *m*-level output phase voltage and a (2*m*-1)-level output line voltage.

The simplest way to control a multilevel converter is to use a fundamental frequency switching control where the switching devices generate an *m*-level staircase waveform that tracks a sinusoidal waveform. In this control, each switching device only needs to switch one time per fundamental cycle, which results in low switching losses and low electromagnetic interference. Considering the symmetry of the waveform, there are only two switching angles (θ_1 and θ_2) that need to be determined in this control strategy, as shown in Fig. 2. Note that the angles θ_1 and θ_2 are measured with respect to the reference angle $\pi/4$.

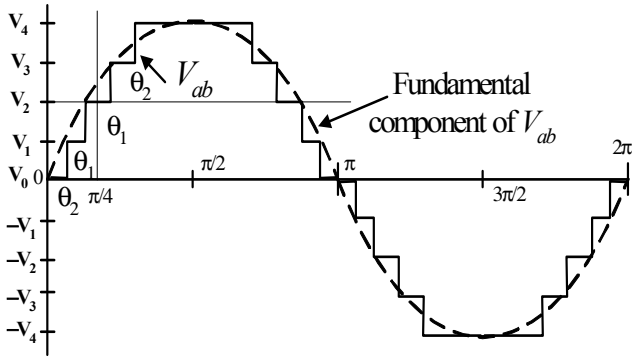


Fig. 2. Line voltage waveform for a five-level DCMLI.

III. PROPOSED METHOD FOR FIVE-LEVEL DCMLI

An important issue in multilevel inverter design is that the voltage waveform is near sinusoidal and the lower order harmonics are eliminated. A key concern in the fundamental switching scheme is to determine the switching angles in order to produce the fundamental voltage and not generate specific higher order harmonics. Often iterative techniques are used to calculate the switching angles [5], though such an approach does not guarantee finding all the possible solutions. Some other fundamental modulation techniques were presented in [6-8].

Previous work in [9] has shown that the transcendental equations characterizing the harmonic content can be converted into polynomial equations, which are then solved using the method of resultants from elimination theory. The work presented here is based on the previous work in [10]. However in this paper, the proposed calculation method results are used for switching of the DCMLI instead of a cascaded H-bridges multilevel inverter.

As shown in Fig. 2, a multilevel inverter can produce a quarter-wave symmetric voltage waveform synthesized by several DC voltages [10]. By applying Fourier series analysis, the output voltage can be expressed as

$$V(t) = \sum_{n=1,3,5...}^{\infty} \frac{4V_{DC}}{n\pi}(\cos(n\theta_1) + (\cos(n\theta_2) + ... + (\cos(n\theta_s))\sin(n\omega t) \quad (1)$$

where s is the number of DC sources, and V_{DC} is the voltage of each DC level. For the DCMLI, the switching angles must satisfy the condition $0 < \theta_1 < \theta_2 < ..... \theta_s < \pi/4$. In order to minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to s-1 harmonic contents can be removed from the voltage waveform.

In general, the most significant low-frequency harmonics are chosen for elimination by properly selecting angles among different level inverters, and high-frequency harmonic components can be readily removed by using additional filter circuits. To keep the number of eliminated harmonics at a constant level, all switching angles must satisfy the condition $0 < \theta_1 < \theta_2 < ..... \theta_s < \pi/4$, or the total harmonic distortion (THD) increases dramatically. Considering the symmetry of the waveform, only two switching angles need to be determined in this strategy, which are θ_1 and θ_2 shown in Fig. 2. For a five-level multilevel inverter, the harmonic equations are given as

$$\cos(\theta_1) + \cos(\theta_2) = m_a$$
$$\cos(5\theta_1) + \cos(5\theta_2) = 0 \quad (2)$$

where modulation index is $m_a = \pi V_1/(4V_{DC})$. By defining $x_i = \cos(\theta_i)$ and then using the trigonometric identity given below

$$\cos(5\theta) = 5\cos(\theta) - 20\cos^3(\theta) + 16\cos^3(\theta) + 16\cos^5(\theta) \quad (3)$$

The polynomial equations given below are used for calculation of the two switching angles (θ_1 and θ_2).

$$p_1(x_1, x_2) = \sum_{n=1}^{2} x_n - m = 0$$
$$p_5(x_1, x_2) = \sum_{n=1}^{2} (5x_n - 20x_n^3 + 16x_n^5) = 0 \quad (4)$$

The switching angles of the DCMLI were determined such that the 5th order harmonic was eliminated while at the same time controlling the value of the fundamental. The appropriate polynomial harmonic equations were first derived as given above, and the equations are solved and modulation index versus switching angles (θ_1 and θ_2) calculated. The proposed fundamental modulation features low switching losses because all the switches operate at the fundamental frequency. In addition, the converter can operate over a fairly wide range of modulation indices based on selective harmonic elimination.

An m-file in Matlab was used to perform all of the above calculations. The switching angles versus the modulation index m_a are shown in Fig. 3. Also, some modulation indices have more than one set of solutions with different values for their residual harmonics and thus THD. For practical applications, the set of switching angles with the lowest THD is used for simulation study and real time implementation.

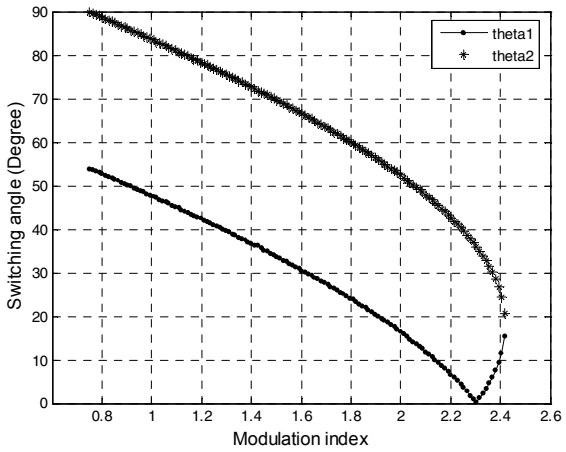


Fig. 3. Switching angles (θ_1 and θ_2) solutions versus modulation index.

IV. SIMULATION RESULTS

Matlab/Simulink and PSIM software packages were linked and run concurrently to perform this simulation implementation. Blocks in Matlab/Simulink generate the proposed fundamental switching pattern. SimCoupler module, an add-on module to the PSIM software, provides an interface between Matlab/Simulink and PSIM software packages for co-simulation [11]. The SimCoupler module enables Matlab/Simulink users to implement and simulate power circuits in their original circuit form, thus greatly shortening the time to set up and simulate a system, which includes electric circuits and motor drives. First, the DCMLI power circuit is simulated in PSIM, and the switching control in Matlab/Simulink. The line voltage waveform and harmonic spectrum of the output voltage that revealed elimination of fifth harmonic are shown in Fig. 4 and Fig. 5, respectively, for 60 Hz.

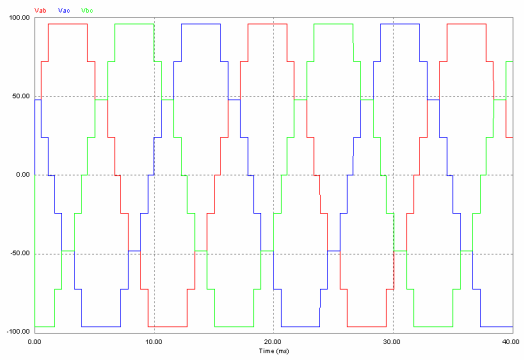


Fig. 4. Line voltage waveforms of the DCMLI output for 60 Hz.

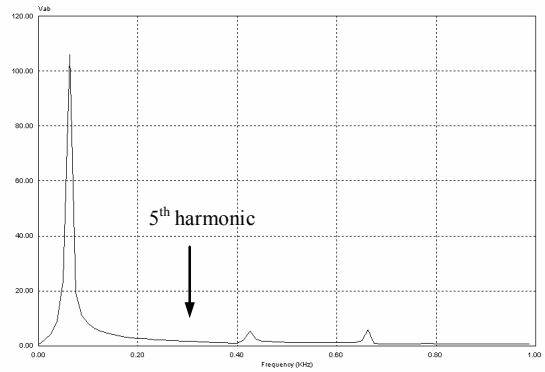


Fig. 5. The harmonic spectrum of line voltage for 60 Hz.

V. Experimental Results

A prototype was built to verify the operation and efficiency of the proposed method. A picture of the laboratory experimental setup is represented in Fig. 6 that includes power supply, five-level DCMLI circuit, three-phase induction motor, and measurement equipment. The DCMLI supplies a three-phase induction motor rated at 250 W, 1725 rpm, 1.5 A, and 208 V coupled with a dc generator (250 W) as a load of the induction motor.

In this work, the RT-Lab real-time computing platform from Opal-RT-Technologies Inc. [12] was used to interface the computer to the five-level DCMLI. The Opal RT-Lab system is utilized to generate gate drive signals and interfaces with the gate drive board. This system allows one to implement the switching algorithm in Simulink that is then converted to *C* code using real-time workshop from Mathworks. The RT-Lab software provides icons to interface the Simulink model to the digital I/O board and converts the *C* code into executables.

The step size for the real-time implementation was 10 microseconds, which was used to obtain an accurate resolution for implementing the switching times. The real-time implementation is accomplished by placing the data in a lookup table and therefore does not require high computational power for implementation.

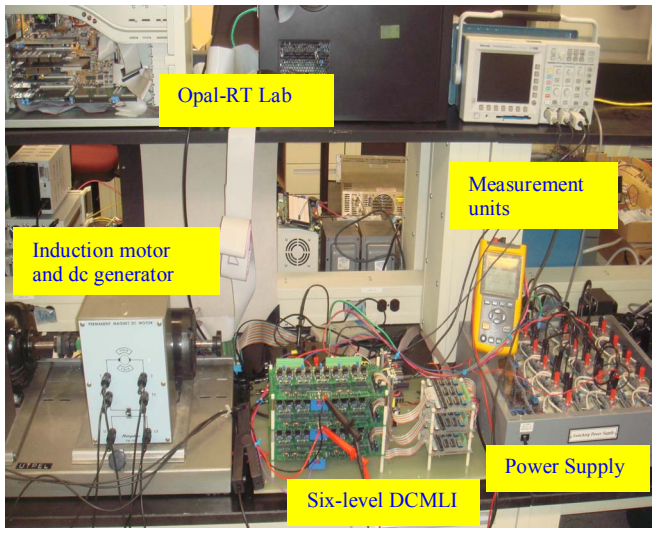


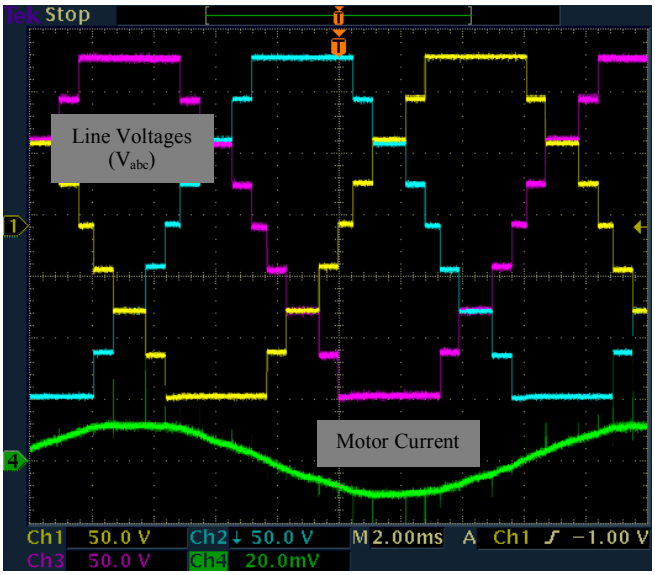
Fig. 6. The five-level DCMLI experimental setup.

Fig. 7(a) shows the three-phase line-to-line voltages and motor current waveforms, and Fig. 7(b) illustrates its corresponding fast Fourier transform (FFT) spectrum that shows the 5th, 13th and triplen harmonics are absent from waveform. The output voltage has nine levels, and the wave shape is near sinusoidal. Using the data in Fig. 7(b), the total harmonic distortion (THD) of the line-line voltage was computed to be 10 %. Since the magnitude of the lower order harmonics is very low, there is no need for a large filter circuit.

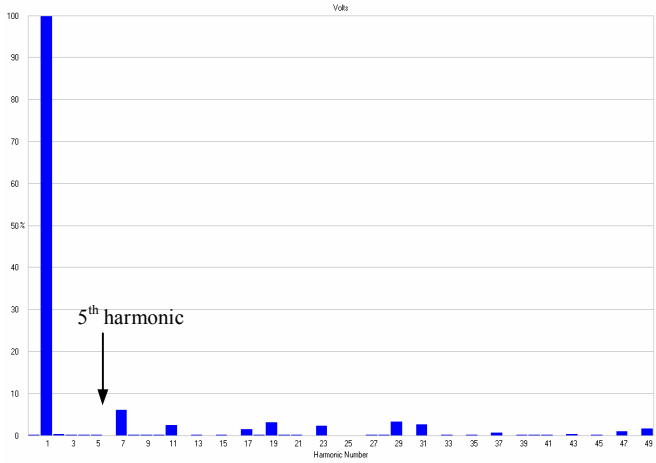
Experimental verification that the low order harmonics are indeed eliminated is also presented by driving a three-phase induction motor from a five-level DCMLI. Since five-level DCMLI can generate a nine-level line-to-line staircase waveform, the generated voltage and current waveforms are sinusoidal shape even at fundamental switching frequency. The THD level of output current of the inverter was as low as 1.9% at full load with fundamental frequency switching.

The conversion efficiency of the inverter, which was measured with a Yokogawa PZ 4000 power analyzer, at low power levels is more than 95%, and the maximum efficiency is about 98.5%, which is comparatively higher than conventional PWM inverters. Negligible switching losses occur for this system due to the low switching frequency employed. In the present case, the main causes of inverter losses are related to semiconductor conduction losses. Each switch in the inverter switches only once per cycle when performing fundamental frequency switching; this results in high efficiency.

Experimental waveforms, efficiency and harmonic measurements, obtained from a small-scale lab prototype, have been used to validate the proposed fundamental switching modulation method and the feasibility of the application of fundamental frequency modulated the three-phase five-level DCMLI. The proposed technique, while maintaining switching at fundamental frequency, is simple and requires relatively simple control circuitry and the output quality becomes better as the number of levels increases. The proposed fundamental frequency operated DCMLI based power system presented a good performance concerning efficiency and power quality.



(a)



(b)

Fig. 7. (a) Three-phase line voltages and motor current waveforms (b) FFT spectrum of output voltage in experiment.

VI. Conclusion

The selected harmonic elimination is a popular issue in multilevel inverter design. The proposed selective harmonic elimination method for DCMLI has been validated in both simulation and experiment. The simulation and experimental results show that the proposed algorithm can be used to eliminate any number of specific lower order harmonics effectively and results in a dramatic decrease in the output voltage THD. In the proposed harmonic elimination method, the lower order harmonic distortion is largely reduced in fundamental switching. Furthermore, in the experiments reported here, an induction motor load is connected to the three-phase five-level DCMLI, and the current as well as the voltage waveforms are collected for analysis. The FFTs of these waveforms show that their harmonic content is close to the simulated values.

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