Fault Detection and Reconfiguration Technique for Cascaded H-bridge 11-level Inverter Drives Operating under Faulty Condition

Surin Khomfoi[1], Leon M. Tolbert[2]
[1] King Mongkut's Institute of Technology Ladkrabang, Dept. of Electrical Engineering, Faculty of Engineering
Chalongkrung Rd. Ladkrabang Bangkok, 10530 THAILAND
[2] The University of Tennessee, Electrical and Computer Engineering
414 Ferris Hall, Knoxville, TN 37996-2100, USA

***Abstract*-A fault detection and reconfiguration technique for a cascaded H-bridge 11-level inverter drives during faulty condition is proposed in this paper. The ability of cascaded H-bridge multilevel inverter drives (MLID) to operate under faulty condition is also discussed. Output phase voltages of a MLID can be used as a diagnostic signal to detect faults and their locations. AI-based techniques are used to perform the fault classification. A neural network (NN) classification is applied to the fault diagnosis of a MLID system. Multilayer perceptron (MLP) networks are used to identify the type and location of occurring faults. The principal component analysis (PCA) is utilized in the feature extraction process to reduce the NN input size. The genetic algorithm (GA) is also applied to select the valuable principal components to train the NN.**

A reconfiguration technique is also developed. The developed system is validated with simulation and experimental results. The developed fault diagnostic system requires about 6 cycles (~100 *ms* at 60 Hz) to clear an open circuit and about 9 cycles (~150 *ms* at 60 Hz) to clear a short circuit fault. The experiment and simulation results are in good agreement with each other, and the results show that the developed system performs satisfactorily to detect the fault type, fault location, and reconfiguration.

***Index Terms*—Fault diagnosis, fault tolerance, genetic algorithm, multilevel inverter, neural network, power electronics**.

I. INTRODUCTION

For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations, and also multilevel inverter drive (MLID) systems have become a solution for high power drive applications. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Two topologies of multilevel inverters for electric drive application have been discussed in [1]. The cascaded MLID is a general fit for large automotive all-electric drives because of the high VA rating possible and because it uses several dc voltage sources which would be available from batteries or fuel cells [1].

A possible structure of a three-phase cascaded multilevel inverter drive for an electric vehicle is illustrated in Fig. 1. The series of H-bridges makes for modularized layout and packaging; as a result, this will enable the manufacturing process to be done more quickly and cheaply. Also, the

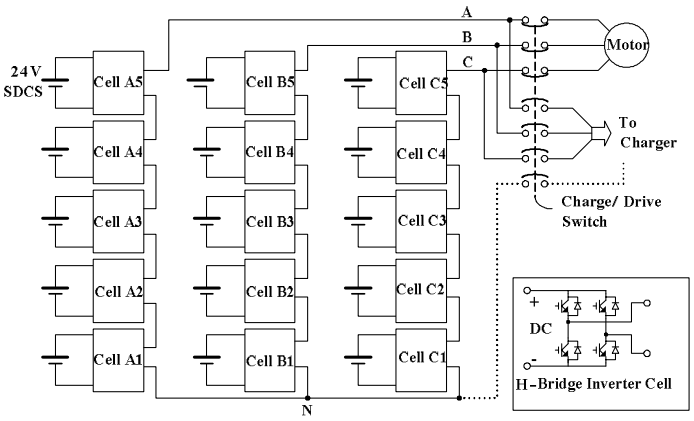


Fig. 1. Three-phase wye-connection structure for electric vehicle motor drive.

reliability analysis reported in [2] indicates that the fault-tolerance of cascaded MLID has the best life cycle cost. However, if a fault (open or short circuit) occurs at a semiconductor power switch in a cell, it will cause an unbalanced output voltage and current, while the traction motor is operating. The unbalanced voltage and current may result in vital damage to the traction motor if the traction motor is run in this state for a long time.

Generally, the passive protection devices will disconnect the power sources or gate drive signals from the multilevel inverter system whenever a fault occurs, stopping the operated process, overlooking the consequence of such accidental shut down. For instance, in the case of a MLID fault such as open or short circuit in a power switch, the fuse in the dc link will blow when the current reaches to the safety limit, disconnecting the dc voltage supply. This may cause vitally consequent damages in the motor if the motor is running at base speed with rated load. Therefore, the passive protection system may not be adequate if the application of a MLID needs a continuous operation or the motor is connected with a large load such as conveyer or hybrid/electric vehicle. It would be better if one can isolate the fault and continue to operate the motor at lower power levels or degraded performance than completely stopping it.

Although a cascaded MLID has the ability to tolerate a fault for some cycles, it would be better if we can detect the fault and its location; then, switching patterns and the modulation

index of other active cells of the MLID can be adjusted to maintain the operation under balanced load condition. Of course, the MLID can not be operated at full rated power. The amount of reduction in capacity that can be tolerated depends upon the application; however, in most cases a reduction in capacity is more preferable than a complete shutdown.

A study on fault diagnosis in drives begins with a conventional PWM voltage source inverter (VSI) system [3-5]. Then, artificial intelligent (AI) techniques such as fuzzy-logic (FL) and neural network (NN) have been applied in condition monitoring and diagnosis [6-8]. Furthermore, a new topology with fault-tolerant ability that improves the reliability of multilevel converters is proposed in [9]. A method for operating cascaded multilevel inverters when one or more power H-bridge cells are damaged has been proposed in [2, 10]. The method is based on the use of additional magnetic contactors in each power H-bridge cell to bypass the faulty cell.

One can see from the concise literature survey that the knowledge and information of fault behaviors in the system is important to improve system design, protection, and fault tolerant control. Thus far, limited research has focused on MLID fault diagnosis and reconfiguration. Therefore, a MLID diagnostic system is proposed in this paper that only requires measurement of the MLID's voltage waveforms and does not require measurement of currents.

II. Reliability Considerations of MLID

Since multilevel inverters contain several semiconductors connected in series to achieve medium voltage and high power demand, one might consider that multilevel inverters are less reliable. In contrast, multilevel cascaded H- bridge inverters using modular series-cells with separated dc sources as depicted in Fig. 1 could improve reliability if the MLID has the ability to detect and bypass the faulty cell. If one of the power cells fails, it can be bypassed and operation can continue at reduced voltage capacity. The definition of reliability given by [11] is "*the probability of a device performing its purpose adequately for the period of time intended under the operating condition encountered*". The word *adequately* permits some application at reduced capacity to be included in the probability calculations [2].

The engineering reliability analysis in a system is usually concerned with the reliability R and/or the probability of failure P. As a system is considered reliable unless it fails, the reliability and probability of failure sum to unity as explained in equation (1) [11].

$$\begin{aligned} R(t) + P(t) &= 1, \\ R(t) &= 1 - P(t), \\ P(t) &= 1 - R(t), \end{aligned} \tag{1}$$

where $P(t)$ is probability of a system will fail by time t,

$R(t)$ is probability of a system will still be operational by time t. Therefore, (1) can be applied in MLID system reliability analysis. Suppose that the cascaded H-bridge MLID system as shown in Fig. 1 contains N cells and can not tolerate any failures; then, if the probability of a single cell will function properly during a time interval is R, so that the probability all N cells will function properly during the same time interval is R^N because the MLID system is considered as series system in this case. $P(t)$ and $R(t)$ can be defined as the point density functions; then, $P = \frac{d\,P(t)}{d(t)}$ and $R = \frac{d\,R(t)}{d(t)}$. Next, if the MLID has an extra cell which can tolerate failures, the MLID reliability will become $R^N + [N \times R^{(N-1)} \times (1- R)]$ instead of R^N. It is obvious that the MLID with a tolerated failure cell has a higher reliability than the one without tolerance for failures. A numerical reliability example of a MLID can be illustrated in Table I. Suppose that the MLID in Table I has a cell reliability R of 99% and it contains totally 15 cells. As can be seen, with one tolerated cell in each phase, the reliability of the MLID can increase from 86% to 99.0%; therefore, a fault diagnostic and fault reconfiguration (bypass) system can improve the reliability of the MLID system. In addition, for the case of m tolerated cells, the reliability function can be written as

$$R_m = \sum_{i=0}^{m} \left(\frac{N!}{(N-i)! \times i!} \times R^{(N-i)} \times (1-R)^i \right), \tag{2}$$

where m is number of tolerated cells,
N is number of cells in MLIDs,
R_m is total reliability of the system.

Table I.
Numerical example of 15 cells MLID with 99% reliability (R) in each power cell.

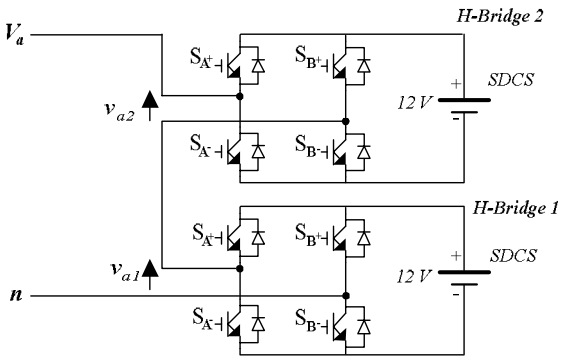
Number of tolerated cell faults	*Reliability Function*	*Reliability (Percentage)*
0	$R_0 = R^N$	86.006%
1	$R_1 = R_0 + [N \times R^{(N-1)} \times (1- R)]$	99.037%
2	$R_2 = R_1 + [(N \times (N-1) \times (R^{(N-2)}) \times (0.5 \times (1-R)^2)]$	99.958%
3	$R_3 = R_2 + [(N \times (N-1) \times (N-2) \times (R^{(N-3)}) \times (0.1667 \times (1-R)^3)]$	99.999%

III. Fault Diagnostic Methodology

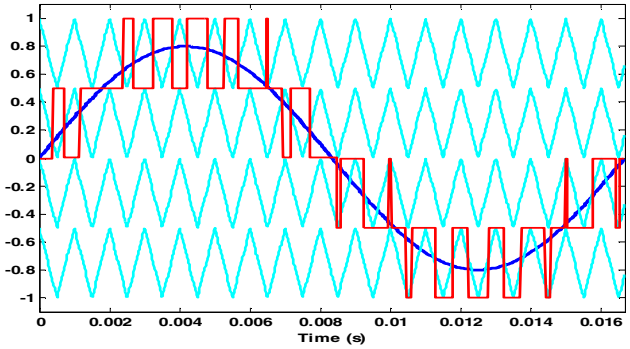
Before continuing discussion, it should be emphasized that the multilevel carrier-based sinusoidal PWM is used for controlling gate drive signals for the cascaded MLID. Fig. 2 shows that the output voltages can be controlled by controlling the modulation index (m_a). To expediently understand, the two separate dc sources (SDCS) cascaded MLID structure is used as an example in this section.

A. Diagnostic Signals

The selection of diagnostic signals is very important because the neural network could learn from unrelated data to classify faults which would result in improper classification. Simulation results (using power simulation (PSIM) from Powersim Inc.) of input motor current waveforms during an open circuit fault at different locations of the MLID (shown in Fig. 2 (a)) are illustrated in Fig. 3 and Fig. 4. As can be seen in Fig. 3 and Fig. 4, the input motor currents can classify open



(a)



(b)

Fig. 2. (a) Single-phase multilevel-inverter system; (b) Multilevel carrier-based sinusoidal PWM showing carrier bands, modulation waveform, and inverter output waveform (m_a = 0.8/1.0).

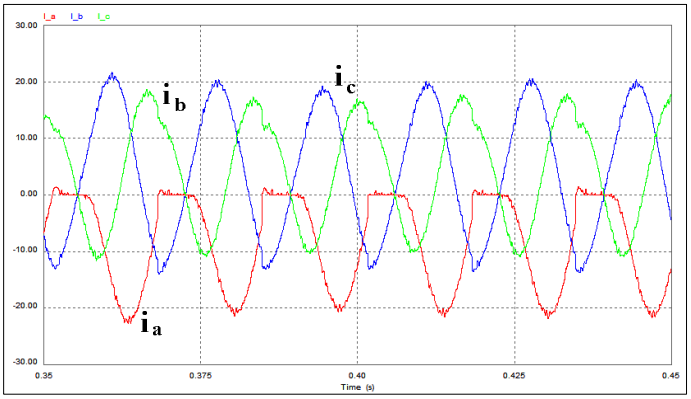
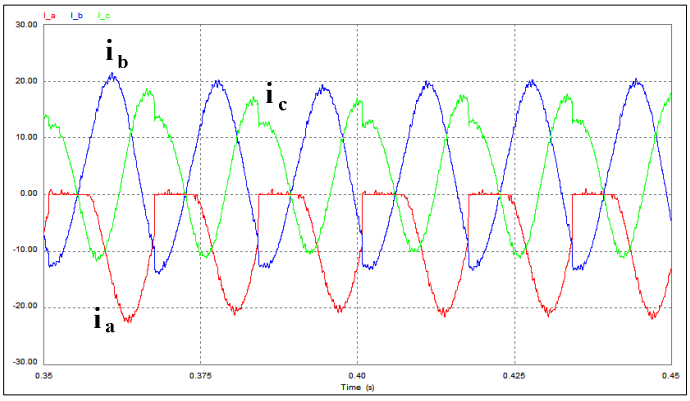


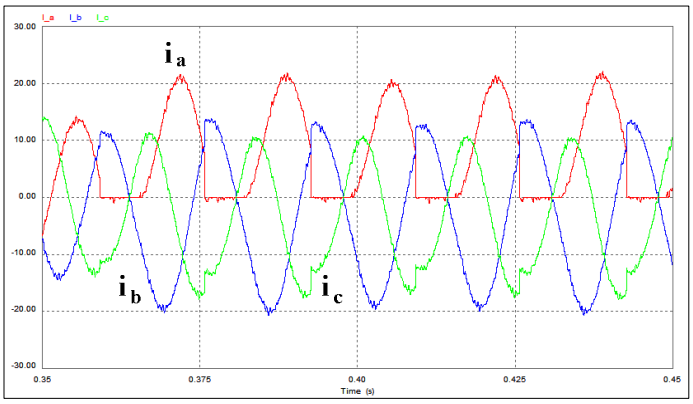
Fig. 3. Input motor currents during open circuit fault at switch S_{A+} of H-bridge 2.

circuit faults at the same power cell by tracking current polarity (see Fig. 4); however, it is difficult to classify the faults at different power cells; the current waveform for a fault of S_{A+} in H-bridge 2 (Fig. 3) looks identical to that for a fault of S_{A+} in H-bridge 1 (Fig. 4 (a)). As a result, the detection of fault locations could not be achieved with only using input motor current signals. Also, the current signal is load dependent: the load variation may lead to misclassification; for instance, light load operation as reported in [12].

Auspiciously, Fig. 2 indicates that an output phase PWM voltage is related to turn-on and turn-off time of associated



(a)



(b)

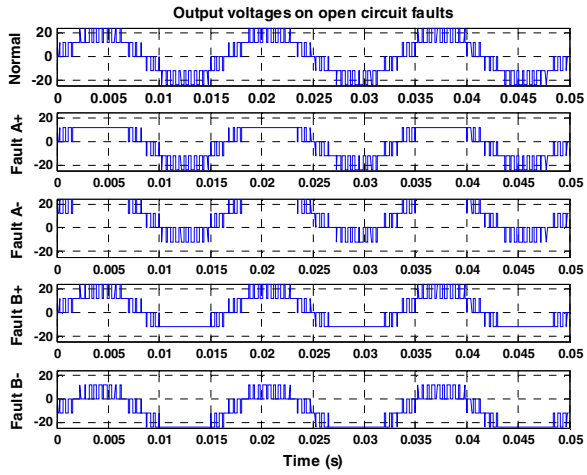
Fig. 4. Input motor currents during open circuit fault at H-bridge 1: (a) switch S_{A+}, (b) switch S_{B+}.

switches; hence, a faulty switch can not generate a desired output voltage. The output voltage for a particular switch is zero if the switch has a short circuit fault, whereas the output voltage is about V_{dc} of SDCS if the switch has an open circuit fault. For this reason, the output phase voltage can convey valuable information to diagnose the faults and their locations. The simulation results of output voltages are shown for an MLID with open circuit faults and short circuit faults in Fig. 5. One can see that all fault features in both open circuit and short circuit cases could be visually distinguished.

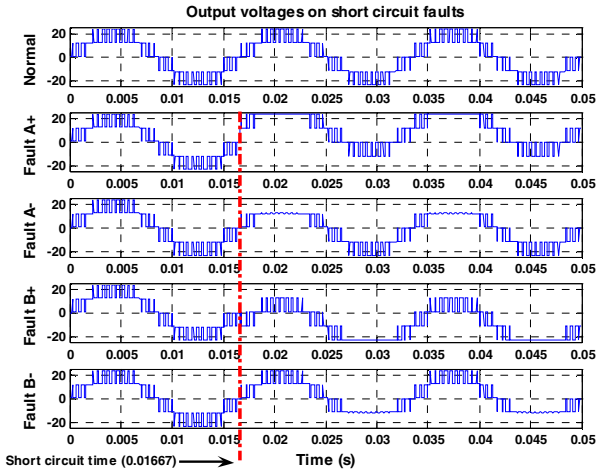
B. AI-Based Techniques for Fault Diagnosis

It is possible that artificial intelligent (AI) based techniques can be applied in condition monitoring and diagnosis. AI-based condition monitoring and diagnosis have several advantages. For instance, AI-based techniques do not require any mathematical models; therefore, the engineering time and development time could be significantly reduced [13]. The methodology of fault diagnostic system using AI has been reported in [14-16] and will not be repeated here. The discussion of AI presented in this section will be brief, providing only the indispensable notion to elucidate the fundamental AI-based approach applied to a fault diagnosis system in a MLID.

First, the feature extraction of the output voltage signals is performed by using FFT; then, the principal component



(a)



(b)

Fig. 5. Simulation of output voltages signals (a) open circuit faults, (b) short circuit faults showing fault features at S_{A+}, S_{A-}, S_{B+}, and S_{B-} of H-bridge 2 with modulation index = 0.8 out of 1.0.

analysis (PCA) is used in the feature extraction process. PCA offers a lower dimensional input space which will also usually reduce the time necessary to train a neural network, and the reduced noise (by keeping only valuable principal components (PCs)) may improve the mapping performance [15]. Next, a genetic algorithm (GA) is applied to search for the best combination of PCs to train the neural network as explained in [16]. The output of the GA is the best combination of PCs which provide the weight and bias matrix of neural networks used for the classification task. After that, the weight and bias matrix of the neural networks will be implemented in Simulink interfacing with FFT and PCA subsystem as shown in Fig. 6. The PCA and GA process will be performed off-line to achieve the best combination of PCs.

Before continuing discussion, it should be mentioned that the methodology of fault diagnosis presented in [15-16] can be applied to any other cascaded H-bridges MLID. However, some minor processes are different such as neural network structure, input/output data set, and principal component (PC) selection. Since the simulation and experiment validation will

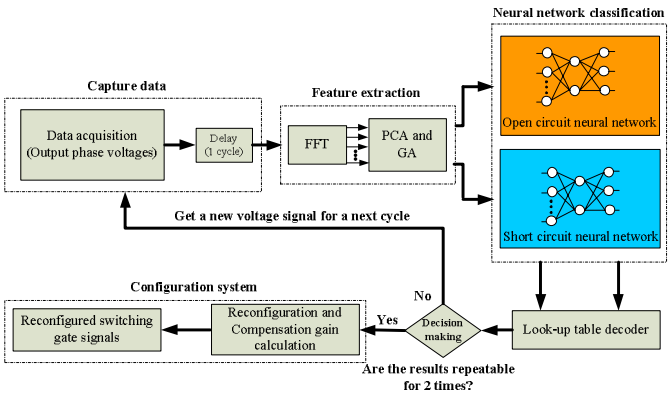


Fig. 6. Fault diagnostic diagram for 11-level MLID with 5 SDCS.

be performed with 11-level MLID, the fault diagnostic processes for the 11-level MLID are explained in the following.

C. Neural Network Structure

The fault diagnostic diagram for an 11-level MLID with 5 SDCS is depicted in Fig. 6. The neural network classification process consists of two networks: open circuit network and short circuit network. The training time and required memory for implementation are reduced with the segregated neural network as reported in [17, 18]. Moreover, in this particular case, the short circuit data set includes the loss of separate dc source (SDCS) condition due to the fuse protection because the fuse may blow before the fault is detected; therefore, the short circuit neural network may contain more complexity than the open circuit neural network. Also, the neural networks may be assigned to have the ability to provide "do not know" conditions. The multilayer feedforward perceptron (MLP) networks are used in both open circuit and short circuit neural networks. The neural network architecture is based upon GA selection as discussed in [16]. The input neurons depend on GA selection; however, for this example, 1 hidden layer with 4 hidden nodes and 6 output nodes are assigned.

D. Input/Output Data

The input/output data set diagram for 11-level MLID is illustrated in Fig. 7. We can see that the set of original input data at each MLID operation point (modulation index) contains five fault classes: normal, Fault A+, A-, B+, and B-. Modulation indices (m_a) are observations changing with desired load. In this particular case, m_a is varied from 0.6 to 1.0 with 0.05 intervals. The original data are divided into two subsets: Open circuit and short circuit. Also, each subset is separated into one training set and two testing sets as shown in Fig. 7. Both open circuit and short circuit neural networks are trained with both open and short circuit training sets. However, the open circuit neural network will be trained with short circuit training set with "do not know" target binary and vice versa with the short circuit neural network as depicted in Fig. 7.

Target binary variables are also illustrated in Table II. Six binary bits are used to code the input/output mapping. The first two bits (counting from the right bits 0 and 1) are utilized to code the faulty switches, the 3rd bit from the right (bit 2) is

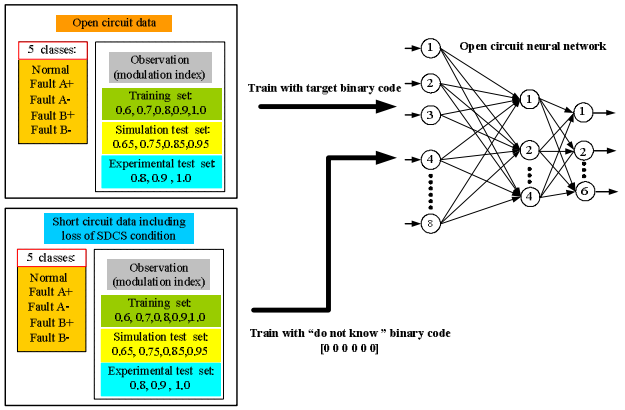


Fig. 7. Training and testing data set diagram.

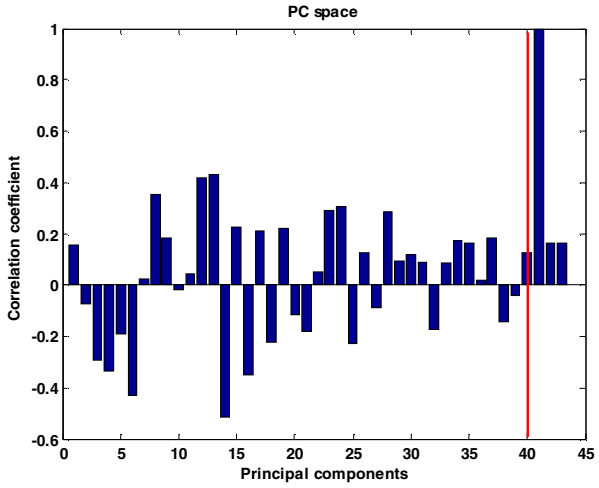
TABLE II.
TARGET BINARY CODE FOR 11-LEVEL MLID.

Condition		Number of binary bits and their description					
		Faulty cell			*Fault type*	*Faulty switch*	
		5	4	3	2	1	0
Normal		1	1	1	1	1	1
Faulty cells	1	0	0	1	-	-	-
	2	0	1	0	-	-	-
	3	0	1	1	-	-	-
	4	1	0	0	-	-	-
	5	1	0	1	-	-	-
Fault types	open	-	-	-	0	-	-
	short	-	-	-	1	-	-
Faulty switches	Fault A+	-	-	-	-	0	0
	Fault A-	-	-	-	-	0	1
	Fault B+	-	-	-	-	1	0
	Fault B-	-	-	-	-	1	1
"Do not know"		0	0	0	0	0	0

used to code the fault type, and the last three bits (bits 3, 4, and 5) are used to code which cell has faulted. Also, the code [1 1 1 1 1 1] is used to represent the normal condition, whereas the code [0 0 0 0 0 0] is used to characterize the "do not know" condition. Therefore, the six output neurons are used for particular 11-level MLID. For instance, if the neural network provides [0 1 1 0 0 1] as the outputs, we can decode the fault type and location as cell 3 is faulty with open circuit fault at switch S_A-. This decoder paradigm can be implemented in Simulink model by using 2-D dimension look-up table as shown in Fig. 6.

E. Principal Component Selection

The selection of principal components (PCs) is significant because input selected PCs can cause uncertainty results: (1) additional unneeded input PCs to the neural network can increase the solution variance; (2) absent necessary input PCs can increase bias. The correlation coefficient (CC) between PCs and target variable is shown in Fig. 8. As can be seen in Fig. 8 (a), 4 PCs have CC higher than 0.4; PC *6, 12, 13,* and *14*. This means that PC *6, 12, 13, 14* are good predictors for the first bit of target variables. Also, PC *15, 18,* and *36* are a good predictors for the second bit of the target variable. We can see that different bits of the target variable have different desired



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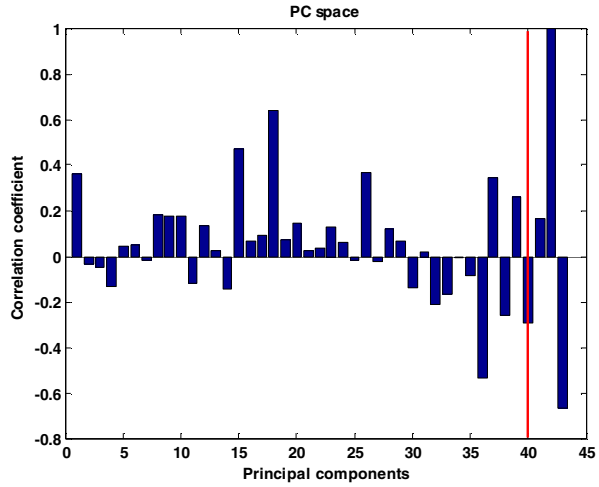


(b)

Fig. 8. Correlation coefficient of PCs and target variables: (a) first bit of target variable, (b) Second bit of target variable.

predictors (PCs). Since we have 6 bits of the target variable, it would be better to use a multivariable optimization technique to select the best combination of PCs. Therefore, a genetic algorithm (GA) is used to search for the best combination of PCs to train the neural network as proposed in [16, 18]. By using the methodology proposed in [16], the principal components (PCs) are selected by GA. 8 PCs (*PC 1, 2, 3, 5, 7, 8, 13, and 14*) are selected for an open circuit neural network, whereas 11 PCs (*PC 2, 3, 4, 5, 7, 8, 9, 11, 12, 13, and 14*) are chosen for short circuit neural networks. Therefore, the neural network architecture for open circuit neural network has 8 input neurons, 4 hidden neurons and 6 output neurons, whereas the short circuit neural network architecture has 11 input neurons, 4 hidden neurons and 6 output neurons.

IV. RECONFIGURATION TECHNIQUE

A. Corrective Action Taken

The basic principal of the reconfiguration method is to bypass the faulty cell (H-bridge); then, other cells in the MLID are used to compensate for the faulty cell. For instance, if cell

2 of MLID in Fig. 2 has an open circuit fault at S_{A+}; accordingly, S_{A-} and S_{B-} need to be turned on (1), whereas S_{B+} needs to be turned off (0) to bypass cell 2. The corrective actions taken for other fault locations are shown in Table III. As can be seen, the corrective action would be the same for cases that have similar voltage waveforms during their faulted mode (for instance, see Fig. 5 for a short circuit fault in S_{A+} and open circuit fault in S_{A-}). Therefore, even if the fault may be misclassified (an actual short circuit fault at S_{A+} is misclassified as an open circuit fault at S_{A-} or vice versa), the corrective action taken would still solve the problem.

B. Reconfiguration Method

The reconfiguration diagram for an 11-level MLID with 5 SDCS is illustrated in Fig. 9. The turn-on intervals of each cell are not equal with multilevel carrier-based sinusoidal PWM: cell 1 has the longest turn-on interval, then the turn-on interval decreases from cell 2 to cell 5 as a staircase PWM waveform. The desired output voltage of a MLID can be achieved by controlling modulation index (m_a). For instance, suppose cell 2 has an open circuit fault at S_1 while the MLID operates at m_a = 0.8/1.0 (MLID is operated with four cells (cell 1-4)). We can see from Fig. 9 (b) that S_3 and S_4 need to be turned on, then the gate signal of cell 2 will be shifted up to control cell 3, then the gate signal of cell 3 will shift to cell 4, and the gate signal of cell 4 will shift to cell 5 respectively.

This reconfiguration also applies to other phases of MLID in order to maintain balanced output voltage. By using this method, the operation of MLID in a modulation index range of 0.0 to 0.8 (out of 1) can be fully compensated such that the inverter will continue to function like normal operation; however, if MLID operates at $m_a > 0.8$ and has a fault, lower order harmonics will occur in the output voltage since the MLID will operate in the overmodulation region in order to output the full requested voltage as illustrated in Fig. 10.

The compensated gain of the MLID operating at $m_a > 0.8$ is shown in Fig. 11. This compensated gain can also be written as a function of m_a by using polynomial curve fitting. Because the overmodulation region has a nonlinear relationship between modulation index and output fundamental voltage, the compensated gain is calculated in particular modulation indices; then, the polynomial function represents the nonlinear characteristic of this particular application. In addition, this polynomial function can be implemented in a Simulink model. The fitting function can predict the compensated gain with a norm of residuals less than 0.09. The overmodulation region will occur when the MLID operates at $m_a > 0.825$. To relieve this problem, space vector, and third harmonic injection PWM schemes may be used. Also, a redundant cell can be added into the MLID, but the additional part count should be considered. The reconfiguration effect and limitation of this reconfiguration method have been reported in [20].

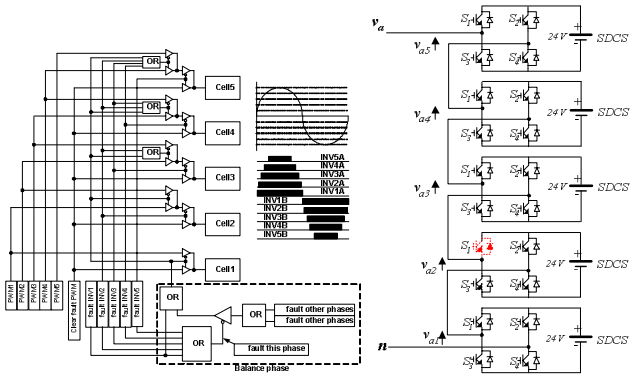
V. Simulation and Experiment Validation

A. Simulation Setup

Two simulation programs are used in the simulation setup: Matlab-Simulink and PSIM [21]. Matlab-Simulink is used to

Table III.
Gate Drive Signals of Corrective Action Taken

Fault types	Locations	Signal S_A+	Signal S_A-	Signal S_B+	Signal S_B-
Open circuit	S_A+	0	1	0	1
	S_A-	1	0	1	0
	S_B+	0	1	0	1
	S_B-	1	0	1	0
Short circuit	S_A+	1	0	1	0
	S_A-	0	1	0	1
	S_B+	1	0	1	0
	S_B-	0	1	0	1



(a) (b)

Fig. 9. Reconfiguration diagram for MLID with five SDCS: (a) Reconfiguration diagram, (b) H-Bridge 2 Switch S_1 open circuit fault at second level of single-phase multilevel-inverter with 5 SDCS.

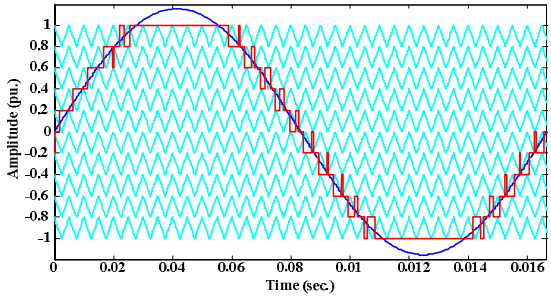


Fig. 10. Multilevel carrier-based sinusoidal PWM with 2 kHz switching frequency for 5 SDCS MLID showing carrier bands, modulation waveform, and inverter output waveform (m_a = 1.2/1.0)

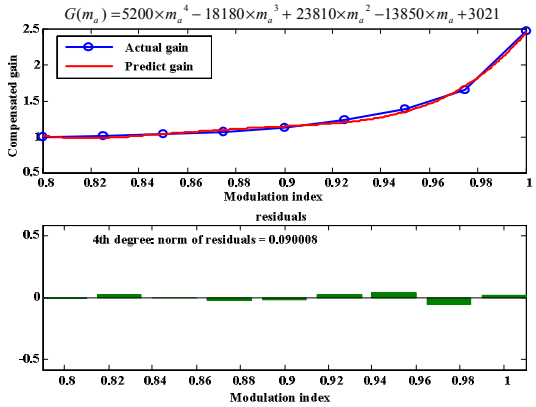


Fig. 11. Compensated gain of the MLID operating at $m_a > 0.8$.

implement feature extraction (FFT and PCA), neural network classification, and reconfiguration. A reconfiguration is corrective method to continuously operate a MLID after the faults are detected. PSIM is used to implement the MLID power circuit. It should be noted that the same Simulink model is used in both simulation and experiment.

B. Experimental Setup

The experimental setup is represented in Fig. 12. A three-phase wye-connected cascaded multilevel inverter using 100 V, 70 A MOSFETs is used. The MLID supplies an induction motor (1/3 hp) coupled with a dc generator load (1/3 hp). The Opal RT-Lab system [22] is utilized to generate gate drive signals and interfaces with the gate drive board. The switching angles are calculated by using a Simulink model based on multilevel carrier-based sinusoidal PWM with 2 kHz switching frequency. A separate individual power supply is supplied to each cell of the MLID, consisting of 5 cells per phase as shown in Fig. 1. Open and short circuit fault occurrences are created by physically controlling the switches in the fault-creating circuit. A Yokogawa DL 1540c is used to measure output voltage signals as ASCII files. The voltage spectrum is calculated and transferred to the Opal-RT target machine.

C. Results

C.1 Open circuit case

The simulation and experimental results are shown in Fig. 13. The faulty power cell (S_{A+}) was placed at cell 2 on phase A (see Fig. 1), and the multilevel inverter drive was operating at 0.8/1.0 modulation index before the fault occurs. We can see that the simulation and experimental results agree with each other. The fault diagnostic system requires about 6 cycles (~100 *ms* at 60 Hz) to clear the open circuit fault. Obviously, the open circuit fault causes unbalanced output voltage (V_{an}) of the MLID during the fault interval, and the average current on phase A (I_a) has negative polarity during the fault interval.

C.2 Short circuit case

The faulty power cell (S_{A+}) of the short circuit case was placed at power cell 3 on phase A (see Fig. 1), and the multilevel inverter drive was operating at 0.8/1.0 modulation index before the fault occurs. The simulation results of a short circuit fault at cell 3 switch S_{A+} are represented in Fig. 14. The fault diagnostic system also requires about 6 cycles to clear the short circuit fault. Obviously, the peak of the fault current increases about 1.5 times compared with the normal operation. Practically, the fuse protecting the SDCS may blow (disconnect the SDCS from a MLID) before the diagnostic system performs fault clearing so that the output phase-voltage will be zero. The developed diagnostic system can also detect a short fault under the loss of SDCS condition as shown in Fig. 15. The clearing time for this particular case is about 9 cycles.

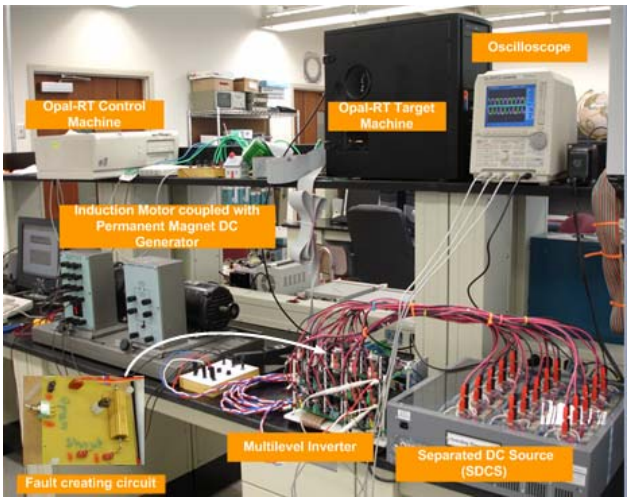
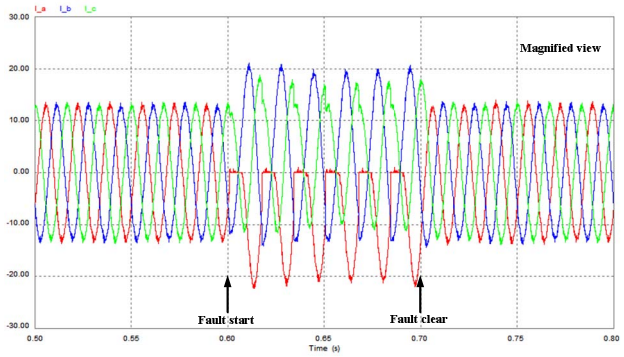
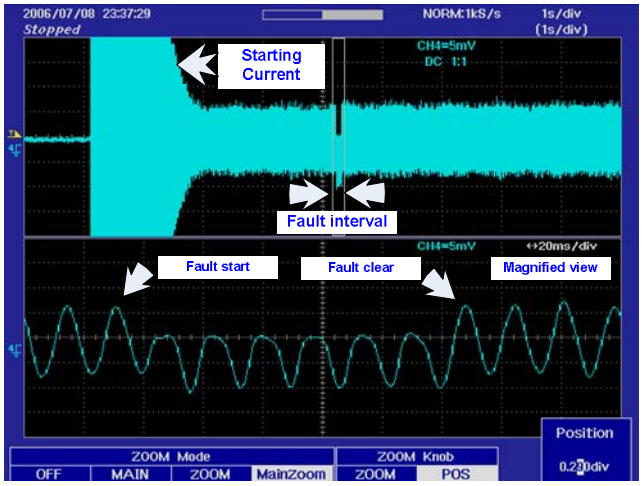


Fig. 12. Experimental setup.



(a)



(b)

Fig. 13. Results of the open circuit fault at S_{A+}, cell 2 of the MLID during operation at m_a = 0.8/1.0: (a) Simulation of current waveforms, (b) Experimental result showing line current (I_a) at the faulty phase.

VI. Conclusion

A fault detection and reconfiguration technique for cascaded H-bridge 11-level inverter drives has been developed. The developed fault diagnostic paradigm has been validated in both simulation and experiment. The fault diagnostic system requires about 6 cycles (~100 *ms* at 60 Hz) to clear the open circuit fault and about 9 cycles (~150 *ms* at 60 Hz) to clear short circuit fault with loss of SDCD. The clearing time of the proposed system can be shorter than this if the proposed system is implemented as a single chip using an FPGA or DSP. The experiment and simulation results in both open circuit

fault and short circuit fault with loss of SDCS are in good agreement with each other. The results show that the proposed diagnostic and reconfiguration paradigm can be applied to MLID applications. Therefore, by using the proposed system, the reliability of the MLID system can be increased.

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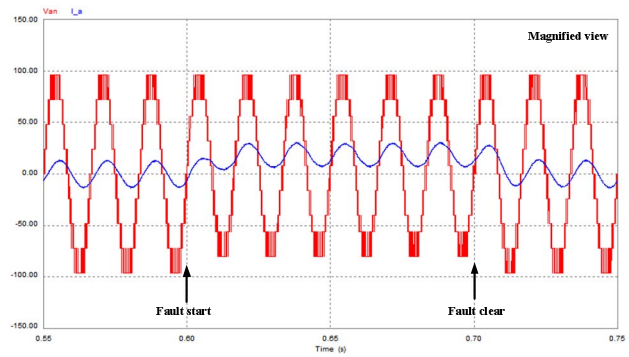
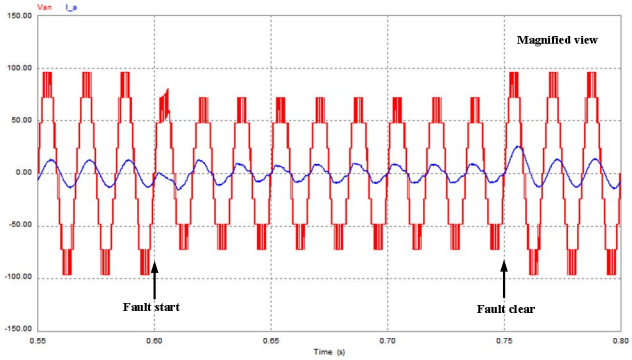
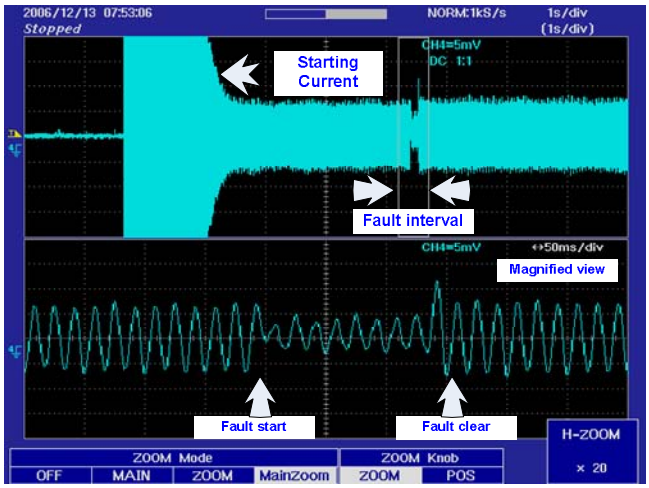


Fig. 14. Simulation results of the short circuit fault at S_{A+}, cell 3 of the MLID during operated at m_a = 0.8/1.0.



(a)



(b)

Fig. 15. Results of the short circuit fault at S_{A+}, cell 3 under loss of SDCS condition at the faulty cell of the MLID during operated at m_a = 0.8/1.0: (a) simulation, (b) experiment showing line current (I_a) at the faulty phase.