SiC GTO Thyristor Model for HVDC Interface

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Abstract— **The development of semiconductor devices is vital for the growth of power electronic systems. Modern technologies like voltage source converter (VSC) based HVDC transmission has been made possible with the advent of power semiconductor devices like GTO thyristors and their high power handling capability. Silicon carbide is the most advanced material among the available wide band gap semiconductors and most SiC devices are currently in the transition from research to manufacturing phase. This paper presents the modeling and design of a loss model for a 4H-SiC GTO thyristor device. The device loss model has been developed based on the device physics and device operation, and simulations have been conducted for various operating conditions. The loss model was integrated in the HVDC transmission system model to study the effects of the Si and SiC devices on the system. The paper focuses on the comparison of Si devices with SiC devices in terms of efficiency and cost savings for a HVDC transmission system.**

***Index Terms*— Semiconductor device modeling, Silicon carbide, Gate turn-off thyrsitor, HVDC transmission.**

I. Introduction

THE need for improved performance of the power electronic systems in many applications has brought about much advancement in silicon (Si) technology. Despite these advances, Si devices are limited to operation at low junction temperatures and low blocking voltages by virtue of the physical properties of Si. Hence, in high power applications, which require efficient, high-density power converters operating at high temperatures, the use of silicon devices is restricted. Silicon carbide (SiC) has superior physical properties like wider bandgap, higher thermal conductivity, higher breakdown field, and higher temperature handling capability that make it a potential material to overcome the limitations of Si. SiC devices have higher voltage blocking capabilities, switching frequencies, temperature operation, and power density than Si devices [1-5]. Various SiC devices have been developed to be used in power applications and to improve the system performance.

GTO thyristors are used in dc applications because of their rapid turn-off capability feature. The GTO thyristor has low on-state conduction losses and high voltage blocking capability making it suitable for high-power switching applications. The advantages of SiC's electrical properties compared to Si have been utilized by the device manufacturers who have transformed these material benefits to device level. These benefits result in the improved system performance. With further developments in semiconductors and their packaging technology, power electronic applications will be extended into power distribution and transmission applications as device efficiency and reliability increases and also as the cost per megawatt falls.

SiC GTO thyristor complimented by the material advantages of SiC has better characteristics than its Si counterpart [6, 7]. This paper presents a comparison study of 4H-SiC GTO thyristor and Si GTO thyristor using an analytical loss model. The model behavior has been studied for various voltage and current ratings and at different operating temperatures. The model was interfaced with an HVDC system model to study the effect of this device on system performance. Converter performance simulation results were evaluated to study the system efficiency; reduction in cost by using SiC GTO thyristors, and the possible other advantages of SiC GTO thyristors over Si GTO thyristors. A description of the device model and simulations are presented, followed by system simulation results to analyze the system performance.

II. Device Model

To study the impact of a device at the system level and to realize the benefits of using the device, its detailed device model is required. The model is developed based on the equations derived for power loss in the conduction state and the energy loss during switching on and switching off periods of the GTO thyristor. Table I gives a list of the variables used in the equations found in this paper.

A. Conduction Losses

The on-state power loss is mainly due to conduction losses, and for a GTO thyristor the on-state power loss equation has been derived to be [8],

$$P_{on-state} = J \cdot (E_g / q) + J \cdot (3\pi/8) \cdot (kT/q) \cdot \exp(3V_B / 2L_a E_c) \quad (1)$$

In (1) the first term in the sum corresponds to the loss due to the voltage drop across the junction, and the second term corresponds to the voltage drop due to on-state specific resistance in the lower base region. This equation can further be simplified and reduced to an expression that is dependent on a fewer parameters.

$$P_{on-state} = J \cdot (E_g / q) + J \cdot (3\pi/8).(kT/q).\exp(D) \quad (2)$$

Where,

$$D = (\varepsilon(N_a + N_d) \cdot E_{bd} \cdot 1.5)/(2 \cdot q \cdot N_a \cdot N_d \cdot \sqrt{(KT/q)}(\mu_n \cdot \mu_p) \cdot \tau_a/(\mu_n + \mu_p) \quad (3)$$

$$V_B = \varepsilon(N_a + N_d) \cdot E_c^2 / (2q \cdot N_a \cdot N_d) \quad (4)$$

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$$\tau_a = \tau_n + \tau_p \quad (5)$$

$$L_a = (D_a \cdot \tau_a)^{0.5} \quad (6)$$

$$D_a = 2 \cdot D_n \cdot D_p / (D_n + D_p) \quad (7)$$

$$D_n = (kT/q) \cdot \mu_n \quad (8)$$

$$D_p = (kT/q) \cdot \mu_p \quad (9)$$

B. Switching Losses

The equations for energy losses, during turn-on and turn-off operations, are shown in (10) and (11) below [8]. During turn-on, it is assumed that the turn-on gain is very high,

$$E_{off} = 1/2 \cdot (\varepsilon_s \cdot E_c V/(1-\alpha_{\overline{npn}}) \sqrt{V/V_B} + J\alpha_{npn,\max} \cdot \tau_a \quad (10)$$

$$E_{on} = 1/3 \cdot \varepsilon_s \cdot E_c V \sqrt{V/V_B} + J^2 \cdot (3\tau_a \cdot V_B^2)/(\varepsilon_s \cdot \mu_n \cdot E_c^3) + (E_g/2q) \cdot J\tau_a \quad (11)$$

hence it can be assumed that the current rise is very fast. During the turn-off period, assuming unity gain turn-off, the energy loss equation is derived as an open base npn transistor turn-off and also assuming that the entire anode current flows to the gate terminal [8].

The switching power losses can be calculated using the total energy loss equation as,

$$P_{switching} = (E_{on} + E_{off}) \cdot f_s \quad (12)$$

The total power loss in the device is given as,

$$P_{total} = P_{conduction} + P_{switching} \quad (13)$$

III. Mobility Model

The loss model equations are dependent on doping densities, mobilities, temperature, and applied voltage and current. For a given operating voltage and current, the model behavior varies with temperature because the electron and hole mobilities vary with temperature. In addition, the doping density is fixed for a desired rating of the device. A temperature dependent mobility model is used in the loss model. The equations used in the mobility model are given in [9] as,

$$\mu_o = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(\frac{N_D + N_A}{N_{ref}}\right)^{\alpha}} \quad (14)$$

where N_A+N_D is the total doping concentration, μ_{max} and μ_{min} are the minimum and maximum mobilities of electrons and holes, N_{ref} is the doping concentration for p-type and n-type materials calculated empirically, and α is the curve fitting parameter measure of how quickly the mobility changes from μ_{min} to μ_{max}.

The temperature dependence of the mobility model can be calculated as,

$$\mu = \mu o * \left(\frac{T}{To}\right)^{\gamma} \quad (15)$$

Table I: Explanation of Symbols

k	Boltzmann constant (J/K)
v_s	electron saturation velocity (cm/s)
V_B	breakdown voltage (V)
D_a	ambipolar diffusion coefficient (cm^2/s)
D_n, D_p	electron and hole diffusion coefficients (cm^2/s)
N	electron concentration (cm^{-3})
q	electron charge (C)
E	electric field (V/cm)
E_c	avalanche breakdown electric field (V/ cm)
E_{on}, E_{off}	turn-on and turn-off losses (J/cm^2)
J	current density (A/cm^2)
L_a, L_n	ambipolar and electron diffusion lengths (cm)
$P_{on\text{-}state}$	on-state losses ($W \cdot cm^{-2}$)
V	applied voltage (V)
$\alpha_{\overline{npn}}$	average current gain during voltage rise
R_{sp}	ideal specific on-state resistance ($ohm \cdot cm^2$)
N_A, N_D	acceptor and donor concentrations (cm^{-3})
$\alpha_{npn,\max}$	maximum common-base current gain for a given applied voltage
α_{npn}	average common-base current gain when applied voltage varies from 0 to V
ε_S	permitivity of the semiconductor (F/cm)
μ_n, μ_p	electron and hole mobility ($cm^2/V \cdot s$)
τ_a	ambipolar carrier lifetime (s)
τ_n, τ_p	electron and hole lifetimes (s)

$$\mu^E(E) = \mu \left(1/(1 + |\mu E / v_S|^{\beta})\right)^{\frac{1}{\beta}} \quad (16)$$

where μ_o is the mobility at room temperature T_o, γ is a constant and varies from -1.8 to -2.5 for n-type and p-type SiC materials, E is the applied electric field, V_s is the saturation velocity, and β is a constant. The data used to calculate the mobilities are given in Table II [9], [10], [11]. Fig. 1 shows the variation in the mobility of the electrons and holes as a function of temperature.

Table II: Parameters Used in Mobility Model

	Si	4H-SiC
Minimum and maximum electron mobility, μ_{minn}, μ_{maxn}, [$cm^2/V \cdot s$]	65, 1360	50, 950
Minimum and maximum hole mobility, μ_{minp}, μ_{maxp} [$cm^2/V \cdot s$]	50, 505	10, 180
Electron and hole ionization coefficients, α_n, α_p	0.91, 0.63	0.76, 0.56
Reference electron and hole concentrations, N_{refn}, N_{refp} [cm^{-3}]	8.5e16, 6.3e16	2.2e17, 2.35e17

IV. Simulations

The SiC GTO thyristor is doped for a desired breakdown voltage $V_B = \varepsilon(N_a + N_d) \cdot E_c^2/(2q \cdot N_a \cdot N_d)$ [12] and is rated at

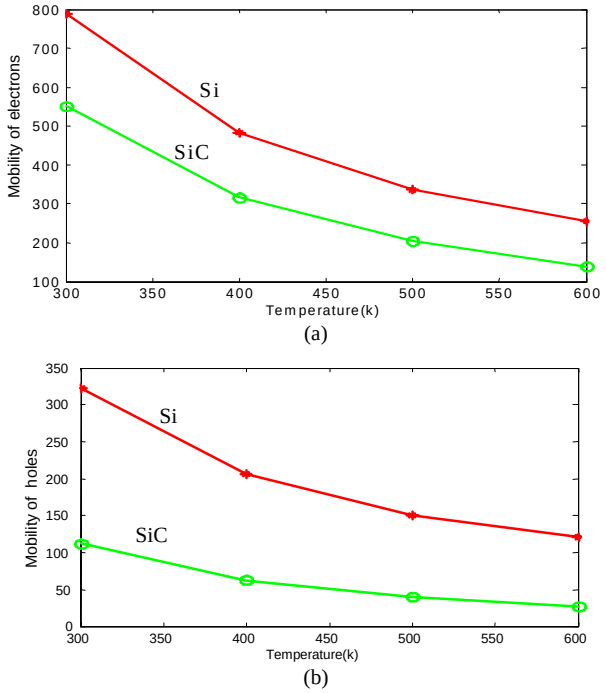

Fig. 1. Mobility calculation of (a) electrons and (b) holes for Si and SiC.

20 kV. The Si GTO thyristor is rated at 5000V, and for comparison, four Si devices are assumed to be connected in series to achieve the same required voltage-blocking rating. The model is studied for variation in temperature for different current and voltage ratings. The frequency of operation is 1 kHz and the model was tested for a temperature range of 300 K – 600 K. It should be noted that the Si GTO thyristor cannot withstand more than 423 K; however, the model is tested at elevated temperatures for comparison purposes. The devices are subjected to a current density range of 100 A/cm^2 – 500 A/cm^2 and the duty cycle is assumed to be 50%. The data used in simulation is shown in Table III [13].

Table III. Simulation Data

Parameter	4H-SiC	Si
(E_g), Energy gap (eV)	3.2	1.11
ε_r, relative permitivity	9.7	11.8
E_c, critical electric field (V/cm)	2.3e06	0.3e06
$V_{sat,}$ saturation velocity (cm/s)	2e07	1e07

A comparison plot of different losses of Si and SiC devices is shown in Fig. 2. Conduction losses dominate because at lower switching frequency the switching losses are low, and the main power loss is a function of on-state resistance. Si GTO thyristor conduction losses are more than the SiC GTO thyristor conduction losses, primarily because of the difference in the on-state specific resistance. It is found that the conduction losses of the Si GTO thyristor are at least double that for the SiC device. The switching losses of SiC GTO thyristor are at least 12 times less than the Si device. This noticeable difference between the switching losses of Si and SiC devices is mainly because for the same blocking voltage, the thickness of the blocking layer in a Si device is more than that of a SiC device. The thinner blocking layer

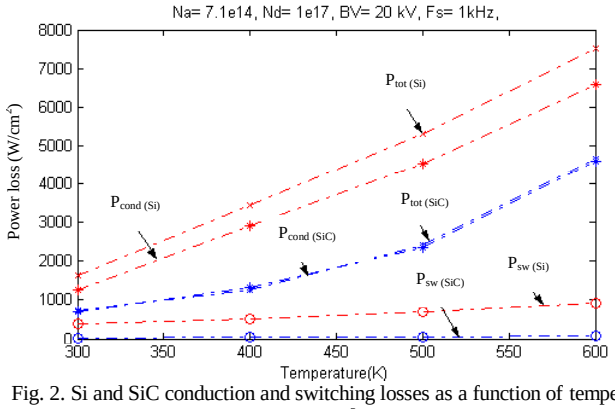

Fig. 2. Si and SiC conduction and switching losses as a function of temperature for J=200 A/cm^2, V= 5000V.

thickness in SiC devices is because of the higher electric breakdown strength of SiC material due to wide bandgap. Thus, the charge stored in the drift region is less, which results in faster switching. The lower conduction and switching losses of SiC devices show that they have high efficiencies compared to Si devices.

V. HVDC System

The configuration chosen for the study is a monopolar configuration, and the transmission system is based on voltage source converter technology. The converters at both ends are voltage source converters also known as forced commutated converters. The converter configuration is a two-level, six-pulse three-phase full bridge converter, and the arrangement is as shown in Fig. 3. The system model is designed to

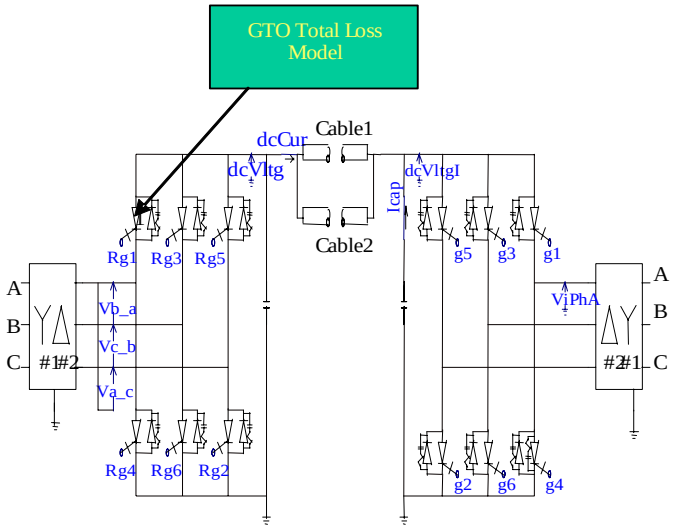

Fig. 3. SIMULINK interface with PSCAD/EMTDC.

emulate the ac characteristics, and it is assumed that one substation is the sending end and the other is the receiving end.

A. Simulation Specifications

- System ratings: 120 kV dc link, up to 75 MW delivered to the receiving end.
- Device ratings: SiC– 20kV, 200 A/cm^2; Si– 5kV, 200 A/cm^2

- Number of devices: The maximum voltage and current ratings for the HVDC system are 120kV, 1000 A. To achieve this rating with SiC devices 5 parallel strings of 6 devices in series (20kV, 200A device) were used. With Si devices 5 parallel strings of 24 devices in series (5kV, 200A device) were used.
- The model is tested for a temperature range of 27^o – 200^oC. The maximum value of 200^oC was chosen to evaluate the SiC device losses above the maximum operating temperature (150^oC) of Si device.
- Simulation is initialized using steady state operating values.
- The system frequency is 60 Hz and the GTO thyristor switching frequency is 2 kHz.

B. System Simulations

The system model described in earlier sections and the control systems have been implemented using PSCAD/EMTDC software. PSCAD/EMTDC is a simulation tool for analyzing power systems. PSCAD is the graphical user interface and EMTDC is the simulation engine. This software is most suitable for simulating the electromagnetic transients of the electrical systems. It also has the feature of interfacing MATLAB/SIMULINK, and hence has the flexibility of interfacing various MATLAB/SIMULINK models. The device models, which were discussed in the earlier sections, have been interfaced with the HVDC system model. This system model has been developed for the specifications listed in the previous section. A program was written in FORTRAN 99 to interface the SIMULINK device models.

VI. RESULTS

The power loss profiles obtained from simulation at 150^oC are presented in Fig. 4 and Fig. 5. The losses are a function of the conduction current and vary proportionally with the square of current. The current flows through the diode when there is a power reversal, and the current through the GTO thyristor is zero. The conduction losses are found to be dominant, similar to the device simulations discussed in the earlier sections. This is because the switching frequency is low and thus the switching losses are less compared to the conduction losses. However, for the same switching frequency, the losses are more for a Si GTO thyristor than a SiC GTO thyristor. The total loss of SiC GTO thyristor is less than Si GTO thyristor as expected, since the on-state resistance of Si GTO thyristor is more than that of a SiC GTO thyristor. The losses increase with an increase in temperature due to the increase in on-state resistance. However, Si GTO thyristor's losses increase more than those of SiC GTO thyristor. The loss profiles were used to calculate the system efficiency and system cost savings.

A. Efficiency Calculation

The efficiency is calculated based on the power loss profile obtained at different operating conditions. The instantaneous losses are a function of the instantaneous current. The

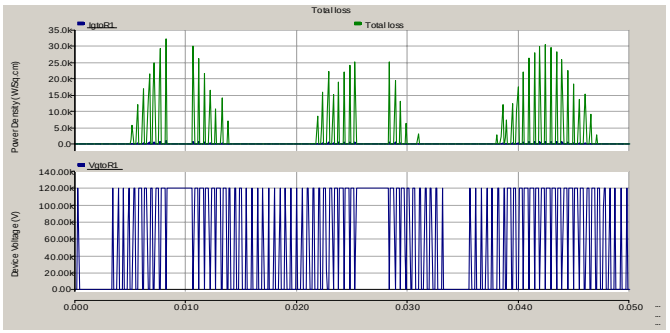

Fig. 4. Loss profile for SiC GTO (423 K).

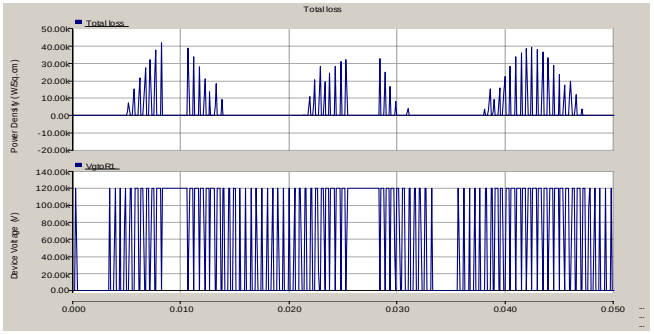

Fig. 5. Loss profile for Si GTO (423 K).

instantaneous current depends on the modulation index and the switching angles generated by the PWM-based controller. The average loss over a few cycles of the fundamental is calculated to find the cyclic power loss (average power loss per cycle of the output voltage). The plots of average power loss for Si GTO thyristor and SiC GTO thyristor are shown in Fig. 6 and Fig.7. The power loss is different for each cycle as the conduction current duty cycle varies. The maximum and minimum power loss for a single device over a few cycles is measured from the plots, and the corresponding converter controlled switches' efficiency (efficiency of the converter's GTO thyristors excluding the antiparallel diodes) is calculated. The efficiency calculations are based on the dc power in the dc link, average loss in the devices, and the number of devices in the converter.

$$\text{Maximum efficiency} = (P_{dc} - P_{loss(min)})/ P_{dc} \quad (17)$$

$$P_{loss(min)} = P_{min} \cdot (n_t) \quad (18)$$

$$\text{Minimum efficiency} = (P_{dc} - P_{loss(max)})/ P_{dc} \quad (19)$$

$$P_{loss(max)} = P_{max} \cdot (n_t) \quad (20)$$

Total number of devices

$$n_t = (n_v)\,(n_c) \cdot 6 \quad (21)$$

Where,

P_{min}, P_{max}, are the average minimum and maximum losses of a single device calculated from the cyclic power loss plots. $P_{loss(min)}$, $P_{loss(max)}$, are the total minimum and maximum losses of the converter. n_t is the total number devices in the

converter. n_v, is the number of devices in series, and n_c, is the number of devices in parallel.

Tables IV and V show the maximum and minimum efficiencies of a Si GTO thyristor rated at 5kV, 200 A/cm^2 and SiC GTO thyristor rated at 20 kV, 200 A/cm^2. Fig. 8 shows the efficiency plot for a Si SiC GTO thyristors. The range of efficiency for SiC converter is higher than Si converter because of the lesser number of devices and also lesser average power loss per SiC GTO thyristor.

It can also be seen from the plot that at 27^{o}C the efficiency is almost the same for the Si and SiC converters. However, at higher temperatures the efficiency of the Si GTO thyristors drops down, but the efficiency of the SiC GTO thyristors is still high. This illustrates that SiC devices can operate efficiently at high temperatures.

Table IV. Efficiency of Si GTO Thyristor

Temp (K)	P_{max}	P_{min}	Max.eff %	Min.eff %
300	433.3	262.7	99.68	99.48
373	1443.1	873.7	98.75	98.26
423	3041.2	1842.4	97.78	96.35
473	6301.9	3818.9	95.41	92.43

Table V. Efficiency of SiC GTO Thyristor

Temp (K)	P_{max}	P_{min}	Max.eff %	Min.eff %
300	475.2	300.6	99.9	99.85
373	1245.6	771.8	99.76	99.62
423	2402.1	1472.8	99.55	99.77
473	4506.9	2749.3	99.17	98.64

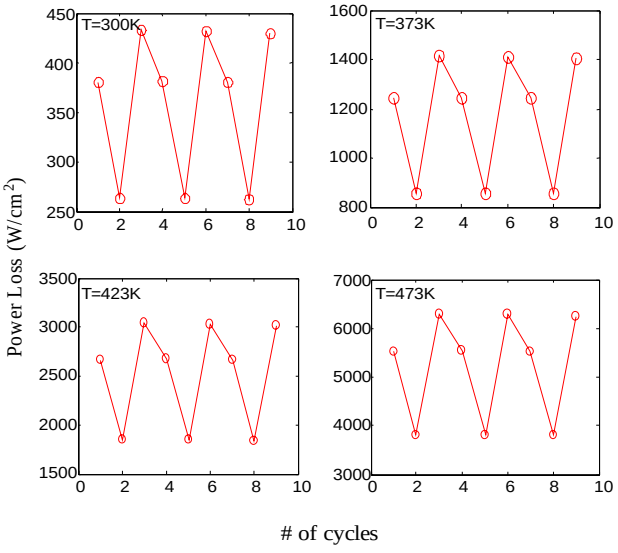

Fig. 6. Cyclic power loss plots for 5 kV, 200 A/cm^2 Si GTO Thyristor.

B. System Cost

The system cost savings is calculated based on the power loss profile obtained for different operating conditions. The cost savings was calculated for different ratings of the devices at 100^{o}C.

Savings Calculation:

Difference in losses,

$$\Delta P_{loss} = (P_{(loss,\ Si)} \times n_t) - (P_{(loss,\ SiC)} \times n_t) \quad (22)$$

Converter operates for 365 days/year and 24 hours/day:

Difference in energy loss/year,

$$\Delta E_{loss}/yr = \Delta P_{loss} \times 365 \times 24 \quad (23)$$

Assuming a rate of \$0.04/ kW·hr:

$$\text{Savings/year} = (\Delta E_{loss}/yr) \cdot (\$0.04) \quad (24)$$

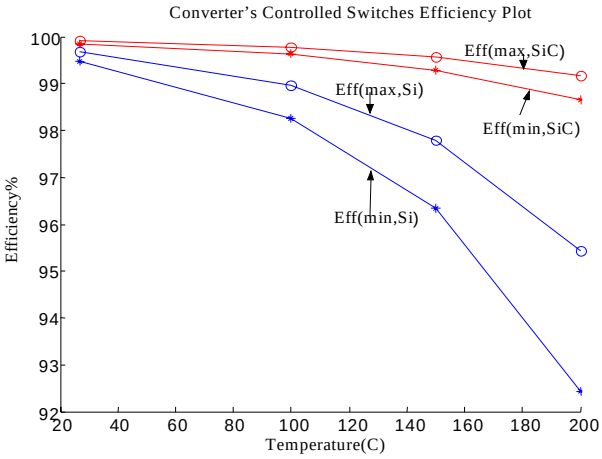

Fig. 8. Converter's controlled switches efficiency plot.

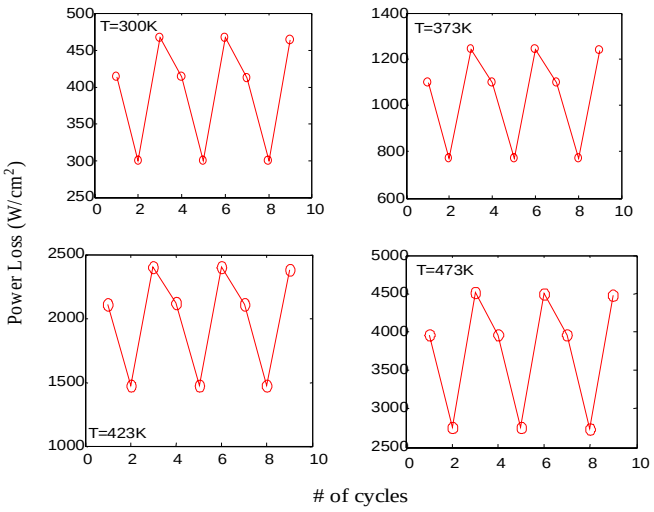

Fig. 7. Cyclic power loss plots for 20kV, 200 A/cm^2 SiC GTO Thyristor.

Table VI gives the maximum and minimum cost savings for a converter using a SiC-based converter with 20 kV, 200 A/cm^2 GTOs instead of 5 kV, 200 A/cm^2 Si GTOs. As seen in table VI using SiC GTO thyristor, rated at 20kV, 200 A/cm^2, result in significant system cost savings over a year. The number of Si devices used to achieve the system power rating is 720 and the number of SiC devices used is 180.

Table VI. Cost Savings due to SiC GTO thyristors replacing Si GTO thyristors

	Average Losses	kW-hr/year	Cost Savings
Max. savings	814.824 kW	7,137,858.24	\$ 285,514.3
Min. savings	490.14 kW	4,293,626.4	\$ 171,745.6

The ratio of number of devices in a SiC converter compared to a Si converter is less because SiC GTO thyristors have a higher voltage rating than their Si counterparts. Thus, the reduction in number of devices results is cost savings, and one can afford to pay more for a SiC GTO thyristor. With a less number of devices, less auxiliary components like snubber circuit, reactors, and capacitors required and the installation costs will be less. Hence, the overall system cost will be reduced. The complexity of the system control is also reduced to a great extent with the reduction in number of devices.

It was also shown in the previous section that the efficiency of a converter with SiC GTO thyristor rated at 20kV, 200 A/cm^2 is higher compared to a Si-based converter. This illustrates that the higher rating of a SiC GTO thyristor results in the better performance of the system.

VII. Conclusions

SiC devices can withstand high temperatures, more than 150^{o}C, and since they have lower losses are also less, thermal management requirements, such as heat sink size, can be greatly reduced. Additionally, the device operating area limits can be improved due to reduced losses; hence, the maximum switching frequency can be increased for a given current density and operating voltage. The higher switching frequency results in improved dynamic characteristics of the system.

The use of VSC in high power transmission application is restricted mainly because of the high converter losses, which make the system highly inefficient. Even though advanced technologies like multilevel converters have been developed, the efficiency improvement is not enough considering the increased complexity. However, using SiC devices, overall losses can be reduced. Currently, system manufacturers face the challenge of reducing the operating cost of the system and hence demand devices with higher current and voltage ratings. It was shown in this study that by using high voltage rated SiC GTO thyristors the system savings are improved. Instead of several Si GTO thyristors in series and parallel, fewer SiC devices can be employed for the same power rating. Hence, it can be concluded that once SiC devices become commercially available, they can effectively replace the conventional Si based thyristor converters.

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Biographies

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