Multi-Level DC/DC Power Conversion System with Multiple DC Sources

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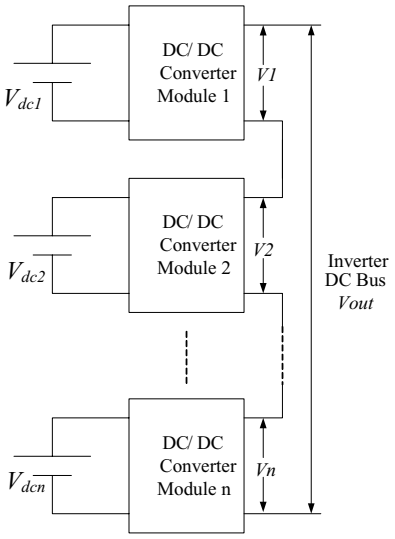
Abstract: **A multilevel dc/dc power conversion system with multiple dc sources is proposed in this paper. With this conversion system, the output voltage can be changed almost continuously without any magnetic components. With this magnetic-less system, very high temperature operation is possible. Power loss and efficiency analysis is provided in the paper. Comparison results show that the system does not require more semiconductors or capacitance than the traditional boost converter. Experimental results are provided to confirm the analysis and control concept.**

I. Introduction

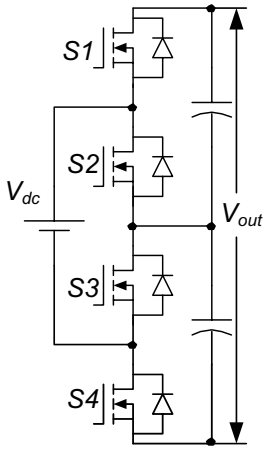
Traditional dc/dc converters require at least one inductive component, which is bulky, heavy, and costly. With the technology advancement of the silicon carbide (SiC) devices and ceramic capacitors, very high temperature components (above 250°C) will be available except magnetic cores. Thus very high temperature operation of magnetic-less converter become possible and very attractive because natural air cooling can be adopted, which will reduce the size, weight, and the cost of the converter significantly. The multi-level dc/dc converter [1-9] becomes a good candidate for this application, because there are no magnetic components necessary, and also because of its bi-directional nature. Traditional multi-level dc/dc converters usually output a fixed voltage for a given input voltage, this may become a drawback of these converters because for some applications, such as hybrid vehicles, a variable dc bus voltage is preferable so that the inverter can always be operated in its most efficient dc voltage. In this paper, a bi-directional multi-level dc/dc conversion system that can output variable voltage with multiple dc sources will be proposed.

II. Description of the Dc/Dc Conversion System

The proposed dc/dc conversion system is shown in Fig.1 (a), where there are n isolated dc sources, V_{dc1}~V_{dcn}, and n identical dc/dc converters cells with the output connected in series. One possible application of this topology is hybrid electric vehicles, instead of connecting all batteries in series as one power source and a bi-directional boost converter to interface the battery and the dc bus, one can use separate batteries to power separate converter modules and connect the output of the modules in series as a dc bus supplying the inverter. The dc/dc converter cell is shown in Fig.1 (b), which is a two level converter.



(a) Dc/dc power converter system configuration



(b) Topology of the dc/dc converter module

Fig. 1. Dc/dc power conversion system configuration and converter cell topology.

For each dc/dc converter cell as shown in Fig. 1 (b), there are three switching states as illustrated in Fig. 2.

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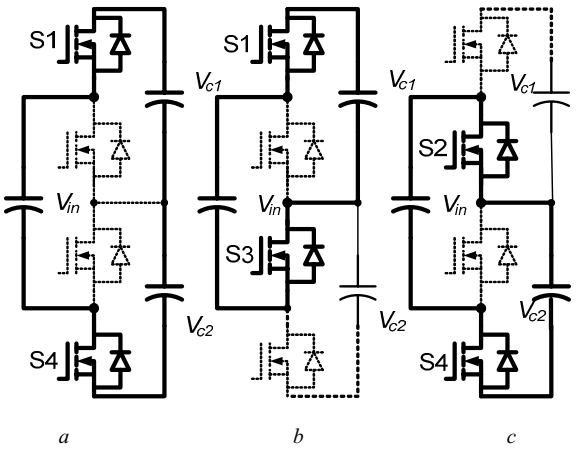


Fig. 2. Converter switching states.

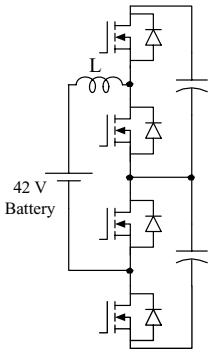


Fig. 3. Converter with small inductance.

With these three switching states, the converter is able to output two different voltages. When the converter is in switching state *a*, (switches S1 and S4 are on, S2 and S3 are off), the following equation will be met,

$$V_{out} = V_{in}. \tag{1}$$

Obviously, when the switches (MOSFETs or IGBTs with free wheeling diodes) are turned on, the current can flow in either direction, so the converter is a bidirectional converter.

In the second mode, the converter alternates its switching states between *b* and *c* complementarily with 50% duty ratio for each switching state at a high frequency, the following equations will be met

$$V_{c1} = V_{in}, \quad V_{c2} = V_{in} \tag{2}$$

Thus the output voltage is $V_{out} = 2V_{in}$. Also, the converter is bi-directional in this mode.

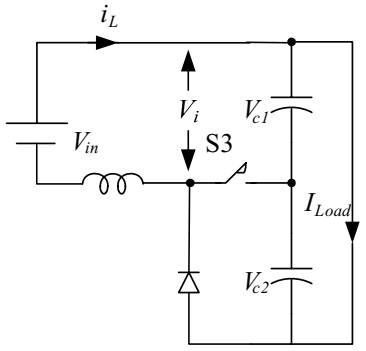
Therefore, each single module is able to output two different voltages: V_{in} or $2*V_{in}$. For a system that consists of *n* cells, the system is able to output *n+1* different voltages from $n*V_{in}$ to $2*n*Vin$ with step of V_{in}, when the number of *n* increases, the output voltage can be considered as almost continuous and the inverter fed by the dc/dc converter can always operate close to the optimum voltage point.

III. Converter Control During Transition

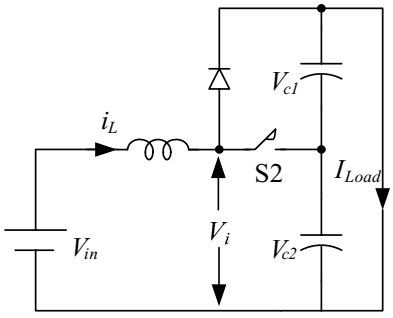
In steady state, the voltage difference between the battery and the capacitors being charged/discharged is very small, therefore the current through the switches is well limited. During transition when one wants to change the output voltage between V_{in} and $2*V_{in}$, the voltage difference between the two could be relatively large, which might result in high transient current. To limit the current, a small inductor as shown in Fig. 3 is considered, the requirement of the inductance is very small (<1uH) as will be shown in the later section, it can be considered as the parasitic inductance of the cable and the ESL of the capacitor on the battery side. Usually it would be large enough especially for hybrid electric vehicles if the battery is not placed adjacent to the converter.

a. Change the output voltage from V_{in} to $2*V_{in}$

Before the output voltage is changed to $2V_{in}$, the capacitor voltage, V_c, equals to half of the battery voltage. In this transition, the two capacitors will be charged up from half input voltage to full input voltage, thus input current will be higher when the battery is outputting power during the transition comparing with when charging the battery. Therefore, the battery is assumed to be outputting current during the transition as the condition is more critical. When the transition starts, the converter starts to get into switching states *b* and *c*, the equivalent circuit when charging C1 and C2 are shown in Fig. 4 (a) and (b) respectively.



(a)



(b)

Fig. 4. The equivalent circuit of switching states (b) and (c).

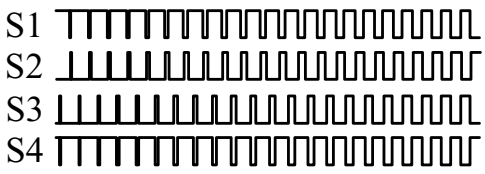


Fig.5. Control signals during output voltage transient from V_{in} to $2*V_{in}$.

In the transition, the battery is charging the two capacitors equally. Fig. 4 (a) and (b) each shows half of the operation condition. In each condition, there are two switching states: the switch (S2 or S3) is on or the switch is off. When the switch is on, V_i equals to one capacitor voltage; when it is off, it equals to the sum of the two capacitor voltages because of the freewheeling. Thus the effect the switching state when S2 is turned on is the same as the state when S3 is turned on in terms of inductor current. Defining the duty ratio, D, as the sum of the duty ratio of S3 and S2 and assuming that the inductor current is in continuous mode, in steady state, the relationship of the capacitor voltage and the input voltage is

$$V_{in} = \overline{V_i} = DV_c + (1-D) \times 2V_c = (2-D)V_c \tag{3}$$

From above equation, the duty ratio should be gradually increased from 0 to 1 in order to increase the capacitor voltage from $V_{in}/2$ to V_{in} gradually. As a result, the switching signals shown in Fig. 5 are required to control the switches. S2 and S3 show the actual duty cycle, which is half of D, S1 and S4 are inverted signals of S2 and S3, respectively.

b. Change the output voltage from 2 V_{in} to 1 V_{in}

Before changing the output voltage from $2*V_{in}$ to V_{in}, the capacitor voltage equals to battery voltage. The capacitor voltage will be discharged from the battery voltage to half of it, thus the transition is more critical when the battery is being charged by the load. The equivalent circuit of switching state *a* is shown in Fig. 6. When the switch is turned on, S1 and S4 are turned on in the actual circuit. When these two switches are on, V_i equals to twice of the capacitor voltage, otherwise V_i equals to zero due to freewheeling. Assuming the duty ratio is D, the relationship of the voltages and the duty ratio for continuous current condition is

$$V_{in} = 2DV_c . \tag{4}$$

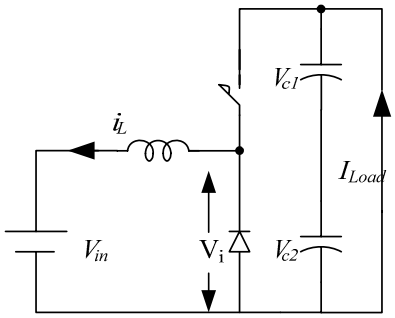


Fig. 6. Equivalent circuit for switching state (*a).*

As a result, the duty ratio should change from 0.5 to 1 gradually to control the capacitor voltage from V_{in} to $V_{in}/2$ as shown in Fig.7. S2 and S3 are inverted signals of S1 and S4.

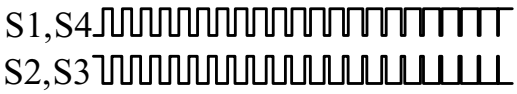


Fig. 7. Control signals during output voltage transient from $2V_{in}$ to V_{in}.

When the switching frequency is relatively low, using the above method may not be sufficient enough to limit the peak current because the current change in one cycle can be relatively big due to small inductance. To further suppress the peak current during transient, a higher switching frequency may be used during the transition.

IV. Output Voltage Loss

When outputting 2*Vin, dead time has to be implemented in order to prevent shoot through. Assume that the input current is continuous because of the small parasitic inductor, and the duty cycle is D (the percentage of time the input is connected to either of the capacitors). When the input is connected to one of the capacitors, the voltage across the parasitic inductor is

$$V_L = V_{in} - V_c \quad . \tag{5}$$

During the dead time, if the battery is outputting power to the load, the current flows through the freewheeling diodes of S1 and S4 to charge both capacitors, the voltage across the inductor is

$$V_L = V_{in} - 2V_c . \tag{6}$$

If the battery is being charged from the load side, the current flows through the freewheeling diodes of S2 and S3, and the voltage across the inductor is

$$V_L = V_{in} . \tag{7}$$

Thus the steady state output voltage differs by the direction of the power flow. When the battery is powering the load, the output voltage is

$$V_{out} = \frac{2V_{in}}{2-D} . \tag{8}$$

The output voltage when the battery is being charged by the load is

$$V_{out} = \frac{2V_{in}}{D} . \tag{9}$$

Thus the output voltage could be slightly different depending on the power flow direction and dead time. Also the voltage drop across the switches should be included.

V. Power Loss Analysis

In previous literature [1-3], the power loss of this type of converters is analyzed. In the literatures, the parasitic inductance is not considered and the RC constant of the converter is always comparable to the switching period to achieve high efficiency. When considering the small parasitic inductance, results differ. When the input is connected to one of the capacitors, the equivalent circuits with and without considering the parasitic inductor are shown in Fig. 8(a), where I_{Load} is the load current. When there is no inductance, the current can be expressed by the following equation,

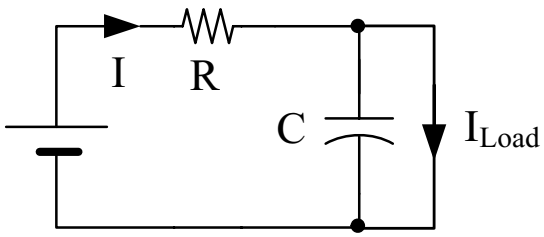
$$i(t) = \frac{V_0}{R} e^{-\frac{t}{RC}} + I_{Load}, \qquad (10)$$

where V_0 is the initial voltage difference between the voltage source and the voltage across the capacitor. The current waveform is shown in Fig. 9, the shaded area corresponds to the average input current.

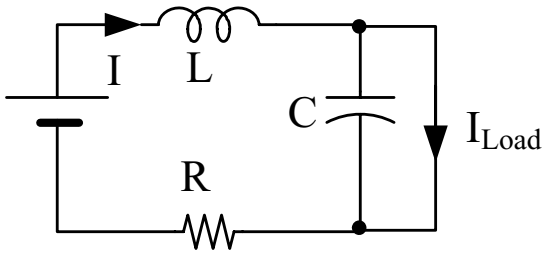
When considering the parasitic inductor, the input current is

$$\begin{aligned} i(t) &= I_{Load} + I_0 e^{-\frac{R}{2L}t} \cos\left(\sqrt{\frac{1}{LC} + \left(\frac{R}{2L}\right)^2}\, t\right) \\ &+ \frac{V_0 - \frac{RI_0}{2}}{\sqrt{\frac{L}{C} - \left(\frac{R}{2}\right)^2}} e^{-\frac{R}{2L}t} \sin\left(\sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}\, t\right) \qquad (11) \\ &= I_{Load} + f(I_0, V_0) e^{-\frac{R}{2L}t} \sin\left(\sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}\, t + \varphi(I_0, V_0)\right) \end{aligned}$$

where I_{Load}+I_0 and V_0 are the initial current and initial voltage difference between the input voltage and capacitor. Another feature of this case is that the initial current and the current when the switch turns off are the same because the converter repeats the same process with the other capacitor after it finishes charging one capacitor. Thus the input current is shown in Fig. 9 with the initial current equal to the current at the end of the process, the shaded area corresponds to the average input current.



(a)



(b)

Fig. 8. Equivalent circuit with and without the parasitic inductance.

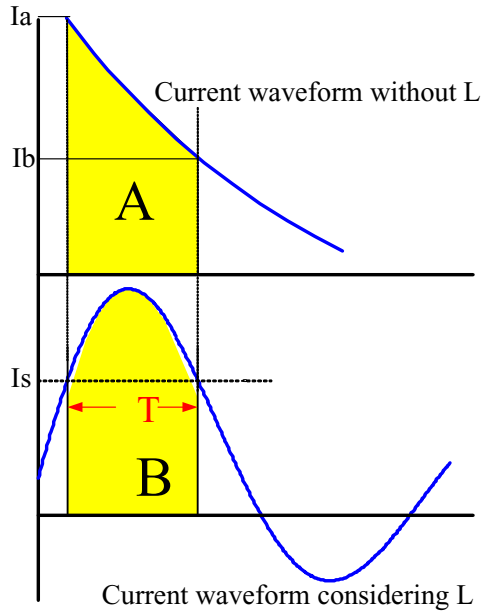


Fig. 9. Input current of the converter with and without parasitic inductance.

For a fixed output power and given input voltage, the average input current is fixed (area A should equal to area B for the same power and voltage), different inductance results in different input current shape, which further results in different input current rms value. The conduction loss of the circuit is directly proportional to the square of the rms value assuming MOSFETs are used as the switches. Based on the above equations, one can easily numerically calculate the ratio of rms current over the average current based on the different parameters, and from which the loss can be calculated. As an example, Fig. 10 shows the normalized conduction loss of a converter with different parasitic inductances, the other parameters of the converter are: R_{ds}on (MOSFET on resistance) = 1 mohm, C (capacitance of each capacitor) = 1 mF, f_s (switching frequency) = 5 kHz. The normalized loss with no parasitic inductance is 7.0. From which we can see that the conduction loss is dramatically reduced with a small parasitic inductance.

The switching loss is directly proportional to the switching current given the fixed converter voltage. It is noteworthy that half of the switching actions in this converter is zero voltage switching due to the current freewheeling

through the body diodes during the dead time. The switching current is the initial and ending current, I_a, I_b, and I_s, shown in Fig. 9. Fig. 11 shows the switching current normalized by the average current for the same converter versus different parasitic inductances. From Fig. 11, the switching current reduces as the parasitic inductance reduces until it reaches the resonant point with 0.6 μH and then increases again with further reducing of the inductance. The normalized switching current of the system without any parasitic inductance is 26.

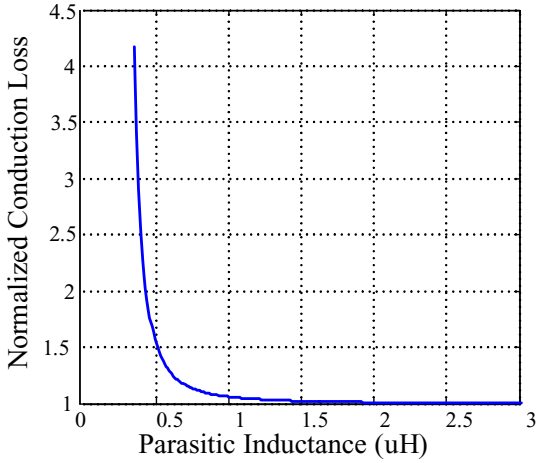


Fig. 10. Normalized conduction loss versus L

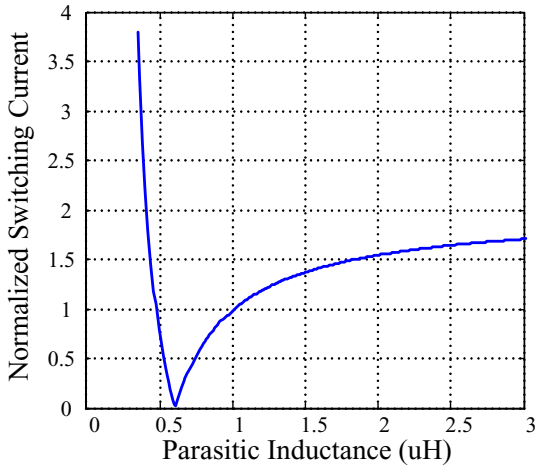


Fig. 11 Normalized switching current versus L.

With small amount of parasitic inductance, both conduction loss and switching loss are reduced significantly compared to the system with zero inductance. In previous literature [1-3], the capacitance has to be relatively large so that the time constant of RC is comparable to switching period to keep high efficiency. In other words, the converter's capacitance requirement is dramatically reduced with small parasitic inductance.

VI. Cost Comparison with Traditional Converter

To compare the cost of the converter with the traditional bi-directional boost converter, the semiconductor VA rating and the capacitor current capability are compared. Define the semiconductor VA rating as the product of the average current that flows through the device and the maximum voltage across it. For a traditional bi-directional boost converter, the sum of the VA rating of the two switches is

$$VA_{traditional} = V_{out} * I_{in}\,, \tag{12}$$

where V_{out} is the output voltage and I_{in} is the input average current.

For the proposed converter, there are four switches and each of them sustains half of the output voltage and conveys the input current during half of the time, thus the total VA rating is

$$VA_{proposed} = 4 * \frac{V_{out}}{2} * \frac{I_{in}}{2} = V_{out} * I_{in}\,. \tag{13}$$

Therefore the total VA ratings of the semiconductors are the same for both cases.

To compare the capacitor requirement, the traditional boost converter is assumed to be operated with duty ratio of 50%, so that the boost ratio is the same as the proposed converter. Under this condition, the capacitor current is square wave and with an rms value of half of the input current assuming that the input current is constant for both cases. Therefore, the capacitor current is the same. One capacitor sustaining whole output voltage is used in traditional boost converter, while 2 capacitors each sustaining half of the output voltage are used in the proposed converter. Thus the total capacitor requirement is roughly the same. In the proposed topology, one of the capacitors is being charged while the other is being discharged, therefore the output voltage ripple is much smaller than the traditional boost converter for the same capacitance because of the cancellation of the ripple across each capacitor. This results in lower capacitance requirement than the traditional boost converter for the same output voltage ripple requirement.

VII. Experimental Results

To verify the concept, a 10 kW dc/dc converter shown in Fig. 12 has been built. The switches used are MOSFET module FM600TU-07A, 1 mF film capacitors are used for both capacitors C1 and C2. The converter operates at 5kHz for steady state operation when outputting 2 Vin, and it operates at 50 kHz during the 15-ms transition between 1 Vin to 2 Vin to limit the transient current. No extra inductor is used and the battery is connected to the converter from a foot away.

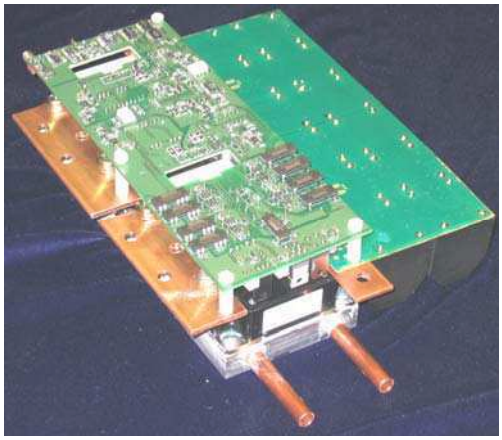
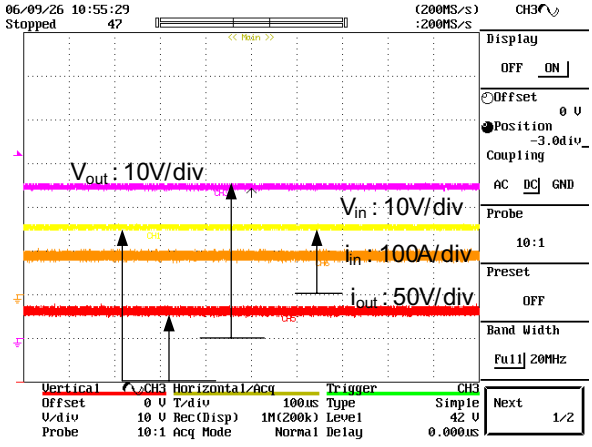
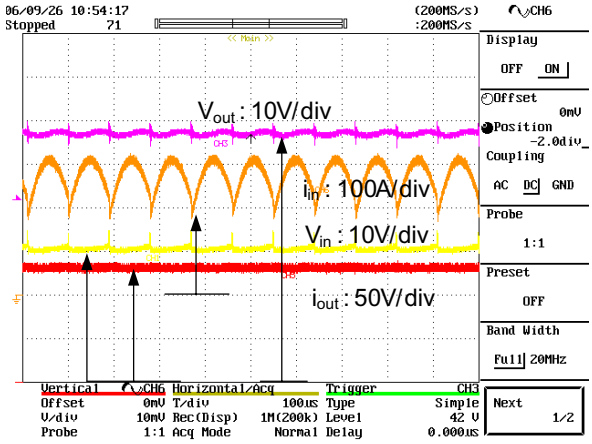


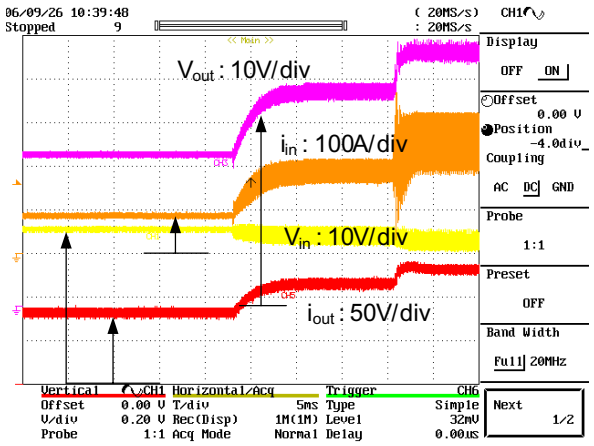
Fig. 12. The dc/dc converter module.



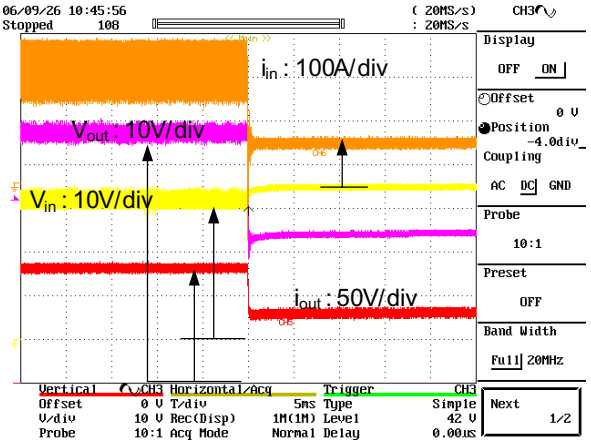
(a) Steady state waveform when outputting 1Vin



(b) Steady state waveform when outputting 2Vin



(c) Transition from 1Vin to 2Vin

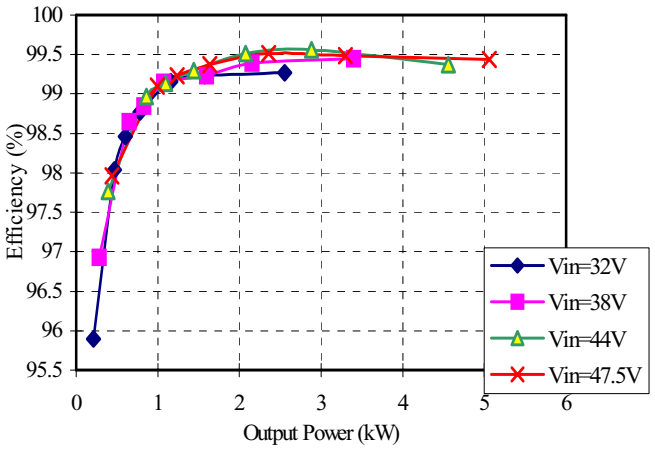


(d) Transition from 2Vin to 1Vin

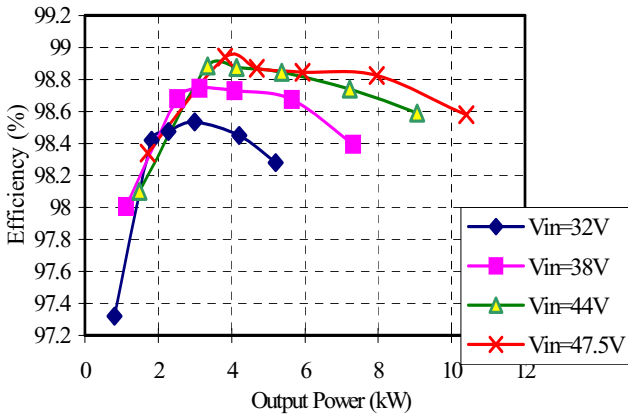
Fig. 13 Experimental results of the converter, 1Vin means the output voltage equals to input voltage, 2Vin means the output voltage is twice of the input voltage.

Fig. 13 (a) shows the input and output current/voltage when outputting $1V_{in}$. Fig. 13(b) shows the same waveforms when outputting $2V_{in}$. As can be seen from the results that the input current is continuous and has exactly the same shape as depicted in Fig. 9. Also, it is noteworthy that the output voltage does not quite reach twice of the input voltage, which is caused by the voltage loss across the switches and dead time. Fig. 13(c) and (d) shows the transition between 1 V_{in} and 2 V_{in}. As can be seen from the results, the current is well regulated during steady state operation and well limited during the transition. The transition time is only 15 ms.

The converter efficiency is measured at different input voltages and different powers as shown in Fig. 14. As can be seen from the figure, the efficiency is quite high. The reduction of the efficiency at low power is mainly because of the control and gate drive power becomes significant in terms of percentage at low power.



(a) when outputting 1Vin



(b) when outputting 2Vin

Fig. 14. Measured efficiency

VIII. Conclusion

In this paper, a multi-level dc/dc conversion system with multiple dc sources is proposed. Circuit analysis and control are presented. The power loss of the converter is analyzed, the analysis shows that a small amount of parasitic inductance reduces the power loss dramatically and reduces the capacitance requirement significantly. Also, the requirement of semiconductor and capacitor of the converter is compared with the traditional boost converter, the comparison shows that the proposed converter requires no more semiconductors or capacitance. Experimental results are provided to confirm the functionality without any extra inductors. With the help of parasitic inductance of the connection cable, the current during transition is well regulated. The requirement of the parasitic inductance can be further reduced by increasing the switching frequency during transition time. The high efficiency nature is proved by experimental results. This topology provides the potential for high temperature operation of dc/dc converters.

Acknowledgment

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