

# Modulation Extension Control of Hybrid Cascaded H-bridge Multilevel Converters with 7-level Fundamental Frequency Switching Scheme

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**Abstract**—This paper presents a modulation extension control algorithm for hybrid cascaded H-bridge multilevel converters. The hybrid cascaded H-bridge multilevel motor drive using only a single DC source for each phase is promising for high power motor drive applications since it can greatly decrease the number of required DC power supplies, has high quality output power due to its high number of output levels, and has high conversion efficiency and low thermal stress by using fundamental frequency switching scheme. But one disadvantage of the 7-level fundamental frequency switching scheme is that its modulation index range is too narrow when capacitor's voltage balance is maintained. The proposed modulation extension control algorithm can greatly increase capacitors' charging time and decrease the capacitors' discharging time by injecting triplen harmonics to extend the modulation index range of the hybrid cascaded H-bridge multilevel converters.

## I. INTRODUCTION

The multilevel converter is a promising power electronics topology for high power motor drive applications because of its low electromagnetic interference (EMI) and high efficiency with low frequency control method [1-5]. Among the multilevel converter topologies, the cascaded multilevel converter with separate DC sources closely fits the needs of all-electric vehicles because it can use the onboard batteries or fuel cells to generate a sinusoidal voltage waveform to drive the main vehicle traction motor.

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Traditionally, each phase of a cascaded multilevel converter requires  $n$  DC sources for  $2n + 1$  levels. For many applications, to get many separate DC sources is difficult, and too many DC sources will require many long cables and could lead to voltage unbalance among the DC sources. To reduce the number of DC sources required when the cascaded H-bridge multilevel converter is applied to a motor drive, hybrid cascaded multilevel converter has been proposed which only uses a single DC source for each phase. This hybrid cascaded multilevel converter has the advantages of higher speeds with a low switching frequency (especially useful for electric/hybrid electric vehicle applications), which has inherent low switching losses and high conversion efficiency [6-7].

However, one disadvantage of the hybrid cascaded multilevel converter is that it has narrow modulation index range when using fundamental frequency switching scheme at high modulation index, and this disadvantage limits its highest output voltage when maintaining the capacitors' voltages. To conquer this problem, this paper proposes a modulation extension control algorithm to extend the modulation index range for hybrid cascaded H-bridge multilevel converters. The reason for narrow modulation index range is from longer discharging time and shorter charging time when the hybrid cascaded multilevel converter outputs high voltages. The new proposed modulation extension control algorithm can greatly increase capacitors' charging time and decrease the capacitors' discharging time by injecting triplen harmonics to extend the modulation index range of the hybrid cascaded H-bridge multilevel converters. Therefore, the proposed modulation extension control algorithm has not only wider modulation index range but also all the advantages of inherent high output power quality, low output switching frequency, high conversion efficiency, and high speed capability. This control scheme especially fits fuel cell vehicle motor drive applications. Simulation and experiments verified the proposed control algorithm with the desired features.

## II. CONTROL OF HYBRID CASCADED H-BRIDGE MULTILEVEL CONVERTER WITH 7-LEVEL OUTPUT VOLTAGE

A 7-level hybrid cascaded H-bridge multilevel converter has two H-bridges for each phase, one H-bridge is connected to a DC source, another H-bridge is connected to a capacitor as shown in Fig. 1. The DC source for the first H-bridge ( $H_1$ ) could be a battery or fuel cell with an output voltage of  $V_{dc}$ , and the DC source for the second H-bridge ( $H_2$ ) is the capacitor voltage to be held at  $V_c$ . The output voltage of the first H-bridge is denoted by  $v_1$ , and the output of the second H-bridge is denoted by  $v_2$  so that the output voltage of the cascaded multilevel converter is

$$v(t) = v_1(t) + v_2(t) \quad (1)$$

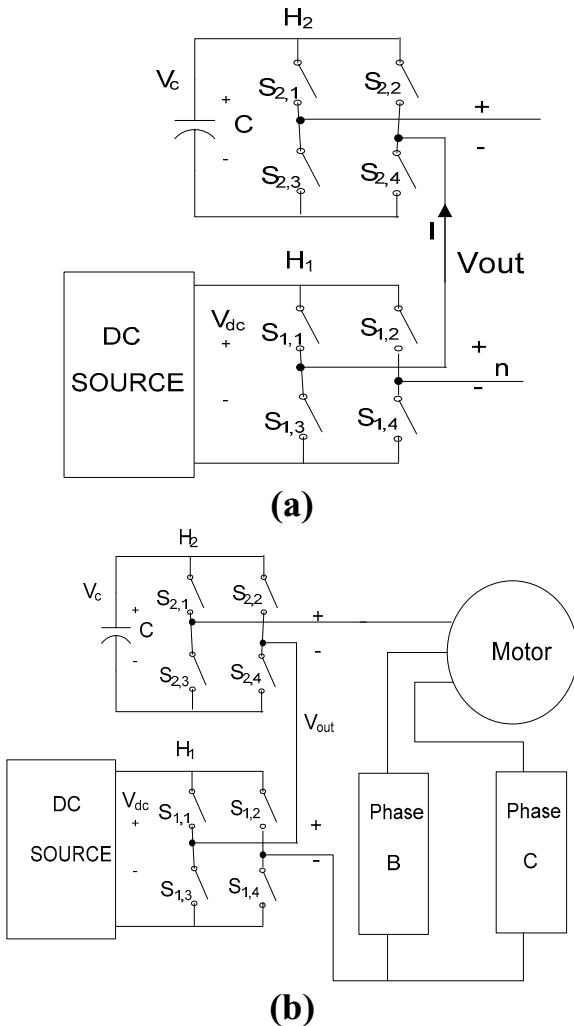


Fig. 1. Topology of the proposed multilevel converter with a single DC source for first level and capacitors for other levels (a) single-phase topology; (b) three-phase topology.

By opening and closing the switches of  $H_1$  appropriately, the output voltage  $v_1$  can be made equal to  $-V_{dc}$ , 0, or  $V_{dc}$  while the output voltage of  $H_2$  can be made equal to  $-V_c$ , 0, or  $V_c$  by opening and closing its switches appropriately. Therefore, the output voltage of the converter is a combination

of  $V_{dc}$  and  $V_c$  which can have 9 possible values  $-(V_{dc}+V_c)$ ,  $-V_{dc}$ ,  $-(V_{dc}-V_c)$ ,  $-V_c$ , 0,  $V_c$ ,  $(V_{dc}-V_c)$ ,  $V_{dc}$ ,  $(V_{dc}+V_c)$ .

To regulate the capacitor's voltage to guarantee the output power quality, 7-level fundamental switching scheme has been proposed. This switching scheme uses a possible cycle to output  $-(V_{dc}+V_c)$ ,  $-V_{dc}$ ,  $-(V_{dc}-V_c)$ , 0,  $(V_{dc}-V_c)$ ,  $V_{dc}$ ,  $(V_{dc}+V_c)$  voltage levels, and the DC source is charging the capacitor simultaneously when producing  $-(V_{dc}-V_c)$  and  $(V_{dc}-V_c)$  which is called a charging cycle. Similarly, the switching scheme uses another possible cycle to output  $-(V_{dc}+V_c)$ ,  $-V_{dc}$ ,  $-V_c$ , 0,  $V_c$ ,  $V_{dc}$ ,  $(V_{dc}+V_c)$  voltage levels, and the capacitor can be discharged simultaneously which is called a discharging cycle. Then the capacitors' voltage can be regulated by charging and discharging when the multilevel converter is running. When  $V_c = V_{dc}/2$  is chosen, the output voltage waveform is a 7-level waveform. Although PWM control method is popular for inverters regardless of their topologies [8-13], the 7-level fundamental frequency switching control is a good method for the hybrid cascaded H-bridge multilevel converter, which is shown in Fig. 2. This switching scheme is using 3 switching angles  $\theta_1$ ,  $\theta_2$  and  $\theta_3$  to output a voltage waveform, and to eliminate the low order 5<sup>th</sup> and 7<sup>th</sup> harmonics [14-17]. The solutions of the switching angles can be solved by several methods [18-21], such as resultant method [18-19]. For the 7-level hybrid cascaded H-bridge motor drive control, the output voltage can be represented by the mathematical model

$$V(\omega t) = \sum_{n=1,3,5 \dots}^{\infty} \frac{2V_{dc}}{n\pi} (\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)) \sin(n\omega t) \quad (2)$$

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = m$$

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0$$

For convenience, here the modulation index is defined as

$$m = \frac{\pi V_1}{2V_{dc}} \quad (3)$$

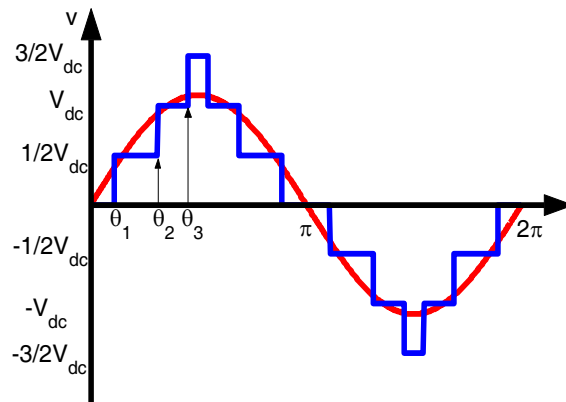


Fig. 2. 7-level equal step output voltage waveform.

From Fig. 2, it can be seen that the capacitor is discharging when the inverter outputs voltage  $-(V_{dc}+V_c)$  and  $(V_{dc}+V_c)$ . During a cycle, if the discharging amount is greater than the charging amount, then the capacitor's voltage balance is not possible. For high modulation index range above 1.54 of 7-level fundamental frequency switching control, the discharging amount is greater than the charging amount which results in the inability to regulate the capacitor's voltage.

In addition, the charging amount and discharging amount are also related to the power factor angle. This can be seen from Fig. 3 which shows the charging and discharging situation with different power factor angles (lead or lag).

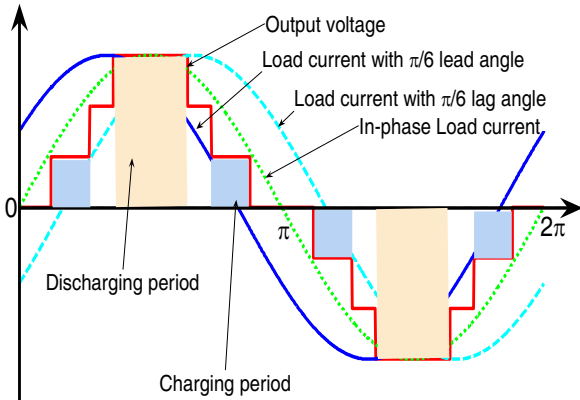


Fig. 3. Capacitor charging and discharging time with different load current without triplen harmonic voltage compensation.

### III. MODULATION INDEX EXTENSION CONTROL BY INJECTING TRIPLEN HARMONICS

To decrease the discharging time and increase the charging time, a new modulation extension control method by injecting triplen harmonic voltages into a 7-level output voltage is proposed. The triplen harmonic is a square wave with a frequency equal to 3 times the fundamental frequency with amplitude  $\frac{1}{2} V_{dc}$ . A triplen harmonic which can be represented by

$$V_{tri}(\omega t) = \sum_{n=1,3,5,\dots}^{\infty} \frac{2V_{dc}}{n\pi} \cos(n\theta_3) \sin(3n\omega t) \quad (4)$$

is injected into the 7-level output voltage, and the output voltage waveform is changed which is shown in Fig. 4. The triplen harmonic voltages will automatically cancel in the line-line voltages, and will not change the fundamental frequency contents. Therefore, here, the only effect is to change the charging period and discharging period. From Fig. 5, it can be seen that the original long discharging period has been changed into two short discharging periods.

To analyze the voltage balance situation due to capacitor charging and discharging in detail, define charging amount

$$Q_{charging} = \int_0^{2\pi} I_{charging} d\theta \quad (5)$$

and discharging amount

$$Q_{discharging} = \int_0^{2\pi} I_{discharging} d\theta \quad (6)$$

Then in a whole cycle, the net accumulation amount is defined as

$$Q_{accumulation} = Q_{charging} - Q_{discharging} \quad (7)$$

Therefore, if capacitor voltage regulation is possible, then the net accumulation amount must be greater than zero in a whole cycle.

Based on the above analysis, the net accumulation amount is calculated for the 7-level output voltage cases with and without triplen harmonic compensation method.

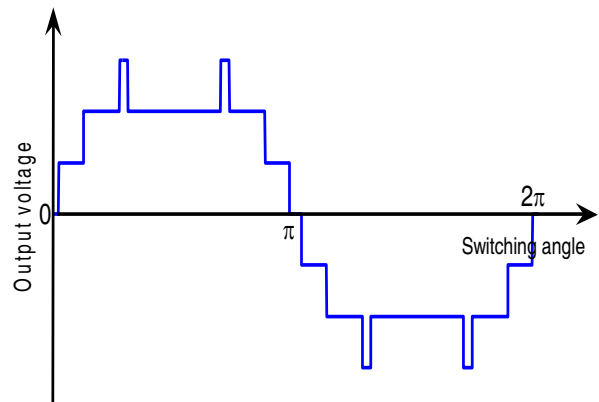


Fig. 4. Output voltage waveform with triplen harmonic compensation.

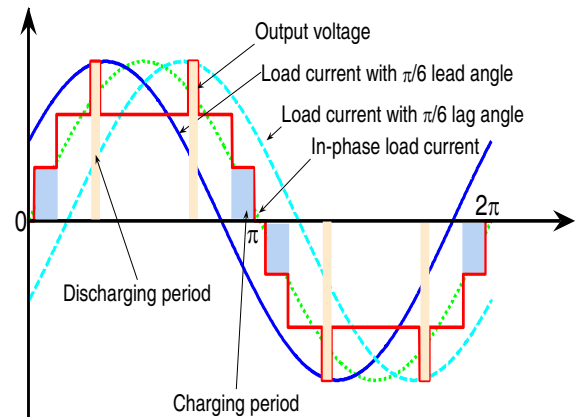


Fig. 5. Capacitor charging and discharging time with different load current with triplen harmonic voltage compensation.

If only 7-level fundamental frequency switching scheme is used to regulate the capacitor's voltage, the accumulation curve is shown in Fig. 6. The highest modulation index that can balance the capacitor's voltage is around 1.54.

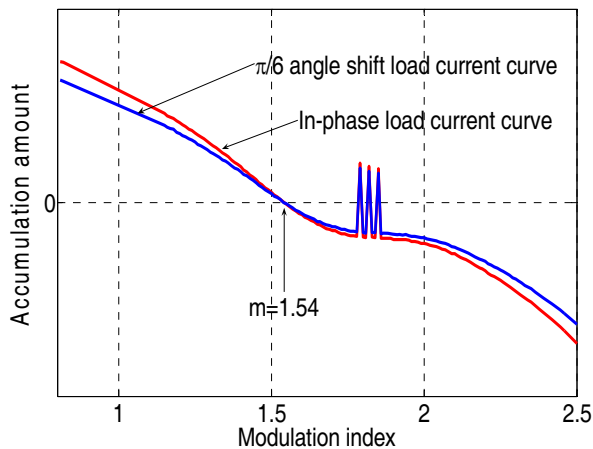


Fig. 6. Accumulation curve without triplen harmonic voltage compensation.

If triplen harmonic voltage compensation method is used, the accumulation curve is shown in Fig. 7. The highest modulation index that can balance the capacitor's voltage is around 2.

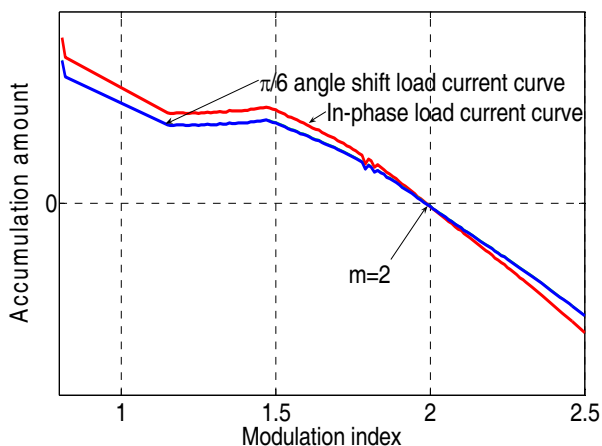


Fig. 7. Accumulation curve with triplen harmonic voltage compensation.

If Fig. 6 and Fig. 7 are compared, it can be seen that the triplen harmonic compensation method can increase the modulation index range by 33% for hybrid cascaded H-bridge multilevel converter to balance the capacitors' voltage.

#### IV. EXPERIMENT IMPLEMENTATION AND VALIDATION

To experimentally validate the proposed hybrid cascaded H-bridge multilevel motor drive control scheme, a prototype three-phase cascaded H-bridge multilevel converter has been built using MOSFETs as the switching devices which is shown in Fig. 8. Three 48 V DC power supplies (one for each phase) feed the motor drive. A real-time variable output

voltage, variable frequency three-phase motor drive controller based on Altera FLEX 10K field programmable gate array (FPGA) is used to implement the control algorithm. For convenience of operation, the FPGA controller is designed as a card to be plugged into a personal computer, which uses a peripheral component interconnect (PCI) bus to communicate with the microcomputer. The FPGA controller board will be based on a PCI bus. To maintain the capacitor's voltage balance, a voltage sensor is used to detect the capacitor's voltage and feed the voltage signal into the FPGA controller. A 1 kW induction motor is used as the load of the inverter.



Fig. 8. 10 kW multilevel inverter prototype.

To verify the proposed voltage balance control algorithm, the modulation index  $m=1.97$  is chosen for experiment. The phase voltage waveform and phase current waveform are shown in Fig. 9. The experiment shows that the capacitor's voltage can be regulated at 24 V which is half of the DC source voltage.

Fig. 10 shows the normalized FFT analysis of the phase voltage, and Fig. 11 shows the normalized FFT analysis of the phase current. From the voltage spectrum distribution in Fig. 10, it can be seen that the 5<sup>th</sup> and 7<sup>th</sup> harmonic voltages are near zero, and the triplen harmonic voltages (such as the 3<sup>rd</sup>, 9<sup>th</sup> etc.) are not zero. From the current spectrum distribution shown in Fig. 11, it also can be seen that it has very low 5<sup>th</sup> or 7<sup>th</sup> current harmonics 1.3% and 0.2%, respectively, and very low triplen current harmonics.

Further experiments show that for high modulation index range, 7-level output voltage waveform with triplen harmonic compensation can balance the capacitors' voltages, but 7-level output voltage waveform without triplen harmonic compensation can not balance the capacitors' voltages.

In theory, the voltage balance can reach modulation index  $m=2.0$ . But, for actual experiments, due to the switching loss, conduction loss of the switching devices and the wire copper loss of the circuit, the modulation index for capacitor's voltage balance is a little less than 2.0. In the experiments, if the modulation index is higher than 1.97, it is shown that the capacitor's voltage is maintained at a lower voltage instead of half of the DC source voltage.

## V. CONCLUSIONS

This paper proposed a new modulation extension control algorithm for 7-level hybrid cascaded H-bridges multilevel converters which only use one power source for each phase to balance the capacitors' voltages while producing desired 7-level voltage waveforms. It can be derived from the simulation and experiment results that this control algorithm can balance the capacitors' voltages while producing higher fundamental voltages with specific low order harmonics eliminated. This control method can effectively extend the modulation range to output higher fundamental frequency voltage compared to the traditional 7-level fundamental frequency switching scheme, and is promising to high power motor drive applications.

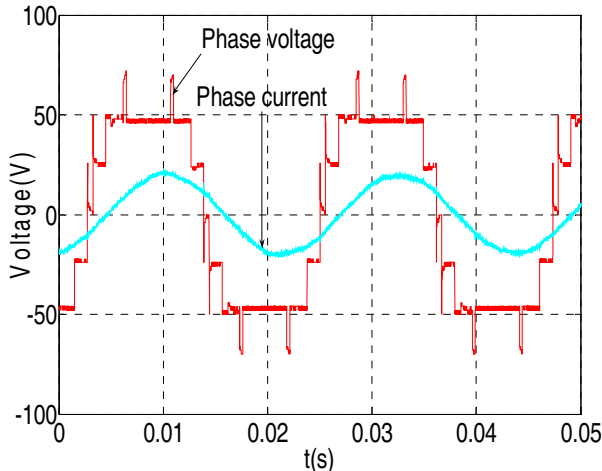


Fig. 9. Experimental voltage and current waveforms with a motor load and regulated capacitor's voltage.

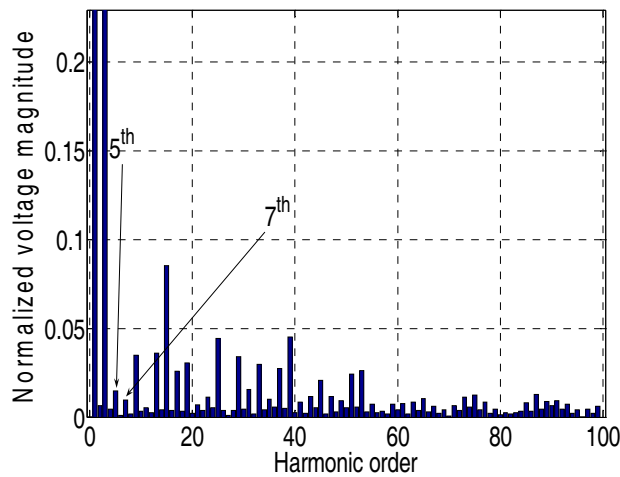


Fig. 10. Normalized FFT analysis of phase voltage shown in Fig. 9.

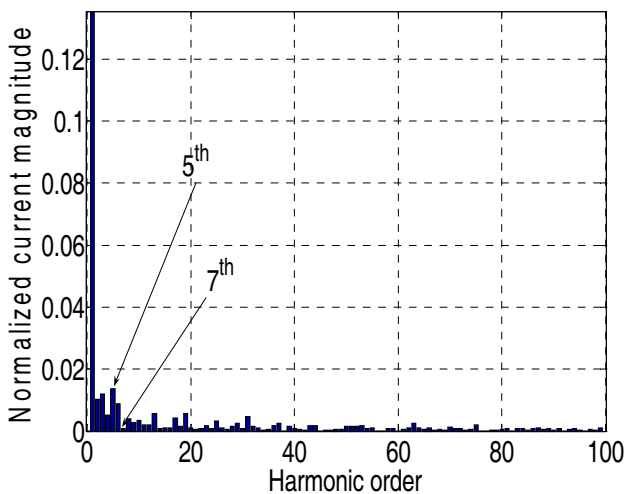


Fig. 11. Normalized FFT analysis of phase current shown in Fig. 9.

## REFERENCES

- [1] L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Transactions on Industry Applications*, vol. 35, no. 1, Jan./Feb. 1999, pp. 36-44.
- [2] J. S. Lai and F. Z. Peng, "Multilevel converters – A new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no.3, May/June 1996, pp. 509-517.
- [3] J. Rodriguez, J. Lai, and F. Peng, "Multilevel inverters: a survey of topologies, controls and applications," *IEEE Transactions on Industry Applications*, vol. 49, no. 4, Aug. 2002, pp. 724-738.
- [4] P. Hammond, "A new approach to enhance power quality for medium voltage ac drives," *IEEE Transaction on Industry Applications*, vol. 33, Jan./Feb. 1997, pp. 202-208.
- [5] W. A. Hill and C. D. Harbourt, "Performance of medium voltage multilevel inverters," *IEEE Industry Applications Society Annual Meeting*, October 1999, Phoenix, AZ, pp. 1186-1192.
- [6] Z. Du, L.M. Tolbert, J.N. Chiasson, B. Ozpineci, H. Li, A.Q. Huang, "Hybrid cascaded H-bridges multilevel motor drive control for electric vehicles," *IEEE Power Electronics Specialists Conference*, June, 18-22, 2006, Juhu, Korea, pp. 1-6.
- [7] Z. Du, L. M. Tolbert, J. N. Chiasson, "A cascade multilevel inverter using a single fuel cell DC source," *IEEE Applied Power Electronics Conference*, March 19-23, 2006, Dallas, Texas, vol. 1, pp. 419-423.
- [8] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *IEEE Transaction on Power Electronics*, vol. 7, no. 3, July 1992, pp. 497-505.
- [9] L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel PWM methods at low modulation indices," *IEEE Transaction on Power Electronics*, vol. 15, no. 4, July 2000, pp. 719-725.
- [10] L. M. Tolbert, T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Transaction on Industry Applications*, vol. 35, no. 5, Sept./Oct. 1999, pp. 1098-1107.
- [11] J. Vassallo, J. C. Clare, P. W. Wheeler, "A power-equalized harmonic-elimination scheme for utility-connected cascaded H-bridge multilevel converters," *IEEE Industrial Electronics Society Annual Conference*, 2-6 Nov. 2003, pp. 1185-1190.
- [12] S. Sirisukprasert, J.-S. Lai, T.-H. Liu, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters," *IEEE Transaction on Industrial Electronics*, vol. 49, no. 4, Aug. 2002, pp. 875-881.
- [13] P. C. Loh, D. G. Holmes, T. A. Lipo, "Implementation and control of distributed PWM cascaded multilevel inverters with minimum harmonic distortion and common-mode voltages," *IEEE Transaction on Power Electronics*, vol. 20, no. 1, Jan. 2005, pp. 90-99.
- [14] H. S. Patel and R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor inverters: Part I –harmonic elimination," *IEEE Transaction on Industry Applications*, vol. 9, May/June 1973, pp. 310-317.
- [15] H. S. Patel and R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor inverters: Part II –voltage control technique," *IEEE Transaction on Industry Applications*, vol. 10, Sept./Oct. 1974, pp. 666-673.

- [16] P. N. Enjeti, P. D. Ziogas, J. F. Lindsay, "Programmed PWM techniques to eliminate harmonics: A critical evaluation" *IEEE Transaction on Industry Applications*, vol. 26, no. 2, March/April. 1990. pp. 302 – 316.
- [17] Z. Du, L.M. Tolbert, J.N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, March 2006, pp. 459-469.
- [18] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, Z. Du, "Control of a multilevel converter using resultant theory," *IEEE Transactions on Control System Theory*, vol. 11, no. 3, May 2003, pp. 345-354.
- [19] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, Z. Du, "A new approach to solving the harmonic elimination equations for a multilevel converter," *IEEE Industry Applications Society Annual Meeting*, October 12-16, 2003, Salt Lake City, Utah, pp. 640-645.
- [20] Z. Du, L. M. Tolbert, J. N. Chiasson, "Modulation extension control for multilevel converters using triplen harmonic injection with low switching frequency," *IEEE Applied Power Electronics Conference*, March 6-10, 2005, Austin, Texas, pp. 419-423.
- [21] T. Kato, "Sequential homotopy-based computation of multiple solutions for selected harmonic elimination in PWM inverters," *IEEE Transaction on Circuits and Systems I*, vol. 46, no. 5, May 1999, pp. 586-593.